SCALE™-2 1SC0450V2A0
Preliminary Description & Application Manual

Single-Channel Cost-Effective Driver Core with Fiber-Optic Interface for IGBTs up to 4500V and 6500V

Abstract

The 1SC0450V2A0 single-channel SCALE™-2 driver core combines unrivalled compactness with broad applicability and cost-effectiveness. It is designed for industrial and traction applications requiring high reliability. The 1SC0450V2A0 drives all usual high-voltage IGBT modules up to 4500V and 6500V. Up to four parallel-connected IGBT modules can be driven to cover higher power ratings. Multi-level topologies involving 3300V or 4500V IGBTs with higher isolation requirements can also be easily supported by the 1SC0450V2A0.

The 1SC0450V2A0 is equipped with versatile fiber-optic links (AVAGO HFBR-x522ETZ). It is the most compact driver core in its voltage and power range, featuring a footprint of only 60mm x 90mm and a maximum insertion height of 27.5mm. It allows even the most restricted insertion spaces to be efficiently used.
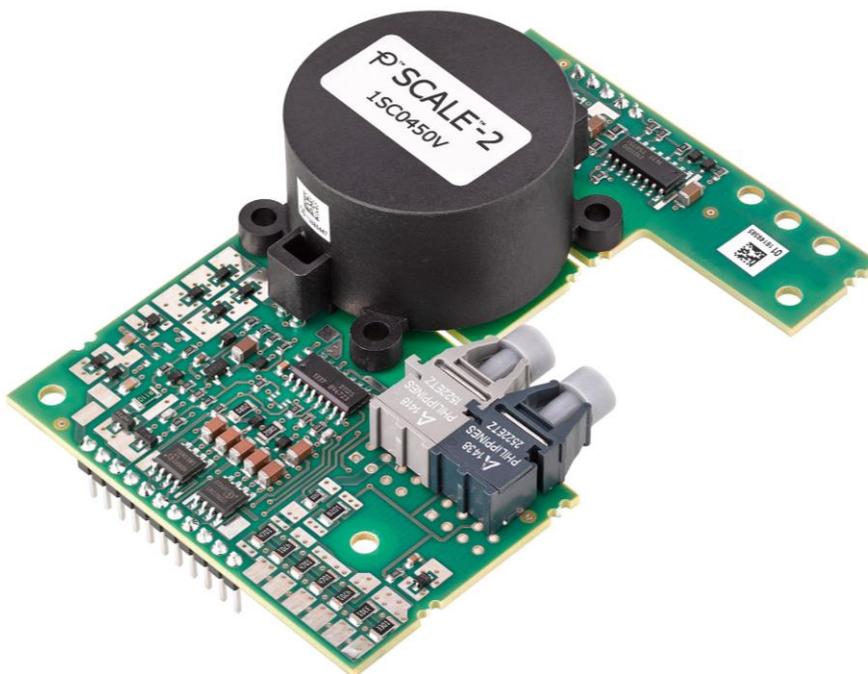
Fig. 1   1SC0450V2A0 driver core

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Driver Overview

The 1SC0450V2A0 is a driver core equipped with the latest SCALE-2 chipset from Power Integrations /1/. The SCALE-2 chipset comprises a set of application-specific integrated circuits (ASICs) that cover the main functions needed to design intelligent gate drivers. The SCALE-2 driver chipset is a further development of the proven SCALE™-1 technology /2/.

The 1SC0450V2A0 targets medium- and high-power IGBT applications up to 6500V. The driver supports switching frequencies up to 10kHz with best-in-class efficiency. The 1SC0450V2A0 comprises a complete single-channel IGBT driver core, fully equipped with an isolated DC/DC converter, optical signal interface, short-circuit protection, Advanced Active Clamping and supply-voltage monitoring. Additional features such as gate boosting or power supply short-circuit protection – which protects the driver in case of VISO to COM or gate-emitter short circuits – are also implemented and provide further driving benefits.
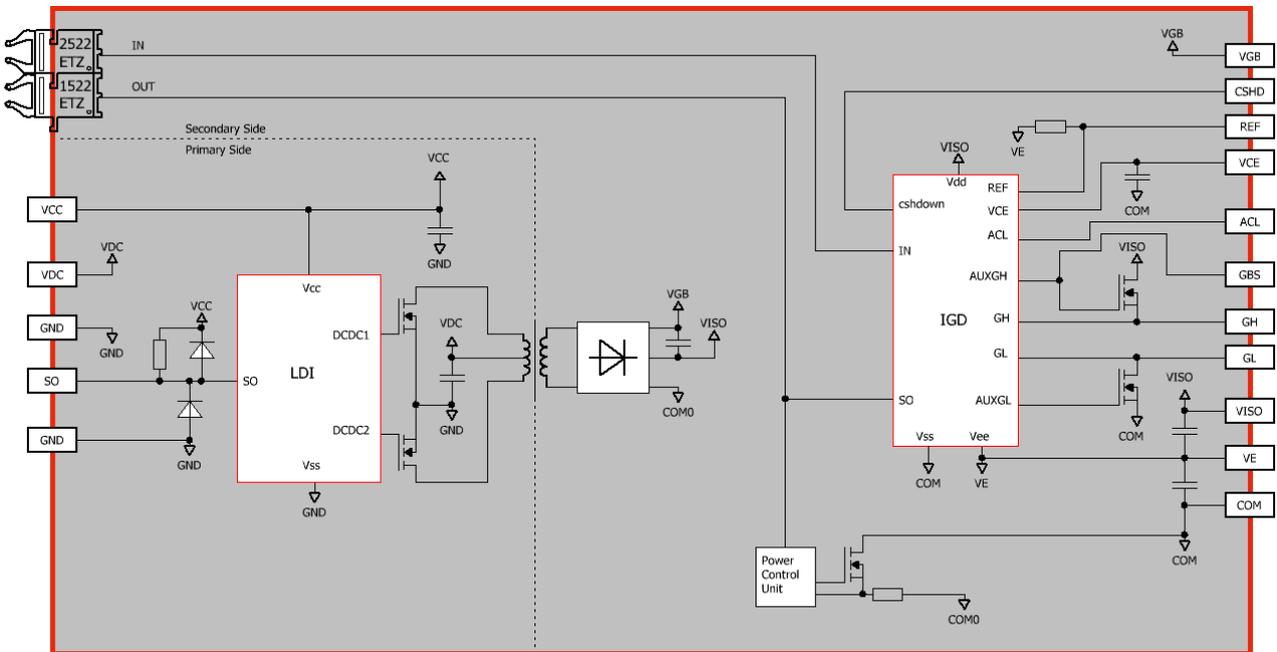
Fig. 2   Block diagram of the 1SC0450V2A0 driver core

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Mechanical Dimensions
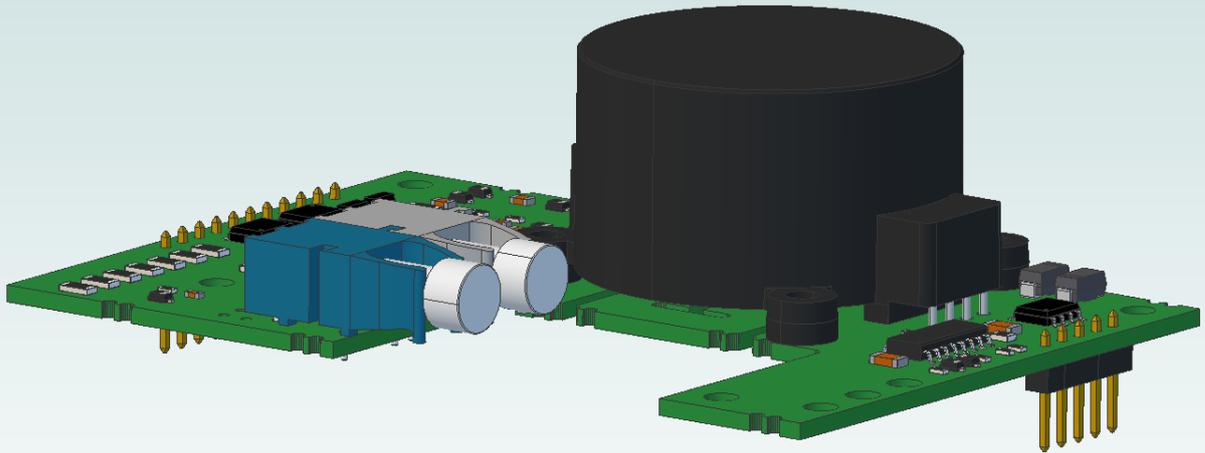
Fig. 3   Interactive 3D drawing of the 1SC0450V2A0

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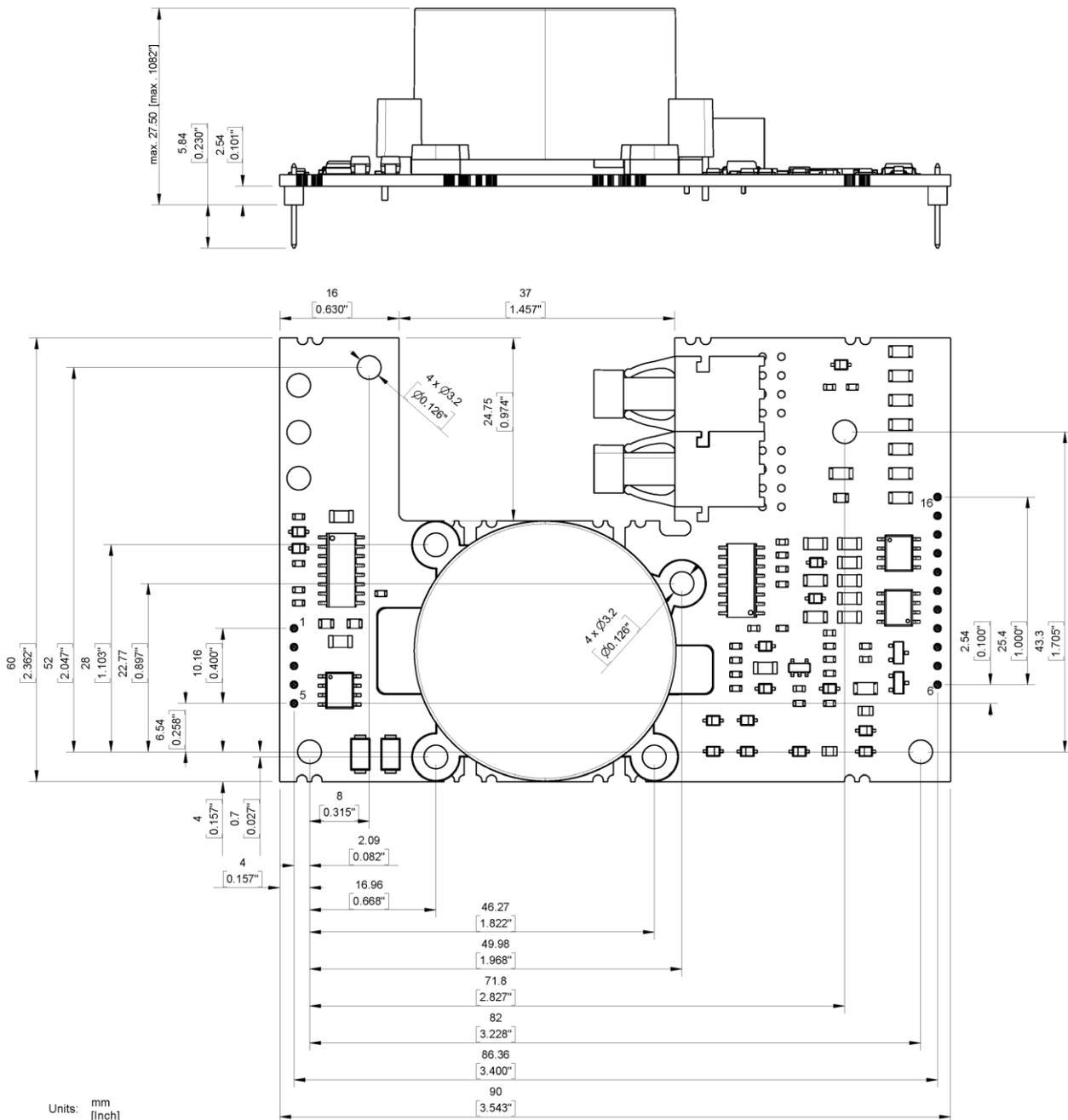
Fig. 4   Mechanical drawing of the 1SC0450V2A0

The primary-side and secondary-side pin grid is 2.54mm (100mil) with a pin cross-section of 0.64mm x 0.64mm. Total outline dimensions of the board are 60mm x 90mm. The total height of the driver is maximum 27.5mm measured from the bottom of the pin bodies to the top of the populated PCB.

Note that the mechanical fixing points are placed in the clearance and creepage paths. Insulated fixation material (screws, distance bolts) must therefore be used in order not to reduce these. The fixing points support M3 screw size.

Recommended diameter of solder pads: Ø 2mm (79mil)
Recommended diameter of drill holes: Ø 1mm (39mil)

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Pin Designation

Pin No. and Name	Function
Primary Side	
1 SO	Status output primary side; normally pulled up to VCC over a 10kΩ resistor, pulled down to low in case of a fault
2 GND	Ground
3 VCC	Supply voltage; 15V supply for primary side
4 VDC	DC/DC converter supply
5 GND	Ground
Secondary Side	
6 VGB	Gate-boosting power supply
7 VISO	DC/DC output
8 COM	Secondary-side ground
9 CSHD	Set turn-off delay after fault detection; capacitor to COM
10 GH	Gate high; pulls gate high through turn-on resistor
11 GBS	Gate-boosting signal
12 VE	IGBT emitter
13 GL	Gate low; pulls gate low through turn-off resistor
14 ACL	Active clamping feedback; leave open if not used
15 REF	Set V_{CE} detection threshold through resistor to VE
16 VCE	V_{CE} sense; connect to IGBT collector through impedance network
Optical Connectors	
IN	Optical input; signal input to turn the IGBT on and off
OUT	Optical output; gate driver status output

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Recommended Interface Circuitry for the Primary-Side Connector
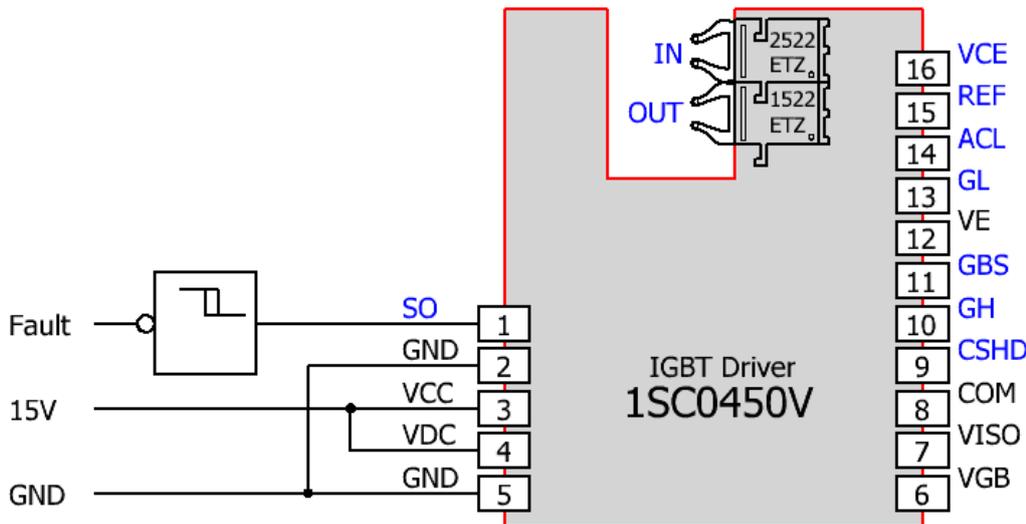
Fig. 5   Recommended user interface of the 1SC0450V2A0 (primary side)

Description of Primary-Side Interface

General

The primary-side interface of the 1SC0450V2A0 driver is very simple and easy to use.

The driver primary side is equipped with a 5-pin interface connector with the following terminals:

- 2x power-supply terminals VCC and VDC
- 2x ground terminals GND
- 1x status output SO (indicating a fault during primary-side under-voltage)

All inputs and outputs are ESD-protected.

VCC terminal

The driver has one VCC terminal on the interface connector to supply the primary-side electronics with 15V.

VDC terminal

The driver has one VDC terminal on the interface connector to supply the DC/DC converter for the secondary side.

VDC should be supplied with 15V. It is recommended to connect the VCC and VDC terminals to a common 15V power supply. In that case, the driver limits the inrush current at startup and no external current limitation of the voltage source for VDC is needed.

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GND

Both ground pins must be connected together with low parasitic inductance. A common ground plane is strongly recommended. Furthermore it is recommended to shield all primary-side circuitry with the ground plane. The connecting distance between the ground pins must be kept to a minimum.

SO (status output)

When no primary-side under-voltage condition is detected, an internal pull-up resistor of 10kΩ keeps the output level at the voltage level of VCC. When a primary-side supply under-voltage is detected, the status output SO goes to low (connected to GND). The SO output is automatically reset (returning to the voltage level of VCC) when the under-voltage on the primary side disappears.

The maximum SO current in a fault condition must not exceed the value specified in the driver data sheet /3/.

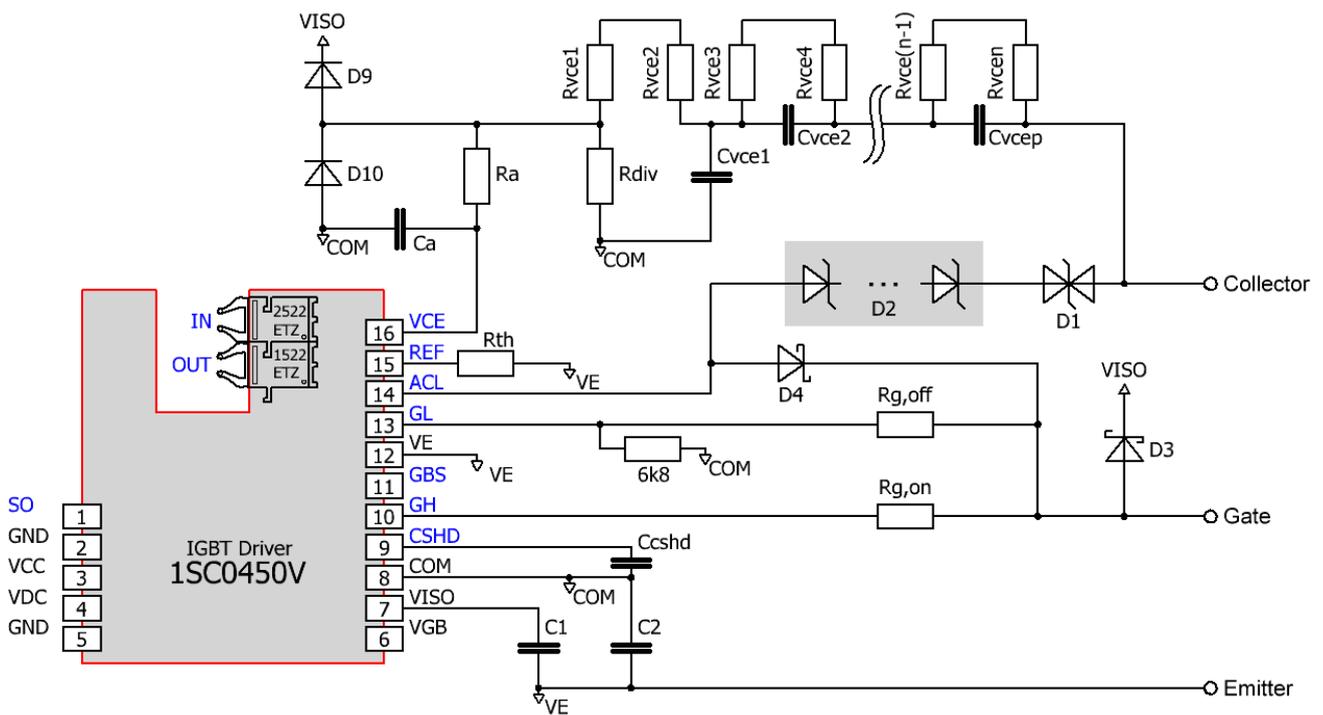### Recommended Interface Circuitry for the Secondary Side Connector

Fig. 6 Recommended user interface of the 1SC0450V2A0 (secondary side) without gate boosting (refer to chapter "Gate Boosting" and Fig. 11 for gate-boosting circuitry)

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Description of Secondary-Side Interface

General

The driver's secondary side is equipped with an 11-pin interface connector with the following terminals:

- 1x DC/DC output terminal VISO
- 1x emitter terminal VE
- 1x secondary-side ground COM
- 1x collector sense terminal VCE
- 1x reference terminal REF for short-circuit protection
- 1x input terminal CSHD to set the turn-off delay after fault
- 1x active clamping terminal ACL
- 1x turn-on gate terminal GH
- 1x turn-off gate terminal GL
- 1x gate-boosting power supply VGB
- 1x gate-boosting signal GBS

All inputs and outputs are ESD-protected.

DC/DC output (VISO), emitter (VE) and COM terminals

The driver is equipped with blocking capacitors on the secondary side of the DC/DC converter (for values refer to the data sheet /3/). IGBTs with a gate charge of up to 4.7µC can be driven without additional external capacitors (C_1 and C_2 in Fig. 6 are not assembled). Eq. 1 and Eq. 2 give the recommended capacitance value of C_1 and C_2 for gate charges above this value:

$$C_1[\mu F] \geq (Q_G[\mu C]-4.7)\cdot 4$$

C_1 in Fig. 6; 4µF blocking capacitance per 1µC gate charge between VISO and VE — Eq. 1

$$C_2 = \frac{C_1}{2}$$

C_2 in in Fig. 6; blocking capacitance between VE and COM, half of the C_1 value — Eq. 2

Example: IGBT modules with a gate charge of up to 42µC can be driven with external capacitances of 149.2µF between the VISO and VE terminals and 74.6µF between the VE and COM terminals (C_1 and C_2 of Fig. 6).

If the capacitance C_1 (or C_2) exceeds 200µF (or 100µF), please contact the Power Integrations support service.

The blocking capacitors must be connected as close as possible to the driver's terminal pins with minimum inductance. Ceramic capacitors with a dielectric strength ≥25V are recommended.

No static load must be applied between VISO and VE, or between VE and COM. A static load can be applied between VISO and COM if necessary.

Reference terminal (REF)

The reference terminal REF allows the threshold to be set for short-circuit protection with a resistor placed between REF and VE (R_{th} of Fig. 6). An internal resistor of 68kΩ sets the default threshold value to 10.2V. It can be reduced with the use of an external resistor R_{th} according to the following Eq. 3:

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$$R_{th}[k\Omega] = \frac{68 \cdot V_{th}[V]}{10.2 - V_{th}[V]} \qquad \text{with } V_{th} < 10.2V \qquad \text{Eq. 3}$$

It is recommended to keep the reference voltage at its maximum default value of 10.2V (without using an external resistor R_{th}).

Collector sense (VCE)

The collector sense must be connected to the IGBT collector with the circuit shown in Fig. 6 in order to detect a short circuit condition.

General information and recommendations:

- The overall value R_{tot} of the resistors R_{vcei} is calculated with equation Eq. 4:

$$R_{tot} = \sum_{i=1}^{n} R_{vcei} = R_{vce1} + ... + R_{vcen} \qquad \text{Eq. 4}$$

- It is recommended to dimension the overall value R_{tot} of the resistors in order for a current I_{Vce} of about 0.6…0.8mA to flow through them at the maximum DC-link voltage (Eq. 5). This current must not exceed 0.8mA. It is recommended to use series-connected resistors; the minimum creepage and clearance distances required for the application must be considered and the maximum voltage, power and temperature rating of the resistors used must not be exceeded. Dimensioning recommendations are given below.

$$I_{Vce} \cong \frac{V_{DC-link(max)}}{R_{tot}} = 0.6...0.8mA \qquad \text{Eq. 5}$$

- All resistors R_{vcei} (i ≥ 1) must have the same value.

- R_{div} allows the static threshold detection level V_{CEth} to be increased if required (resistive voltage divider with R_{tot}). R_{div} can be calculated with Eq. 6 in order to determine the static detection level V_{CEth}.

$$R_{div}[k\Omega] = R_{tot}[k\Omega] \cdot \frac{V_{th}[V] + |V_{GL}[V]|}{V_{CEth}[V] - V_{th}[V]} \qquad (V_{CEth} > V_{th}) \qquad \text{Eq. 6}$$

$|V_{GL}|$ is the absolute value of the gate-emitter turn-off voltage at the driver output. It depends on the driver load and can be found in the driver data sheet /3/. V_{th} is the reference value set at the reference terminal REF as described in the "Reference terminal (REF)" section.

- The recommended range for the overall capacitance value C_{tot} is given in Eq. 7:

$$C_{tot} = \frac{1}{\sum_{k=1}^{p} \frac{1}{C_{vcek}}} = 1...4pF \qquad \text{Eq. 7}$$

- All capacitances C_{vcek} with k≥2 must have the same value.

- The capacitance C_{vce1} must be chosen such that the Eq. 8 is satisfied:

$$\frac{C_{vce1}}{C_{tot}} = (0.7...0.9) \cdot \frac{R_{tot}}{R_{vce1} + R_{vce2}} \qquad \text{Eq. 8}$$

- The maximum voltage rating of the resistors and capacitors used must not be exceeded. Peak values and average values must be considered. Dimensioning recommendations are given below.

- The diodes D_9 and D_{10} must have a very low leakage current and a blocking voltage of >40V (e.g. BAS416). Schottky diodes must be explicitly avoided.

- R_a and C_a are used to set the response time.

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Recommended values for 6500V IGBTs with DC-link voltages up to 4500V

- $R_{vce1}=R_{vce2}=...=R_{vce30}=200k\Omega$ (500mW, 400V_{peak}, 1%)
- $R_{div}=620k\Omega$ (0603, 1%)
- $C_{vce1}=15pF$ (C0G, 1000V, 5%)
- $C_{vce2}=C_{vce3}=...=C_{vce15}=22pF$ (C0G, 630V, 5%)
- $C_a=22pF$ (C0G, 50V, 5%)
- R_{th}=not assembled
- R_a=refer to Table 1 below (0603, 1%)

This setup uses 30 resistors R_{vcei} and 15 capacitors C_{vcek} and leads to a static desaturation detection threshold of about 201V.

$V_{DC-Link}$	$R_a=68k\Omega$	$R_a=91k\Omega$	$R_a=120k\Omega$
4500V	5.3µs	6.9µs	9.0µs
3000V	5.3µs	7.0µs	9.1µs
2250V	5.5µs	7.0µs	9.1µs
1500V	7.2µs	8.0µs	9.4µs
1125V	9.9µs	10.3µs	11.1µs
900V	14.1µs	14.1µs	14.2µs

Table 1   Typical response time as a function of the resistance R_a and the DC-link voltage $V_{DC-Link}$

Table 1 gives indicative values only. The response time depends on the specific layout and the IGBT module used. It is therefore recommended to measure the short-circuit duration in the final design.

Note that slow IGBT modules may report a wrong V_{CE} desaturation fault at turn-on. It is therefore recommended to test the setup under worst case conditions (maximum DC-link voltage, maximum collector current and highest IGBT junction temperature). Please also refer to AN-1101 /4/ for more information.

Recommended values for 4500V IGBTs with DC-link voltages up to 3200V

- $R_{vce1}=R_{vce2}=...=R_{vce20}=220k\Omega$ (500mW, 400V_{peak}, 1%)
- $R_{div}=620k\Omega$ (0603, 1%)
- $C_{vce1}=15pF$ (C0G, 1000V, 5%)
- $C_{vce2}=C_{vce3}=...=C_{vce10}=22pF$ (C0G, 630V, 5%)
- $C_a=22pF$ (C0G, 50V, 5%)
- R_{th}=not assembled
- R_a=refer to Table 2 below (0603, 1%)

This setup uses 20 resistors R_{vcei} and 10 capacitors C_{vcek} and leads to a static desaturation detection threshold of about 150V.

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$V_{DC\text{-}Link}$	$R_a=68k\Omega$	$R_a=91k\Omega$	$R_a=120k\Omega$
3200V	5.1µs	6.8µs	8.8µs
2000V	5.2µs	6.8µs	8.9µs
1500V	6.1µs	7.0µs	8.9µs
1000V	8.8µs	9.3µs	10.3µs
800V	12.7µs	13.1µs	12.9µs

Table 2   Typical response time as a function of the resistance R_a and the DC-link voltage $V_{DC\text{-}Link}$

Table 2 gives indicative values only. The response time depends on the specific layout and the IGBT module used. It is therefore recommended to measure the short-circuit duration in the final design.

Note that slow IGBT modules may report a wrong V_{CE} desaturation fault at turn-on. It is therefore recommended to test the setup under worst case conditions (maximum DC-link voltage, maximum collector current and highest IGBT junction temperature). Please also refer to AN-1101 /4/ for more information.

Recommended values for 3300V IGBTs with DC-link voltages up to 2200V

- $R_{vce1}=R_{vce2}=…=R_{vce14}=220k\Omega$ (500mW, 400V_{peak}, 1%)

- $R_{div}=1.5M\Omega$ (0603, 1%)

- $C_{vce1}=15pF$ (C0G, 1000V, 5%)

- $C_{vce2}=C_{vce3}=…=C_{vce7}=22pF$ (C0G, 630V, 5%)

- $C_a=22pF$ (C0G, 50V, 5%)

- $R_{th}=$ not assembled

- $R_a=$ refer to Table 3 below (0603, 1%)

This setup uses 14 resistors R_{vcei} and 7 capacitors C_{vcek} per channel and leads to a static desaturation detection threshold of about 50V.

$V_{DC\text{-}Link}$	$R_a=68k\Omega$	$R_a=91k\Omega$	$R_a=120k\Omega$
2200V	5.3µs	7.0µs	9.0µs
1500V	5.3µs	7.0µs	9.0µs
1100V	5.4µs	7.0µs	9.1µs
700V	7.6µs	8.1µs	9.3µs
600V	17.0µs	14.4µs	13.7µs

Table 3   Typical response time as a function of the resistance R_a and the DC-link voltage $V_{DC\text{-}Link}$

Table 3 gives indicative values only. The response time depends on the specific layout and the IGBT module used. It is therefore recommended to measure the short-circuit duration in the final design.

Note that slow IGBT modules may report a wrong V_{CE} desaturation fault at turn-on. It is therefore recommended to test the setup under worst case conditions (maximum DC-link voltage, maximum collector current and highest IGBT junction temperature). Please also refer to AN-1101 /4/ for more information.

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Input for adjusting the turn-off delay in fault condition (CSHD)

The terminal CSHD allows the delay in turning off the IGBT after a fault detection on the driver's secondary side (short-circuit, undervoltage, power supply short-circuit/overload) to be determined with a capacitor C_{cshd} (C0G/50V) with a maximum value of 10nF connected to COM. Table 4 shows the resulting delay as a function of the circuit used at pin CSHD.

Circuit at pin CSHD	Typical turn-off delay T_{cshd}	
Left open:	$T_{cshd}=0.2\mu s$	Eq. 9
Capacitor between CSHD and COM:	$T_{cshd}[\mu s]= \frac{C_{cshd}[pF]}{50}$ ($C_{cshd} \leq 10nF$)	Eq. 10

Table 4   Turn-off delay as a function of CSHD wiring

As soon as the fault turn-off delay time T_{cshd} has elapsed, the driver's channel is automatically turned off.

The driver's channel can also be turned off from the driver's fiber-optic input within the turn-off delay time T_{cshd} determined by the CSHD pin after a secondary-side fault detection.

Note that it will not be possible to turn the IGBT on during about 100ns per 100pF capacitance applied to CSHD after a fault condition, starting from the turn-off event of the IGBT (minimum off-time required).

Active Clamping (ACL)

Active clamping is a technique designed to partially turn on the power semiconductor as soon as the collector-emitter voltage exceeds a predefined threshold. The power semiconductor is then kept in linear operation.

Basic active clamping topologies implement a single feedback path from the IGBT's collector through transient voltage suppressor devices (TVS) to the IGBT gate. The 1SC0450V2A0 supports Advanced Active Clamping from Power Integrations, where the feedback is also provided to the driver's secondary side at pin ACL (Fig. 6): as soon as the voltage at pin ACL exceeds about 1.3V, the turn-off MOSFET is progressively switched off in order to improve the effectiveness of the active clamping and to reduce the losses in the TVS. The turn-off MOSFET is turned completely off when the voltage at pin ACL approaches 20V (measured to COM).

It is recommended to use the circuit shown in Fig. 6. The following parameters must be adapted to the application:

- For TVS D_1, D_2 it is recommended to use:
    - 3300V IGBTs with DC-link voltages up to 2200V: Seven unidirectional 300V TVS and one bidirectional 350V TVS. Good clamping results can be obtained with seven unidirectional TVS P6SMB300A and one bidirectional TVS P6SMB350CA from Diotec.
    - 4500V IGBTs with DC-link voltages up to 3200V: Eight unidirectional 400V TVS and one bidirectional 350V TVS. Good clamping results can be obtained with eight unidirectional TVS P6SMB400A and one bidirectional TVS P6SMB350CA from Diotec.
    - 6500V IGBTs with DC-link voltages up to 4350V: Ten unidirectional 440V TVS and one bidirectional 440V TVS. Good clamping results can be obtained with ten unidirectional TVS P6SMB440A and one bidirectional TVS P6SMB440CA from Diotec.

    At least one bidirectional TVS (D_1) (≥300V for 3300V IGBTs, ≥350V for 4500V IGBTs, ≥440V for 6500V IGBTs) must be used in order to avoid negative current flowing through the TVS chain during turn-on of the anti-parallel diode of the IGBT module due to its forward recovery behavior. Such a

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current could, depending on the application, lead to under-voltage of the driver secondary-side voltage VISO to VE (15V).

Note that it is possible to modify the number of TVS in a chain. The active clamping efficiency can be improved by increasing the number of TVS used in a chain if the total breakdown voltage remains at the same value. Note also that the active clamping efficiency is highly dependent on the type of TVS used (e.g. manufacturer).

- D_3 and D_4: It is recommended to use Schottky diodes with blocking voltages >35V (>1A depending on the application).

Please note that the diodes D_3 and D_4 must not be omitted if Advanced Active Clamping is used.

If active clamping is not used, the diode D_4 can be omitted. The pin ACLx must then be left open.

Gate turn-on (GH) and turn-off (GL) terminals

These terminals allow the turn-on (GH) and turn-off (GL) gate resistors to be connected to the gate of the power semiconductor. The GH and GL pins are available as separated terminals in order to set the turn-on and turn-off resistors independently without the use of an additional diode. Please refer to the driver data sheet /3/ for the limit values of the gate resistors used.

A resistor between GL and COM of 6.8kΩ (other values are also possible) may be used in order to provide a low-impedance path from the IGBT gate to the emitter even if the driver is not supplied with power. No static load (e.g. resistors) must be placed between GL and the emitter terminal VE.

Note, however, that it is not advisable to operate the power semiconductors within a half-bridge with a driver in the event of a low supply voltage. Otherwise, a steep increase of V_{CE} may cause partial turn-on of these IGBTs.

Gate Boosting Power Supply (VGB)

The driver supports an increased IGBT turn-on voltage source VGB to perform gate boosting. The voltage is generated by internal circuitry. No static load must be applied to VGB. Refer to the driver data sheet /3/ for more information.

Gate Boosting Signal (GBS)

The gate-boosting signal GBS is an auxiliary signal that has the same time waveform – but different voltage values – as the GH signal. Please refer to the driver data sheet for the exact voltage values /3/ and to the "Gate Boosting" section for more information.

Note that no static load must be applied to GBS. Refer to the driver data sheet /3/ for more information.

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Description of the Fiber-Optic Output of 1SC0450V2A0

During normal operation (i.e. the driver is supplied with power at nominal voltage and there is no fault anywhere), the status feedback is given by a "light on" at the optical link. A malfunction is signaled by a "light off".

Each edge of the control signal is acknowledged by the driver with a short pulse (the light remains off for about 700ns). As this can be observed by the host controller, this method allows simple and continuous monitoring of all drivers and fiber-optic links of the system. Fig. 7 shows the control and response signals of a gate driver in normal operation.
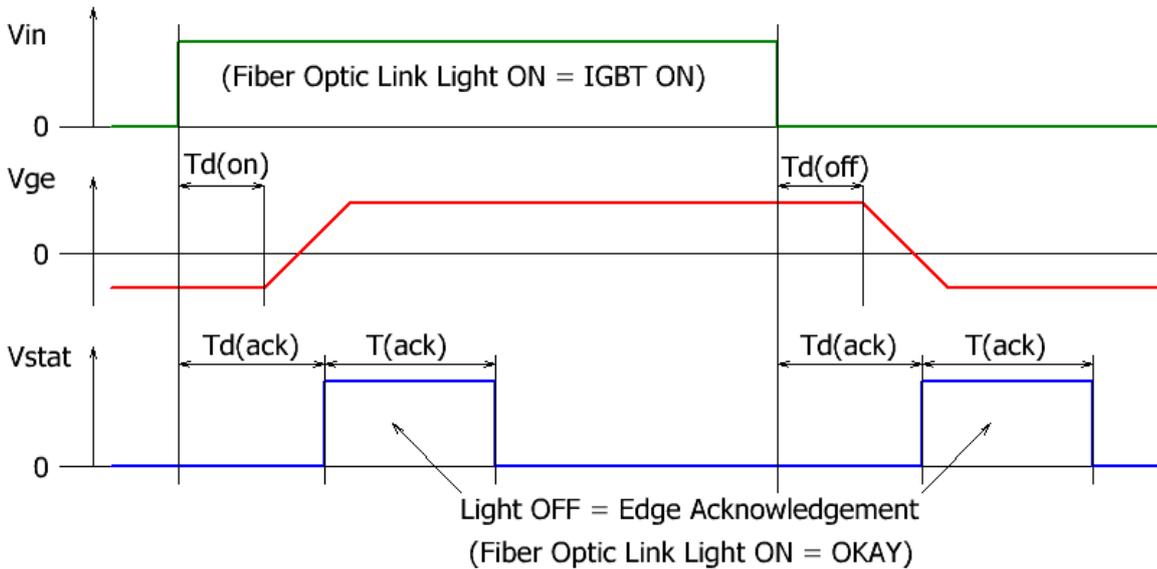

Fig. 7   Driver behavior and status feedback in normal operation

Fig. 8 shows the response of the driver in the event of a short-circuit fault. The fault status is transferred to the status feedback terminal after the response time. The light is then driven "off" during the delay in IGBT turn-off T_{cshd} extended by the delay required to clear the fault state $T_{d(cfs)}$. The driver turns the IGBT off after the response time + delay time T_{cshd}. The IGBT can be turned on again by applying a positive edge to the corresponding fiber-optic input after the fault status has disappeared.
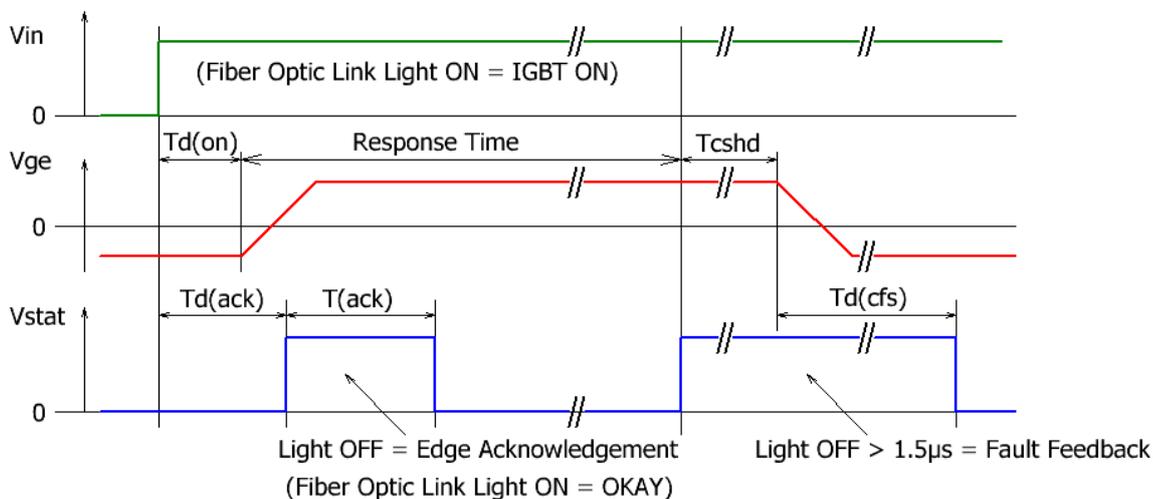

Fig. 8   Driver behavior and status feedback in the IGBT short-circuit condition

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In case of a secondary-side supply under-voltage fault, the fault status remains active as long as this under-voltage remains. The driver response in the event of a supply under-voltage on VISO-VE is shown in Fig. 9.
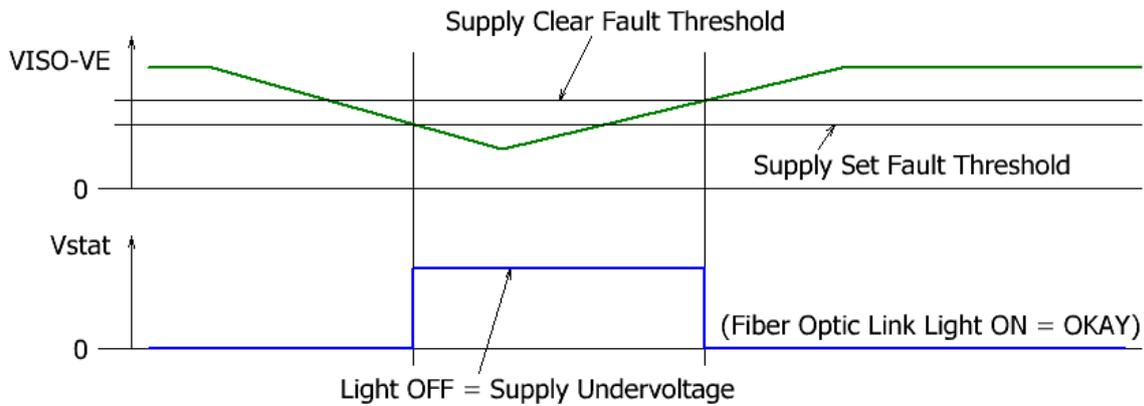

Fig. 9   *Status feedback in the event of a secondary-side supply under-voltage*

In case of power supply short-circuit/overload, the fault status is repeatedly activated for about 1ms.

During power-up, the status feedback will also show a fault condition until the supply under-voltage/power supply overload protection disappears.

Recommended Interface Circuitry for Fiber Optics with 1SC0450V2A0

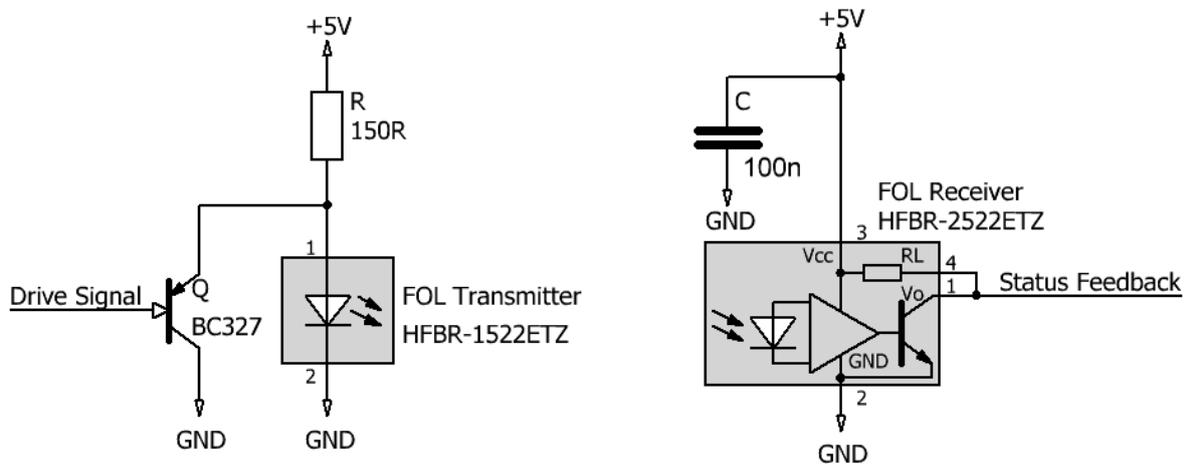The recommended circuitry to interface with the fiber-optic links is given in Fig. 10.

Fig. 10   *Recommended circuitry for the fiber-optic links*

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How Do 1SC0450V2A0 SCALE-2 Drivers Work in Detail?

Power supply and electrical isolation

The driver is equipped with a DC/DC converter to provide an electrically insulated power supply to the gate driver circuitry. The transformer features basic insulation according to IEC 61800-5-1 as well as IEC 60664-1 between the primary and secondary sides.

Note that the driver requires a stabilized supply voltage.

Power-supply monitoring

The driver's primary and secondary sides are equipped with a local under-voltage monitoring circuit.

In the event of a primary-side supply under-voltage, the under-voltage is signalized by the electrical status output SO. A primary-side under-voltage will not automatically cause a gate turn-off command. This condition has to be detected by the control logic which has to switch off and block the gate drive signal.

In case of a secondary-side supply under-voltage, the corresponding power semiconductor is driven with a negative gate voltage after the delay in IGBT turn-off (refer to "Input for adjusting the turn-off delay in fault condition (CSHD)") to keep it in the off-state (the channel is blocked) and a fault condition is monitored on the fiber-optic status feedback with the light off until the supply voltage exceeds the reference level for enabling.

The driver 1SC0450V2A0 is further equipped with an output short-circuit/heavy overload protection. The driver detects any short-circuit/overload current higher than the detection threshold (refer to the data sheet /3/ for more information) between gate and emitter as well as between VISO and COM. There is no protection against light overload of the power supply.

Note that a short circuit between gate and emitter might not be detected in the IGBT off-state (GL is connected to COM). The short circuit would then be detected when the driver turns on (GH is switched to VISO). A short-circuit/overload between VISO and COM is detected immediately.

In the event of a driver's power supply short-circuit/overload, the fault is immediately reported by the optical status feedback output. The fault signal applies – depending on the short circuit/overload condition – permanently or repeatedly for about 1ms. The primary-side supply VDC has to be switched off within the time frame given in the driver data sheet /3/ to prevent driver damage.

Parallel connection of IGBT modules

It is recommended to drive parallel-connected IGBT modules using a single 1SC0450V2A0 driver core. Appropriate gate circuitry has to be used. Please contact the Power Integrations support service for more information.

3-level or multilevel topologies

In applications with multi-level topologies, the turn-off sequence of the individual power semiconductors usually needs to be controlled by the host controller in case of a detected fault condition (e.g. short circuit, over-current), especially if no Advanced Active Clamping or Dynamic Advanced Active Clamping is implemented.

In that case, the turn-off delay in the fault condition of the different drivers can be adjusted to match the corresponding timing specifications. It is in particular possible to determine a specific turn-off delay for the

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inner IGBTs of a 3-level NPC topology as described in the section: "Input for adjusting the turn-off delay in fault condition (CSHD)". The driver's response time can also be adapted accordingly if required.

Note however that Advanced Active Clamping offers simple and safe protection that allows excessive collector-emitter overvoltages to be avoided in case of wrong commutation sequences in the short-circuit condition of 3-level converter topologies (refer to /6/ and /7/ for more information).

Gate Boosting

The 1SC0450V2A0 driver supports gate boosting. This feature allows the commutation speed of the collector-emitter voltage to be accelerated at turn-on after the critical phase of the diode reverse recovery behavior to reduce the IGBT turn-on losses.

A dedicated external circuit as shown in Fig. 11 is required. Detailed gate-boosting recommendations are not currently available.

Gate-boosting circuit principle

The "Gate Boosting Logic" according to Fig. 11 has to trigger the boosting function at the appropriate time during the IGBT turn on transition as illustrated in Fig. 12:

- The delay time between GBS and the required boosting time needs to be determined by the "Gate Boosting Logic" circuit.

- The pulse length of the boosting pulse also needs to be determined by the "Gate Boosting Logic" circuit. It must be limited to a few microseconds.

A turn-on pulse of the gate-boosting power switch Q_1 will be generated. This will lead to an increased turn-on gate current that will be injected into the IGBT gate over R_{gb}.

The boosting charge capability can be increased by adding an external capacitor C_{gb}. The minimum value C_{gb} of the external capacitor can be calculated according to Eq. 11.

$$C_{gb}[nF] = \frac{Q_{gb}[nC]}{V_{GH}[V] + |V_{GL}[V]|} - 22 \qquad\qquad C_{gb} \geq 0 \qquad\qquad \text{Eq. 11}$$

where Q_{gb} stands for the required boosting gate charge and has to be determined according to the IGBT module gate charge requirements. V_{GH} and V_{GL} are the absolute values of the turn-on and turn-off voltage at the driver output respectively. Their value can be found in the driver data sheet /3/. Note that Eq. 11 assumes a full discharge of C_{gb} during a gate-boosting event (worst case).

The gate-boosting capability is further limited by the minimum time span between two consecutive gate turn-on commands as well as by the gate-boosting power. The minimum required time T_{min} between two consecutive gate turn-on commands is given by Eq. 12. The gate-boosting efficiency is reduced if Eq. 12 is not respected.

$$T_{min}[\mu s] = 11 \cdot \left(1 + \frac{22 + C_{gb}[nF]}{22}\right) + T_{gb}[\mu s] \qquad\qquad \text{Eq. 12}$$

T_{gb} stands for the gate-boosting pulse length (Fig. 12). It is recommended to limit it to 1…5μs.

The maximum gate-boosting power must be within the absolute maximum ratings of the driver data sheet /3/. Eq. 13 gives a worst case approximation of the real gate-boosting power P_{gb}. It is sufficient to design the gate boosting such that P_{gb} is lower than the corresponding absolute maximum rating of the driver data sheet /3/.

$$P_{gb}[W] = 10^{-6} \cdot (C_{gb}[nF] + 22 + 6.5 \cdot T_{gb}[\mu s]) \cdot (V_{GH}[V] + |V_{GL}[V]|)^2 \cdot f[kHz] \qquad\qquad \text{Eq. 13}$$

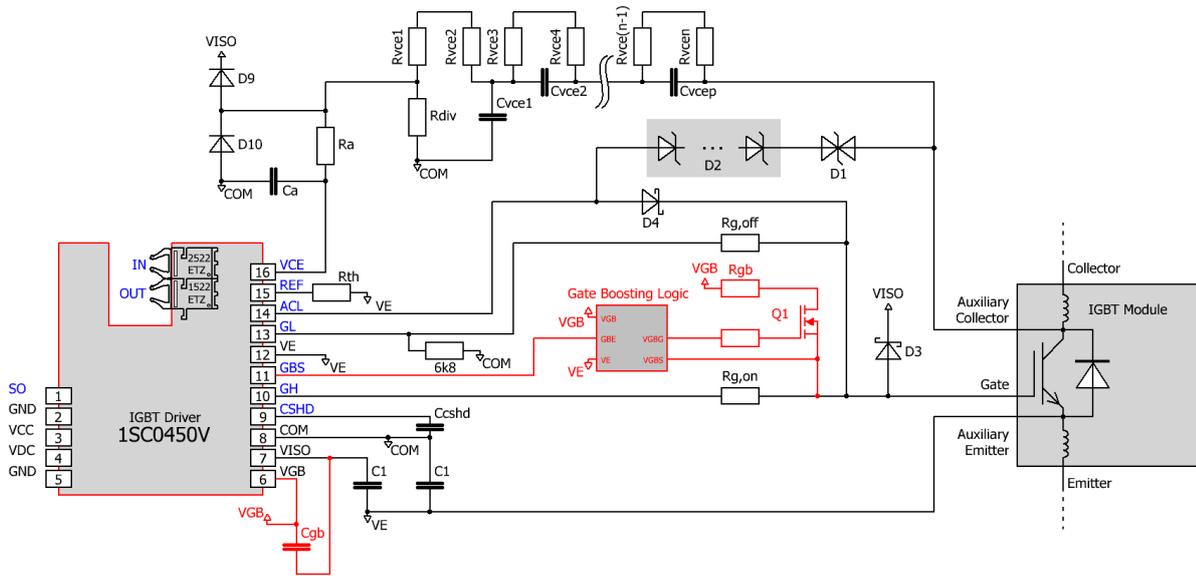## Preliminary Description & Application Manual

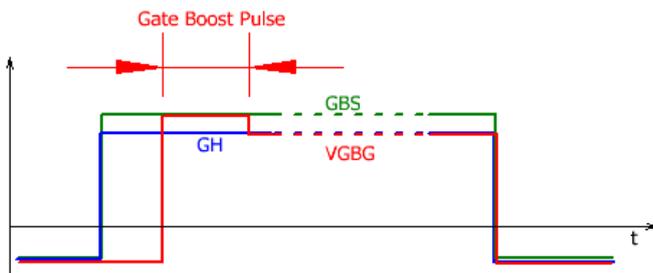*Fig. 11   Gate-boosting circuit principle – highlighted in red color*

Fig. 12   Gate-boosting signals

How to disable gate boosting?

Pins VGB and GBS must be left open. Note that the voltage values of the pins VGB and GBS are 50V and 35V respectively referred to COM (creepage and clearance distances).

Bibliography

/1/   Paper: Smart Power Chip Tuning, Bodo's Power Systems, May 2007

/2/   "Description and Application Manual for SCALE™ Drivers", Power Integrations

/3/   Data sheet SCALE™-2 driver core 1SC0450V2A0, Power Integrations

/4/   Application note AN-1101: Application with SCALE™-2 and SCALE™-2+ Gate Driver Cores, Power Integrations

/5/   Application note AN-0904: Direct Paralleling of SCALE™-2 Gate Driver Cores, Power Integrations

/6/   Application note AN-0901: Methodology for Controlling Multi-Level Converter Topologies with SCALE™-2 IGBT Drivers, Power Integrations

/7/   Paper: Safe Driving of Multi-Level Converters Using Sophisticated Gate Driver Technology, PCIM Asia, June 2013

Note: The Application Notes are available on the Internet at www.power.com/igbt-driver/go/app-note and the papers at www.power.com/igbt-driver/go/papers.

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The Information Source: SCALE-2 Driver Data Sheets

Power Integrations offers the widest selection of gate drivers for power MOSFETs and IGBTs for almost any application requirements. The largest website on gate-drive circuitry anywhere contains all data sheets, application notes and manuals, technical information and support sections: www.power.com.

Quite Special: Customized SCALE-2 Drivers

If you need an IGBT driver that is not included in the delivery range, please don't hesitate to contact Power Integrations or your Power Integrations sales partners.

Power Integrations has more than 25 years of experience in the development and manufacturing of intelligent gate drivers for power MOSFETs and IGBTs and has already implemented a huge number of customized solutions.

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Quality

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Ordering Information

Our international terms and conditions of sale apply.

Type Designation	Description
1SC0450V2A0-45	Single-channel SCALE-2 driver core for 4500V IGBTs
1SC0450V2A0-65	Single-channel SCALE-2 driver core for 6500V IGBTs

Product home page: www.power.com/igbt-driver/go/1SC0450

Refer to www.power.com/igbt-driver/go/nomenclature for information on driver nomenclature.

Information about Other Products

For other driver cores:

Direct link: www.power.com/igbt-driver/go/cores

For other drivers, product documentation and application support:

Please click: www.power.com

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