Design Example Report

Title	***6.6 W, Wide Range Input, Dual Output, Isolated Flyback Converter for Anti-Magnetizing Interference Using LinkSwitch™-XT2-900 LNK3696P***
Specification	85 VAC – 350 VAC Input; 16.5 V / 300 mA, 16.5 V / 100 mA Outputs
Application	Metering
Author	Applications Engineering Department
Document Number	DER-711
Date	July 23, 2021
Revision	1.1

Summary and Features

- Highly integrated solution with 900 V rated power MOSFET
- Output voltage regulation: 16.5 V ±5%, 16.5 V ±10%
- Programmable current limit selection feature of LinkSwitch-XT2-900
- >80% efficiency at full load condition, nominal input voltage
- <120 mW no-load input power at 230 VAC
- >6dB conducted EMI margin
- Can operate up to 350 VAC line input
- Can withstand 6 kV differential line surge
- Can withstand external magnetizing interference

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Important Note:
Although this board is designed to satisfy safety isolation requirements, the engineering prototype has not been agency approved. Therefore, all testing should be performed using an isolation transformer to provide the AC input to the prototype board.

1 Introduction

This engineering report describes an isolated flyback converter designed to provide dual output of 16.5 V at 300 mA and 16.5 V at 100 mA from a wide input voltage range of 85 VAC to 350 VAC. It was designed to withstand external magnetizing interference for metering applications. This adapter utilizes the LNK3696P from the LinkSwitch-XT2 900 V family of devices.

This document contains the power supply specification, schematic, bill of materials, transformer documentation, printed circuit layout, and performance data.

Figure 1 – Populated Circuit Board Photograph, Top.

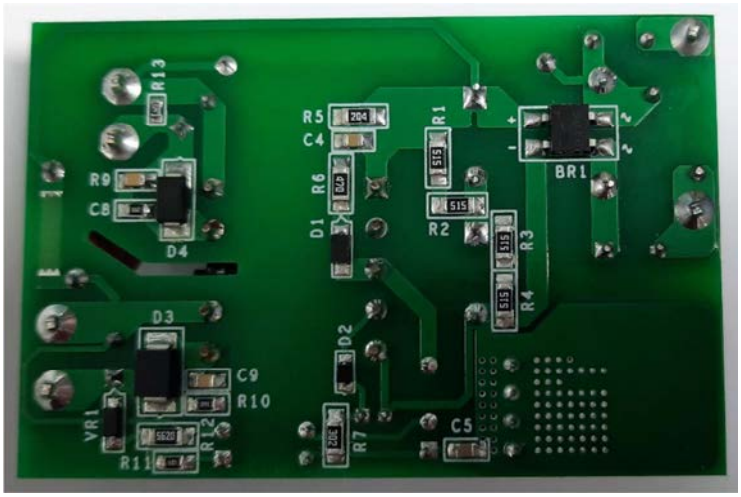


Figure 2 – Populated Circuit Board Photograph, Bottom.

2 Power Supply Specification

The table below represents the minimum acceptable performance of the design. Actual performance is listed in the results section.

Description	Symbol	Min	Typ	Max	Units	Comment
Input						
Voltage	V_{IN}	85	230	350	VAC	2 Wire – no P.E. Verified at 350 VAC.
Frequency	f_{LINE}	50	50/60	60	Hz	
No-load Input Power				150	mW	230 VAC.
Output						
Output Voltage 1	V_{OUT1}	15.675	16.5	17.325	V	±5%
Output Current 1	I_{OUT1}	30	300		mA	
Output Voltage 2	V_{OUT2}	14.85	16.5	18.15	V	±10%
Output Current 2	I_{OUT2}	10	100		mA	
Output Ripple Voltage	V_{RIPPLE}			240	mV	20 MHz Bandwidth.
Output Power	P_{OUT}		6.6		W	
Efficiency						
Full Load	$\eta_{Full-Load}$		80		%	At nominal input voltage, measured at output terminal.
Environmental						
Conducted EMI			CISPR22B / EN55022B Load floating			Resistive Load, 6 dB Margin.
Line Surge						
Differential Mode (L/N)				6	kV	Differential: 2 Ω
Ambient Temperature	T_{AMB}	0		50	°C	Free Convection, Sea Level in Sealed Enclosure.

3 Schematic

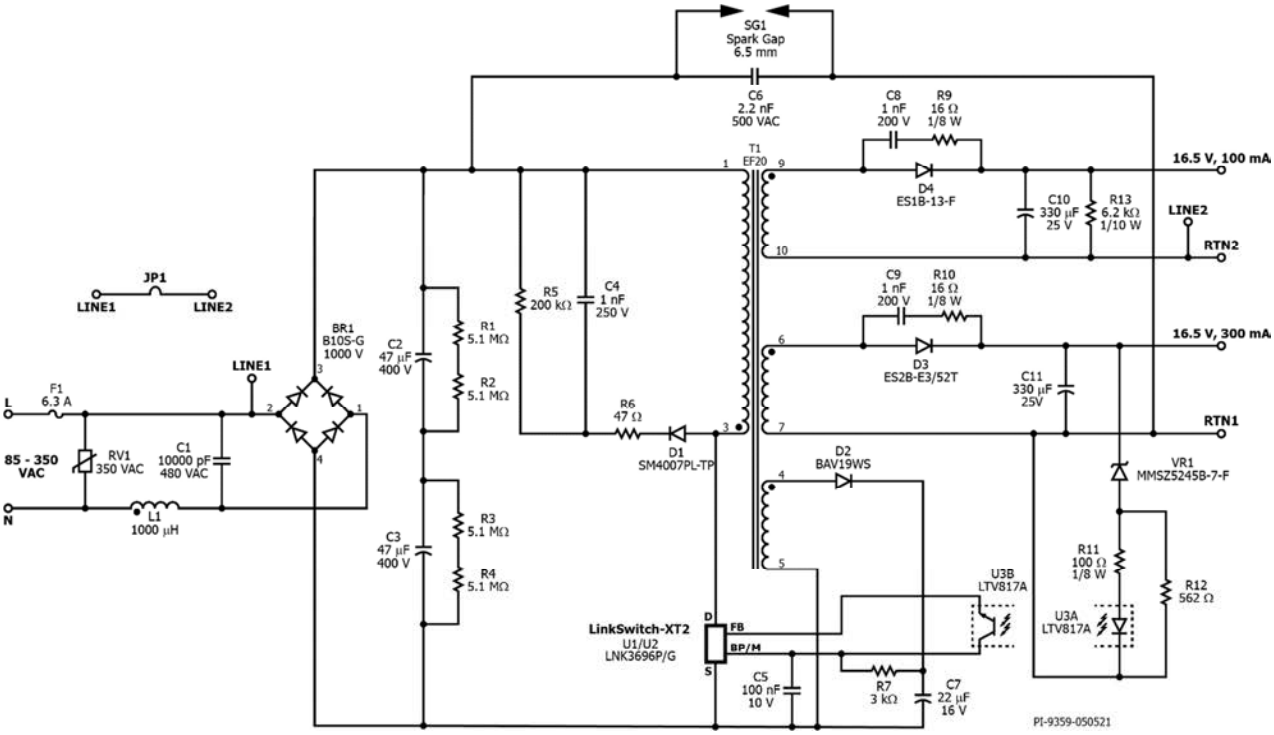


Figure 3 – Schematic.

4 Circuit Description

The LinkSwitch-XT2 900 V family of devices integrates a high-voltage (900 V rated) power MOSFET with an internal oscillator and ON/OFF controller inside a single monolithic IC. Unlike conventional pulse width modulation (PWM) controllers, LinkSwitch-XT2 900 V devices utilize a simple ON/OFF control scheme combined with an internal current limit circuitry to regulate the output voltage. The LNK3696P IC was used in an isolated flyback with dual output (16.5 V and 16.5 V) delivering 300 mA and 100 mA respectively.

4.1 Input Rectifier and Filter

The AC input is rectified by bridge rectifier BR1 and filtered by the bulk storage capacitors C2 and C3. Fuse F1 is a slow-blow, long time lag fuse and, together with the filter formed by C1, C2, C3, and L1, form a differential mode noise attenuator. Resistors R1, R2, R3 and R4 function to balance the voltage between the bulk capacitors in series. Varistor RV1 is used to clamp the voltage during line surge events.

4.2 LinkSwitch-XT2 Primary Side

The LNK3696P device (U1/U2) integrates the oscillator, controller, start-up and other protection circuitry as well as the high-voltage power MOSFET on a single monolithic IC.

The LNK3696P IC operates at a fixed current limit (I_{LIMIT}). Every enabled switching cycle, the primary current ramps to this current limit level. Output regulation is maintained by skipping switching cycles (ON/OFF control). The internal controller determines if the next switching cycle should be enabled or disabled (skipped) based on the current flowing into the FEEDBACK (FB) pin. If a current less than 49 μA flows into the FB pin when the oscillator's (internal) clock signal occurs, power MOSFET switching is enabled for that switching cycle and the power MOSFET turns on. If the current is greater than 49 μA then the power MOSFET is disabled for the current switching cycle.

The switching cycle terminates when the current through the power MOSFET reaches I_{LIMIT}, or the on-time of the power MOSFET reaches the maximum duty cycle (DC_{MAX}) limit.

At full load, few switching cycles will be skipped (disabled), resulting in a high effective switching frequency. As the load reduces, more switching cycles are skipped, which reduces the effective switching frequency. At no-load, most switching cycles are skipped, which is what makes the no-load power consumption of supplies designed around the LinkSwitch-XT2 family so low, since switching losses are the dominant loss mechanism at light loading. Additionally, since the amount of energy per switching cycle is fixed by I_{LIMIT}, the skipping of switching cycles gives the supply a flat efficiency characteristic over the load range.

4.3 Primary RCD Clamp

A low cost RCD clamp is connected across the primary winding of transformer T1. This is composed of resistors R5 and R6, capacitor C4 and diode D1. The clamp helps in dissipating the energy stored in the leakage inductance of T1.

4.4 Auxiliary Winding

The IC is self-starting, using an internal high-voltage current source to charge the BP pin capacitor (C5) when AC is first applied. During normal operation, the primary-side block is powered from an auxiliary winding on the transformer T1. Output of the auxiliary (or bias) winding is rectified using diode D2 and filtered using capacitor C7. Resistor R7 limits the current being supplied to the BP pin of the LinkSwitch-XT2 (U1/U2).

4.5 Output Rectification

Transformer T1 has two secondary windings on its core – one for each output voltage. For both secondaries, the secondary switching voltage is rectified by ultrafast diodes D3 and D4, and then filtered by very low ESR type capacitors C10, and C11. For each ultrafast diode, a snubber network is connected in parallel using resistors R9 and R10, and capacitors C8 and C9. The snubber network helps limit the peak inverse voltage spikes seen by the diode. A pre-load resistor R13 is connected on the second 16.5 V output to improve minimum load regulation performance.

4.6 Output Feedback

The first (isolated) 16.5 V_{OUT1} output is sensed through the Zener diode-optocoupler network consisting of diode VR1, resistors R11 and R12, and optocoupler U3. The current through U3, which is set by resistors R11 and R12, is fed back to U1/U2 through the FEEDBACK (FB) pin. This current should be high enough for optimal feedback sensitivity and output regulation and should be low enough to minimize no-load input power. The second (non-isolated) 16.5 V_{OUT2} output is regulated through the coupling of the two output windings.

5 PCB Layout

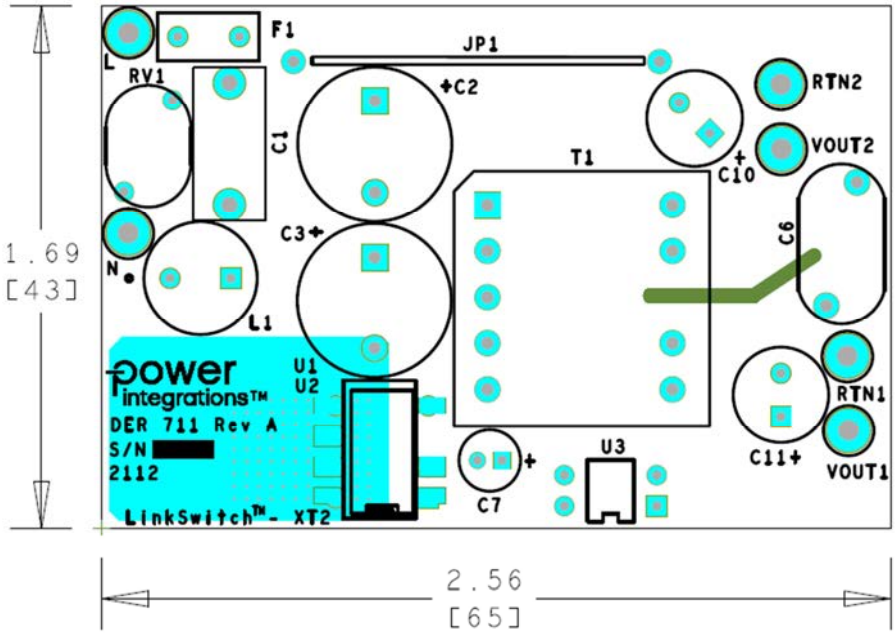


Figure 4 – Printed Circuit Layout, Top.

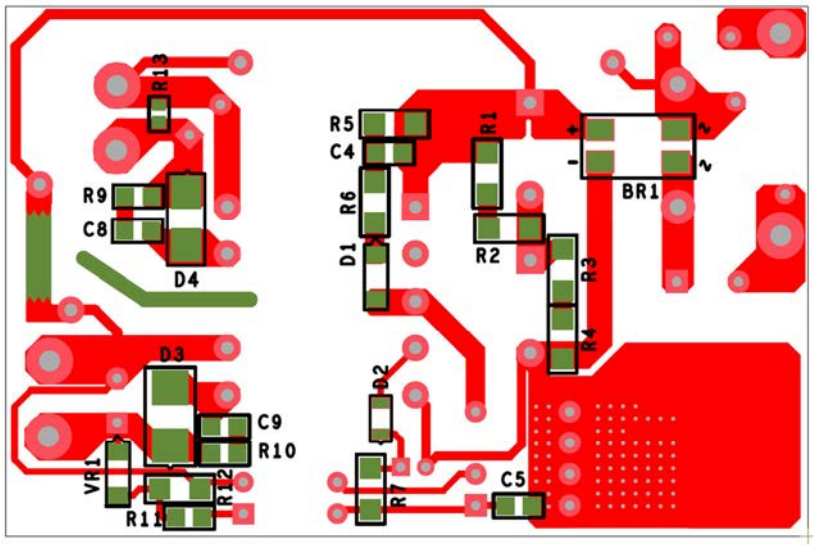


Figure 5 – Printed Circuit Layout, Bottom.

Layers:	Two (2)
Board Materials:	FR4
Board Thickness:	1.59 mm
Copper weight:	2 oz

6 Bill of Materials

Item	Qty	Ref Des	Description	Mfg Part Number	Mfg
1	1	BR1	1000 V, 0.8 A, Bridge Rectifier, SMD, MBS-1, 4-SOIC	B10S-G	Comchip
2	1	C1	10000 pF, ±20%, Film, 480 VAC 1000 VDC (1 kV), Polypropylene (PP), Metallized Radial	F339X131048MDA2B0	Vishay
3	2	C2, C3	47 µF, ±20%, 400 V, Aluminum Electrolytic, Radial, Can, 12000 Hrs @ 105°C, (12.5 x 31.5)	EKXJ401ELL470MK30S	United Chemi-Con
4	1	C4	1 nF, 250 V, Ceramic, X7R, 0805	GRM21AR72E102KW01D	Murata
5	1	C5	100 nF, 0.1 µF,10 V, Ceramic, X7R, 0805	0805ZC104MAT2A	AVX
6	1	C6	2.2 nF, Ceramic, Y1	440LD22-R	Vishay
7	1	C7	22 µF, 16 V, Electrolytic, Gen. Purpose, (5 x 11)	ECA-1CM220	Panasonic
8	2	C8, C9	1 nF, 200 V, Ceramic, X7R, 0805	08052C102KAT2A	AVX
9	2	C10, C11	330 µF, 25 V, Electrolytic, Very Low ESR, 56 mΩ, (8 x 15)	EKZE250ELL331MH15D	Nippon Chemi-Con
10	1	D1	1000 V, 1A, Standard Recovery, SOD-123FL	SM4007PL-TP	Micro Commercial
11	1	D2	100 V, 0.2 A, Fast Switching, 50 ns, SOD-323	BAV19WS-7-F	Diodes, Inc.
12	1	D3	100 V, 2 A, Ultrafast Recovery, 20 ns, DO-214AA	ES2B-E3/52T	General Semi
13	1	D4	100 V, 1 A, Ultrafast Recovery, 25 ns, DO-214AC	ES1B-13-F	Diodes, Inc.
14	1	F1	FUSE BRD MNT 6.3 A 350 VAC 72 VDC	0697H6300-02	Belfuse
15	1	L1	1000 µH, 0.510 A	RLB9012-102KL	Bourns
16	4	R1, R2, R3, R4	RES, 5.1 MΩ, 5%, 1/4 W, Thick Film, 1206	ERJ-8GEYJ515V	Panasonic
17	1	R5	RES, 200 kΩ, 5%, 1/4 W, Thick Film, 1206	ERJ-8GEYJ204V	Panasonic
18	1	R6	RES, 47 Ω, 5%, 1/4 W, Thick Film, 1206	ERJ-8GEYJ470V	Panasonic
19	1	R7	RES, 3.0 kΩ, 5%, 1/4 W, Thick Film, 1206	ERJ-8GEYJ302V	Panasonic
20	2	R9, R10	RES, 16 Ω, 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ160V	Panasonic
21	1	R11	RES, 100 Ω, 1%, 1/8 W, Thick Film, 0805	ERJ-6ENF1000V	Panasonic
22	1	R12	RES, 562 Ω, 1%, 1/4 W, Thick Film, 1206	ERJ-8ENF5620V	Panasonic
23	1	R13	RES, 6.2 kΩ, 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ622V	Panasonic
24	1	RV1	Varistor, 350 VAC, 3.5 kA, 10.5 mm, Bulk ZNR, ERZ-E, Surge Absorber	ERZ-E08A561	Panasonic
25	1	T1	Bobbin, EF20, Horizontal, 10 pins		
26	1	U1/U2	LinkSwitch-XT2 900 V	LNK3696P/G	Power Integrations
27	1	U3	Optocoupler, 35 V, CTR 80-160%, 4-DIP	LTV-817A	Liteon
28	1	VR1	DIODE ZENER 15 V 500 mW SOD123	MMSZ5245B-7-F	Diodes, Inc.

Miscellaneous Parts

Item	Qty	Ref Des	Description	Mfg Part Number	Mfg
1	1	JP1	Wire Jumper, Insulated, #24 AWG, 0.4 in	C2003A-12-02	Gen Cable
2	1	L	Test Point, BLK, THRU-HOLE MOUNT	5011	Keystone
3	1	N	Test Point, WHT, THRU-HOLE MOUNT	5012	Keystone
4	1	VOUT2	Test Point, YEL, THRU-HOLE MOUNT	5014	Keystone
5	1	RTN2	Test Point, BLU, THRU-HOLE MOUNT	5127	Keystone
6	1	VOUT1	Test Point, RED, THRU-HOLE MOUNT	5010	Keystone
7	1	RTN1	Test Point, BLK, THRU-HOLE MOUNT	5011	Keystone

7 Transformer Specification

7.1 Electrical Diagram

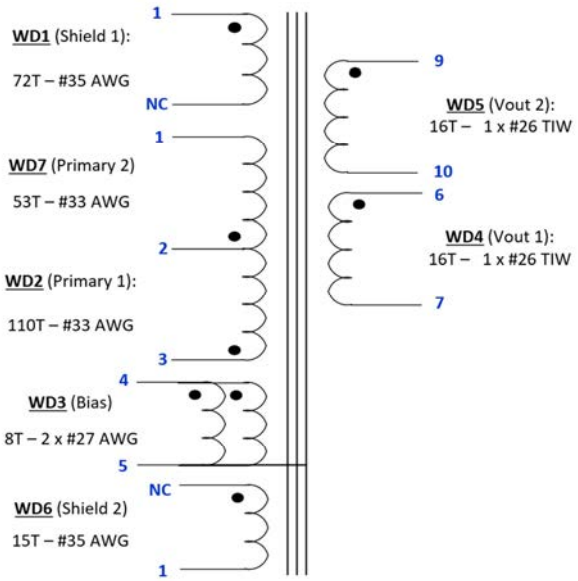


Figure 6 – Transformer Electrical Diagram.

7.2 Electrical Specifications

Parameter	Condition	Spec
Primary Inductance	Pins 1-3, all other windings open, measured at 100 kHz, 1.0 V_{RMS}.	2676 µH ±10%
Primary Leakage Inductance	Pins 1-3, all other windings short, measured at 100 kHz, 1.0 V_{RMS}.	<100 µH

7.3 Material List

Item	Description
[1]	Core: EF20, Gapped.
[2]	Bobbin: EF20, Horizontal, 10 Pins. PI #25-00834-00.
[3]	Magnet Wire: #35 AWG, Double Coated.
[4]	Magnet Wire: #33 AWG, Double Coated.
[5]	Magnet Wire: #27 AWG, Double Coated.
[6]	Magnet Wire: #26 AWG, Triple Insulated Wire.
[7]	Bus Wire: #30 AWG, Alpha Wire, Tinned Copper.
[8]	Tape, 3M 1298 Polyester Film, 2.0 Mils Thick, 12.5 mm Wide.
[9]	Tape, 3M 1298 Polyester Film, 2.0 Mils Thick, 7 mm Wide.
[10]	Tape, 3M 1298 Polyester Film, 2.0 Mils Thick, 4.5 mm Wide.
[11]	Varnish.

7.4 Transformer Build Diagram

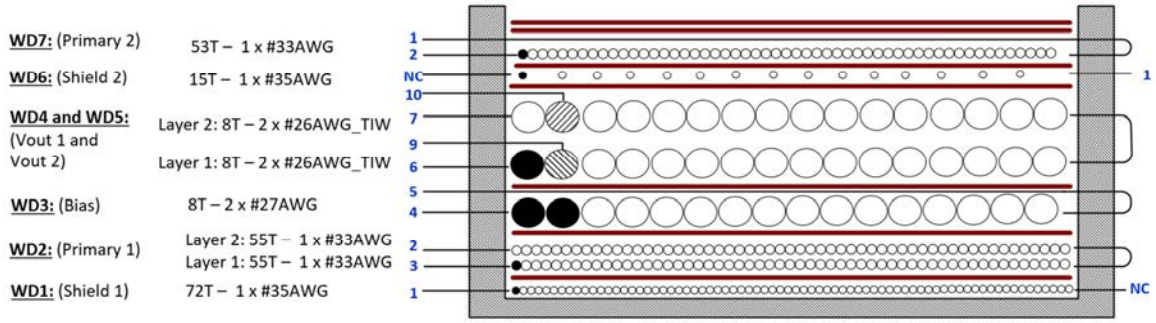
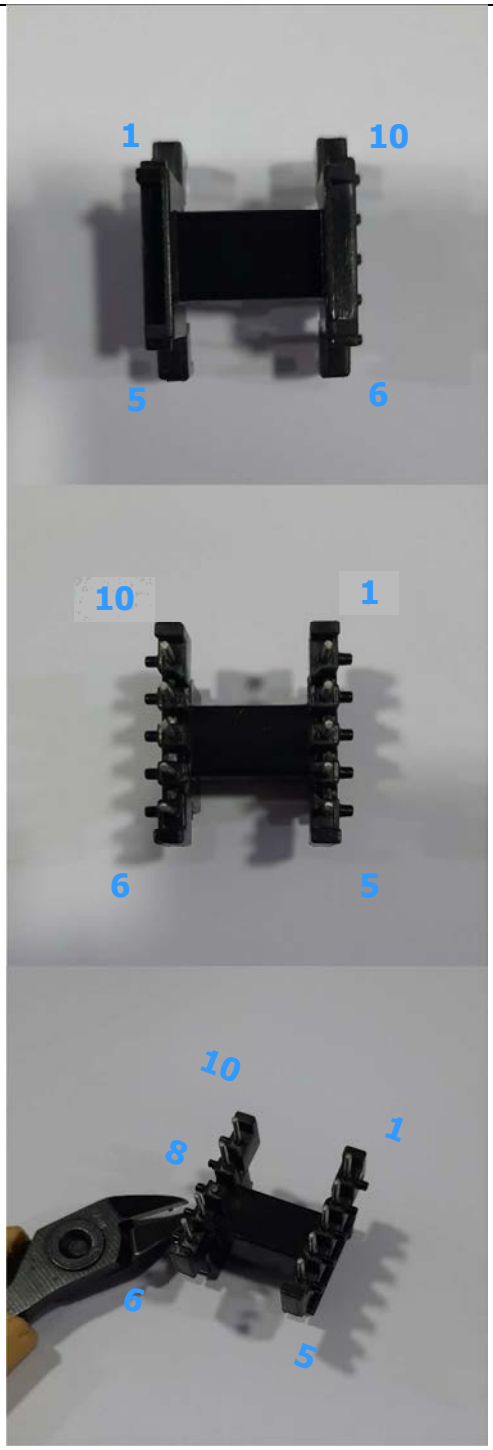


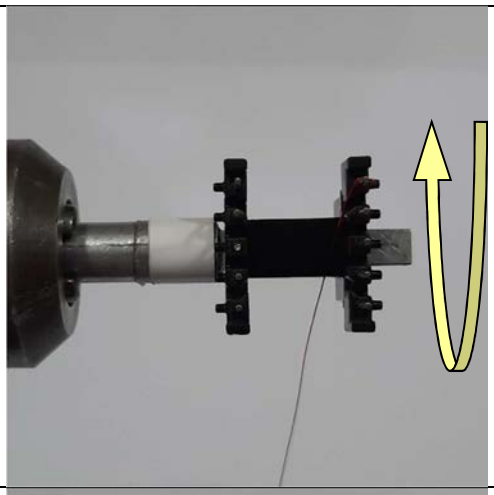
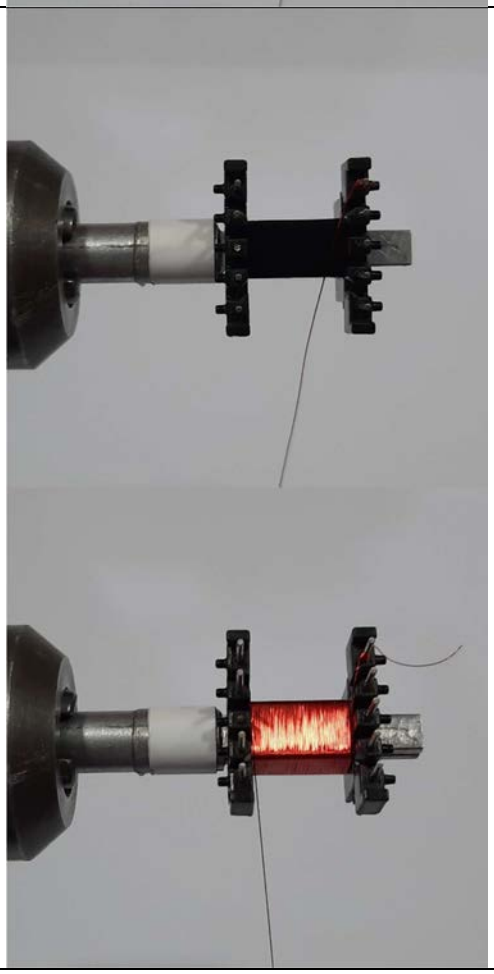
Figure 7 – Transformer Build Diagram.

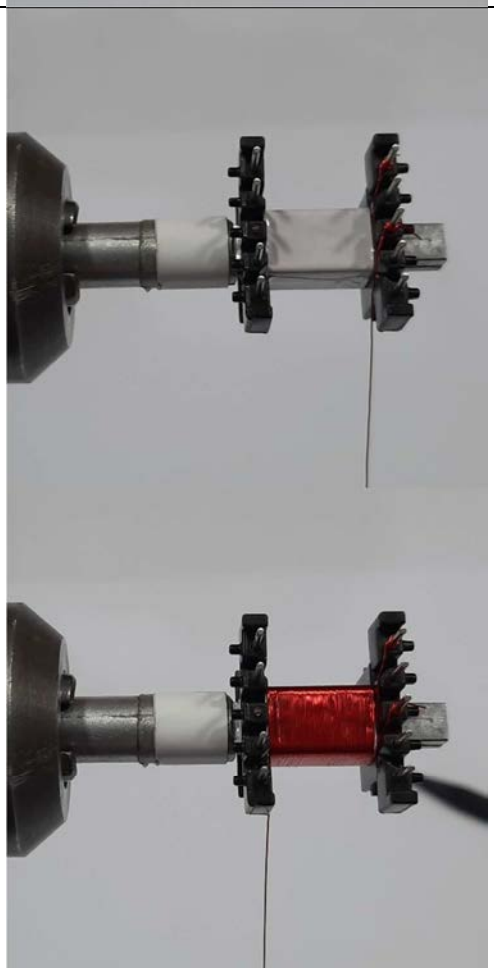
7.5 Transformer Construction

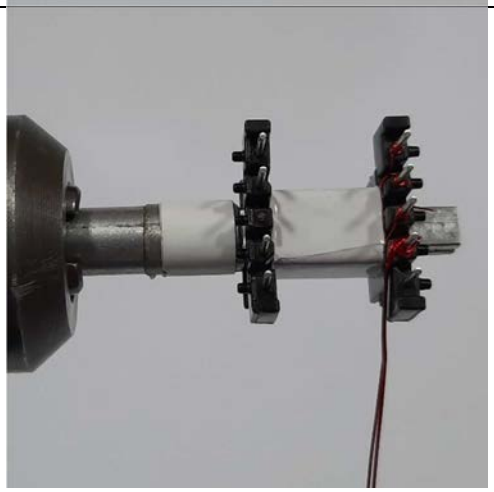
Winding Preparation	Remove pin 8 from the bobbin Item [2]. Place the bobbin Item [2] such that pins 6-10 are facing the winder. Winding direction is counter-clockwise as shown.
WD1 Shield 1	Starting at pin 1, wind 72 turns of wire Item [3] in one layer. Terminate at the end. (NC)
Insulation	Apply one layer of tape Item [8] for insulation.
WD2 Primary 1	Starting at pin 3, wind 55 turns of wire Item [4] for the first layer. Proceed to wind another 55 turns for the second layer. Terminate at pin 2.
Insulation	Apply one layer of tape Item [8] for insulation.
WD3 Bias	Start at pin 4, wind 8 bifilar turns of wire Item [5] in one layer. At the last turn, bring the wires back across the windings and terminate at pin 5.
Insulation	Apply one layer of tape Item [8] for insulation.
WD4 and WD5 V_{OUT1} and V_{OUT2}	Tie a knot at the end of one of the two wires Item [6] to indicate if it is for WD4 (starts at pin 6, is terminated at pin 7) or WD5 (starts at pin 9, is terminated at pin 10). Starting at pin 6 and pin 9, wind 8 bifilar turns of wire Item [6] in one layer. Proceed to wind another 8 bifilar turns for the second layer. For WD4, which started at pin 6, terminate at pin 7. For WD5, which started at pin 9, terminate at pin 10.
Insulation	Apply one layer of tape Item [8] for insulation.
WD6 Shield 2	Place the bobbin Item [2] such that pins 1-5 are facing the winder. Winding direction is counter-clockwise as shown. Start at pin 1, wind 15 turns of wire Item [3] in one layer. Terminate at the end (NC).
Insulation	Apply one layer of tape Item [8] for insulation.
WD7 Primary 2	Place the bobbin Item [2] such that pins 6-10 are facing the winder. Winding direction is counter-clockwise as shown. Start at pin 2, wind 53 turns of wire Item [4] in one layer. At the last turn, bring the wire back across the windings and terminate at pin 1.
Insulation	Apply two layers of tape Item [8] for insulation.
Assembly	Apply tape Item [9] on one of the core Item [1] halves (as shown) to increase creepage between the core and the secondary windings. Insert the taped core half on the secondary side as shown. Grind core halves for specified primary inductance. Solder pin 5 with bus-wire Item [7] then lean along core halves and secure with tape Item [10]. Dip varnish Item [11]. Fill in vias with solder as shown.

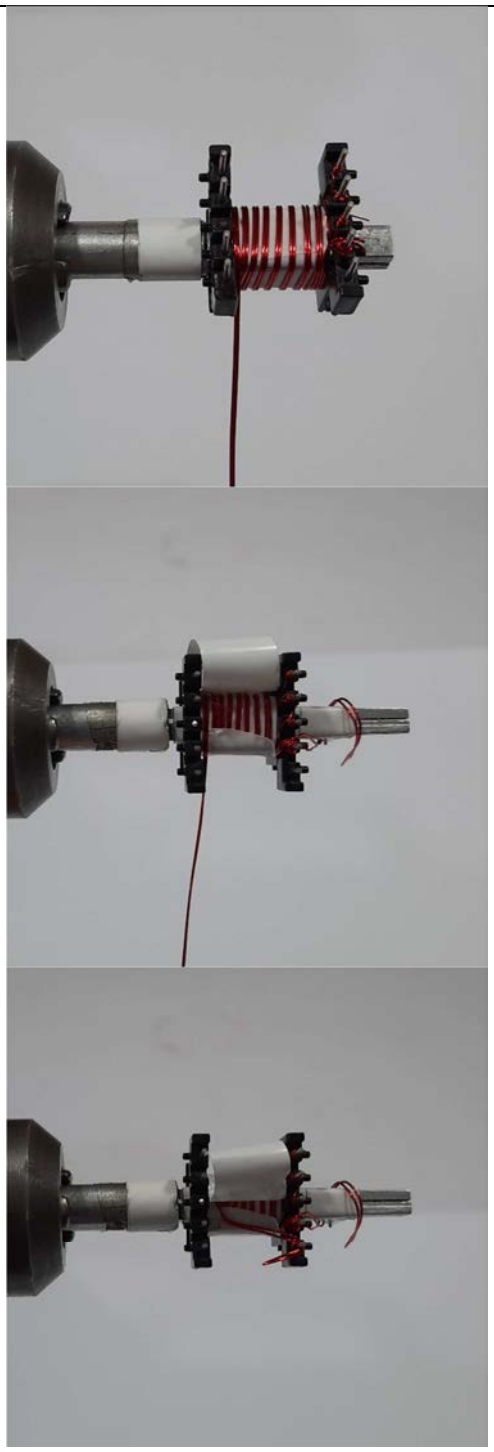
7.6 Transformer Winding Illustrations

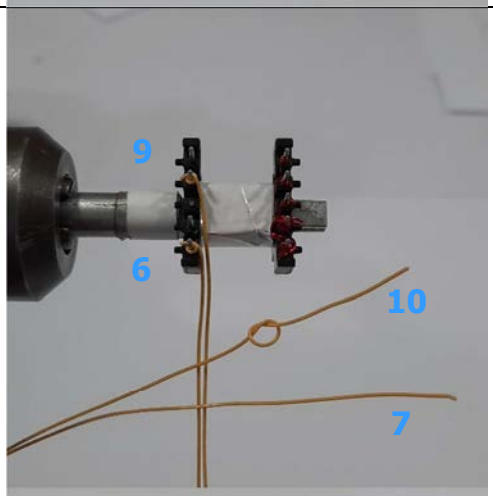
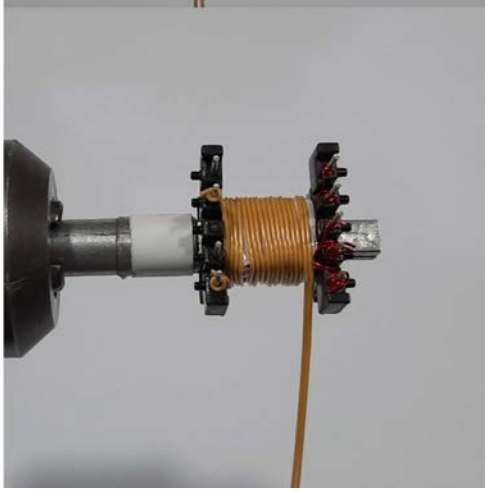
Winding Preparation		Remove pin 8 from the bobbin Item [2].

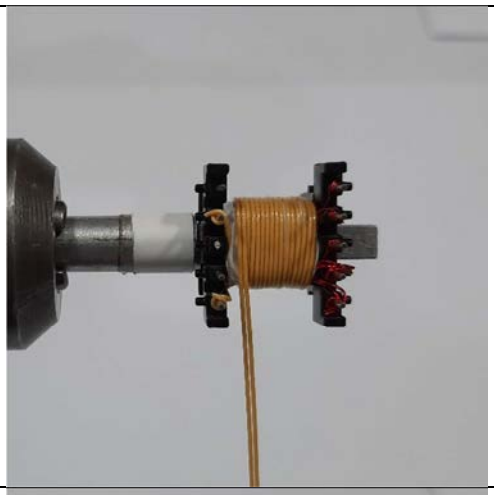
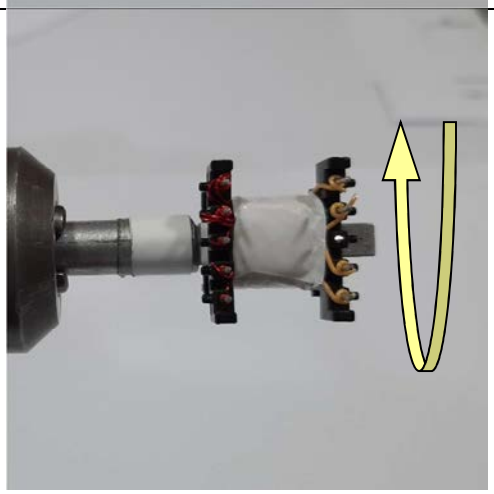
		Place the bobbin Item [2] such that pins 6-10 are facing the winder. Winding direction is counter-clockwise as shown.
WD1 **Shield 1**		Starting at pin 1, wind 72 turns of wire Item [3] in one layer. Terminate at the end. (NC)

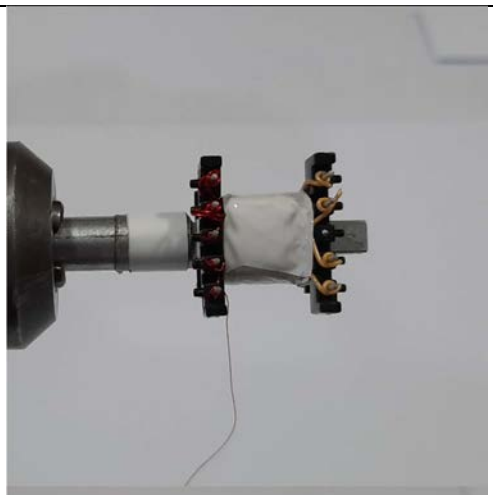
Insulation		Apply one layer of tape Item [8] for insulation.
WD2 **Primary 1**		Starting at pin 3, wind 55 turns of wire Item [4] for the first layer.

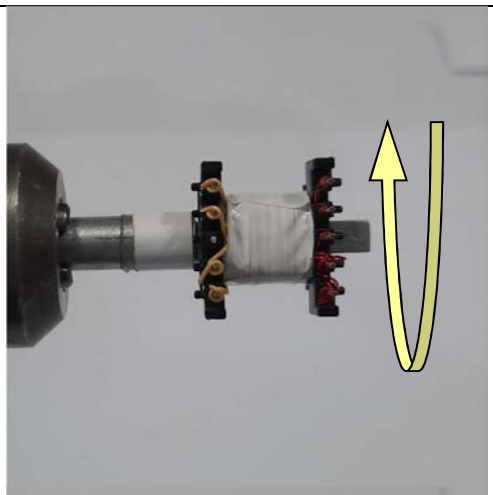
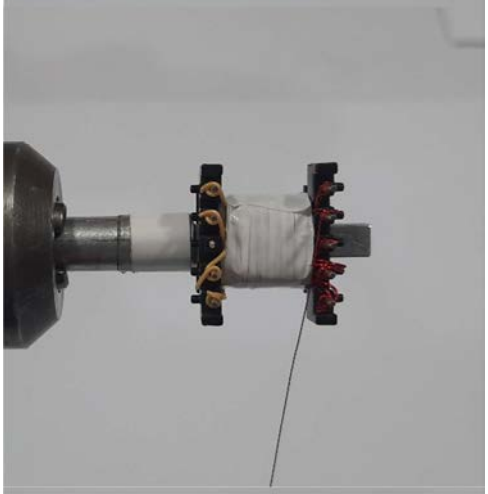
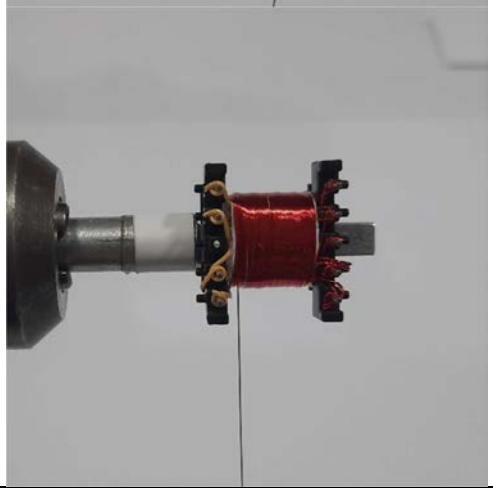
		Proceed to wind another 55 turns for the second layer. Terminate at pin 2.
Insulation		Apply one layer of tape Item [8] for insulation.
WD3 Bias		Start at pin 4, wind 8 bifilar turns of wire Item [5] in one layer.

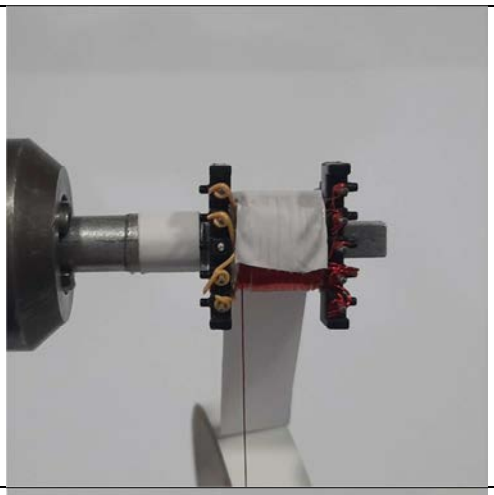
		At the last turn, bring the wires back across the windings and terminate at pin 5.

Insulation		Apply one layer of tape Item [8] for insulation.
WD4 and WD5 Vout 1 and Vout 2	 	Tie a knot at the end of one of the two wires Item [6] to indicate if it is for WD4 (starts at pin 6, is terminated at pin 7) or WD5 (starts at pin 9, is terminated at pin 10). Starting at pin 6 and pin 9, wind 8 bifilar turns of wire Item [6] in one layer.

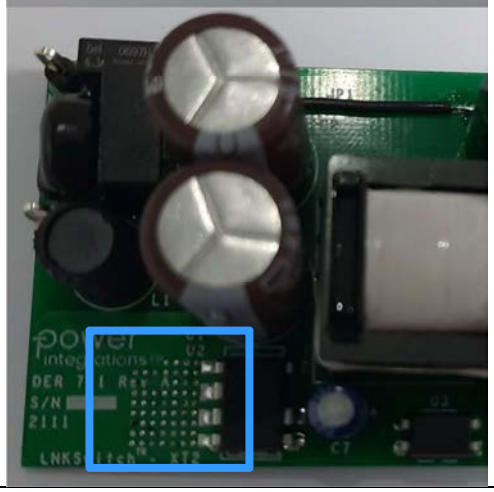
		Proceed to wind another 8 bifilar turns for the second layer. For WD4, which started at pin 6, terminate at pin 7. For WD5, which started at pin 9, terminate at pin 10.
Insulation		Apply one layer of tape Item [8] for insulation.
WD6 **Shield 2**		Place the bobbin Item [2] such that pins 1-5 are facing the winder. Winding direction is counter-clockwise as shown.

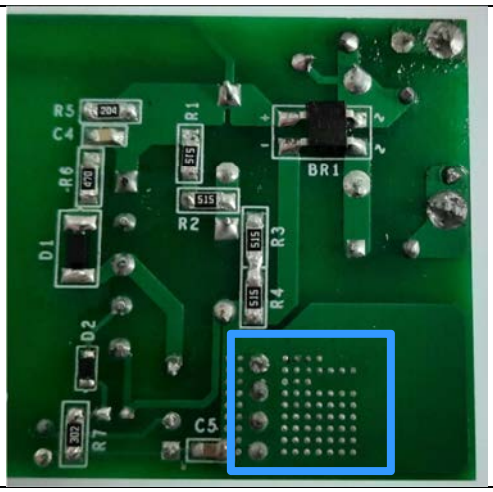
		Start at pin 1, wind 15 turns of wire Item [3] in one layer.
		Terminate at the end (NC).
Insulation		Apply one layer of tape Item [8] for insulation.

WD7 **Primary 2**		Place the bobbin Item [2] such that pins 6-10 are facing the winder. Winding direction is counter-clockwise as shown.
		Start at pin 2, wind 53 turns of wire Item [4] in one layer.
		At the last turn, bring the wire back across the windings and terminate at pin 1.

		
Insulation		Apply two layers of tape Item [8] for insulation.
Assembly		Apply tape Item [9] on one of the core Item [1] halves (as shown) to increase creepage between the core and the secondary windings.

	  	Insert the taped core half on the secondary side as shown. Solder pin 5 with bus-wire Item [7] then lean along core halves and secure with tape Item [10].

	  	Grind core halves for specified primary inductance. Dip varnish Item [11]. Fill in vias with solder as shown.

	 R5 204 C4 R1 515 R6 470 BR1 515 R2 D1 515 R3 515 R4 D2 C5 R7 300	

8 Transformer Design Spreadsheet

Note: The output current entered in the spreadsheet was increased such that POUT matches the combined power of the dual outputs.

ACDC_LinkSwitchXT2900V_092018; Rev.1.1; Copyright Power Integrations 2018	**INPUT**	**INFO**	**OUTPUT**	**UNIT**	**ACDC_LinkSwitchXT2 900V Flyback Design Spreadsheet**
ENTER APPLICATION VARIABLES					
LINE VOLTAGE RANGE			UNIVERSAL		AC line voltage range
VACMIN	85.00		85.00	Volts	Minimum AC line voltage
VACTYP	230.00		230.00	Volts	Typical AC line voltage
VACMAX	350.00		350.00	Volts	Maximum AC line voltage
fL			50	Hertz	AC mains frequency
TIME_BRIDGE_CONDUCTION			2.48	mseconds	Input bridge rectifier diode conduction time
LINE RECTIFICATION			F		Select 'F'ull wave rectification or 'H'alf wave rectification
VOUT	16.50		16.50	Volts	Output voltage
IOUT	0.400		0.400	Amperes	Average output current specification
EFFICIENCY			0.80		Efficiency Estimate at output terminals. Under 0.8 if no better data available
LOSS ALLOCATION FACTOR			0.50		The ratio of power losses during the MOSFET off-state to the total system losses
POUT			6.60	Watts	Continuous Output Power
CIN	23.50		23.50	uFarads	Input capacitor
VMIN			94.00	Volts	Valley of the rectified VACMIN
VMAX			494.97	Volts	Peak of the VACMAX
FEEDBACK	OPTO		OPTO		Select the type of feedback required. (OPTO = feedback via Optocoupler Network)
BIAS WINDING	YES		YES		Select whether a bias winding is required
LINKSWITCH-XT2 VARIABLES					
CURRENT LIMIT MODE			STD		Pick between 'RED' (Reduced) or 'STD' (Standard) current limit mode of operation
PACKAGE			DIP-8C		Device package
ENCLOSURE			OPEN FRAME		Device enclosure
GENERIC DEVICE	LNK3696		LNK3696		Device series
DEVICE CODE			LNK3696P		Device code
PMAX			8.00	Watts	Device maximum power capability
VOR	175		175	Volts	Voltage reflected to the primary winding when the MOSFET is off
VDSON			10.0	Volts	MOSFET on-time drain to source peak voltage
VDSOFF			757.5	Volts	Estimated MOSFET drain-to-source voltage during Off-time
ILIMITMIN			0.446	Amperes	Minimum current limit
ILIMITTYP			0.482	Amperes	Typical current limit
ILIMITMAX			0.518	Amperes	Maximum current limit
FSMIN			62000	Hertz	Minimum switching frequency
FSTYP			66000	Hertz	Typical switching frequency
FSMAX			70000	Hertz	Maximum switching frequency
RDSON			9.70	Ohms	MOSFET drain to source resistance at 25degC
PRIMARY WAVEFORM PARAMETERS					
MODE OF OPERATION			DCM		Mode of operation
KRP/KDP			2.647		Measure of continuous/discontinuous mode of operation
KP_TRANSIENT			1.403		KP under conditions of a transient
DMAX			0.440		Maximum duty cycle at VMIN

TIME_ON			7.103	useconds	MOSFET conduction time at the minimum line voltage
TIME_ON_MIN			1.216	useconds	MOSFET conduction time at the maximum line voltage
IAVG_PRIMARY			0.098	Amperes	Average input current
IRMS_PRIMARY			0.171	Amperes	Root mean squared value of the primary current
LPRIMARY_MIN			1204	uH	Minimum primary inductance
LPRIMARY_TYP			1338	uH	Typical primary inductance
LPRIMARY_MAX			1472	uH	Maximum primary inductance
LPRIMARY_TOL			10		Tolerance of the Primary inductance
SECONDARY WAVEFORM PARAMETERS					
IPEAK_SECONDARY			5.277	Amperes	Peak secondary current
IRMS_SECONDARY			1.401	Amperes	Root mean squared value of the secondary current
PIV_SECONDARY			65.09	Volts	Peak inverse voltage on the secondary diode, not including the leakage spike
VF_SECONDARY			0.70	Volts	Secondary diode forward voltage drop
TRANSFORMER CONSTRUCTION PARAMETERS					
Core selection					
CORE	Custom		Custom		Select the transformer core
BOBBIN	EF20		EF20		Bobbin name
AE	32.10		32.10	mm^2	Cross sectional area of the core
LE	46.30		46.30	mm	Effective magnetic path length of the core
AL	1470.0		1470.0	nH/(turns^2)	Ungapped effective inductance of the core
VE	1490.0		1490.0	mm^3	Volume of the core
AW	41.82		41.82	mm^2	Window area of the bobbin
BW	12.30		12.30	mm	Width of the bobbin
MLT	0.00		0.00	mm	Mean length per turn of the bobbin
MARGIN	0.00		0.00	mm	Safety margin
Primary winding					
NPRIMARY			163		PrImary number of turns
BMAX_TARGET			1500	Gauss	Target value of the magnetic flux density
BMAX_ACTUAL			1325	Gauss	Actual value of the magnetic flux density
BAC			662	Gauss	AC flux density
ALG			50	nH/T^2	Gapped core effective inductance
LG			0.774	mm	Core gap length
LAYERS_PRIMARY	3		3		Number of primary layers
AWG_PRIMARY			33		Primary winding wire AWG
OD_PRIMARY_INSULATED			0.219	mm	Primary winding wire outer diameter with insulation
OD_PRIMARY_BARE			0.180	mm	Primary winding wire outer diameter without insulation
CMA_PRIMARY			293	mil^2/Amperes	Primary winding wire CMA
Secondary winding					
NSECONDARY	16		16		Secondary turns
AWG_SECONDARY			25		Secondary winding wire AWG
OD_SECONDARY_INSULATED			0.760	mm	Secondary winding wire outer diameter with insulation
OD_SECONDARY_BARE			0.455	mm	Secondary winding wire outer diameter without insulation
CMA_SECONDARY			229	mil^2/Amperes	Secondary winding CMA
Bias winding					
NBIAS	8		8		Bias turns
VF_BIAS			0.70	Volts	Bias diode forward voltage drop
VBIAS		Warning	8.60	Volts	Increase the bias winding turns to ensure VBIAS > 12V
PIVB			32.89	Volts	Peak inverse voltage on the bias diode

CBP			0.1	uF	BP pin capacitor
FEEDBACK PARAMETERS					
DIODE_BIAS			1N4003-4007		Recommended diode is 1N4003. Place diode on return leg of bias winding for optimal EMI
RUPPER			500 - 1000	ohms	CV bias resistor for CV/CC circuit. See LinkSwitch-XT2 Design Guide
RLOWER			200 - 820	ohms	Resistor to set CC linearity for CV/CC circuit. See LinkSwitch-XT2 900V Design Guide
MULTIPLE OUTPUT PARAMETERS					
Output 1					
VOUT1			16.50	Volts	Output Voltage 1
IOUT1	0.300		0.300	Amperes	Output Current 1
POUT1			4.95	Watts	Output Power 1
VD1			0.70	Volts	Secondary diode forward voltage drop for output 1
NS1			16		Number of turns for output 1
ISRMS1			1.051	Amperes	Root mean squared value of the secondary current for output 1
IRIPPLE1			1.007	Amperes	Current ripple on the secondary waveform for output 1
PIV1			65.09	Volts	Peak inverse voltage on the secondary diode for output 1
DIODE1_RECOMMENDED			SB1100		Recommended diode for output 1
PRELOAD			N/A	kohms	Preload resistor to ensure a load of at least 3mA on the first output for BIAS, 2mA for MAIN
CMS1			210.1	Cmils	Bare conductor effective area in circular mils for output 1
AWGS1			26	AWG	Wire size for output 1
Output 2					
VOUT2	16.50		16.50	Volts	Output Voltage 2
IOUT2	0.100		0.100	Amperes	Output Current 2
POUT2			1.65	Watts	Output Power 2
VD2			0.70	Volts	Secondary diode forward voltage drop for output 2
NS2			16		Number of turns for output 2
ISRMS2			0.350	Amperes	Root mean squared value of the secondary current for output 2
IRIPPLE2			0.336	Amperes	Current ripple on the secondary waveform for output 2
PIV2			65.09	Volts	Peak inverse voltage on the secondary diode for output 2
DIODE2_RECOMMENDED			SB1100		Recommended diode for output 2
CMS2			70.0	Cmils	Bare conductor effective area in circular mils for output 2
AWGS2			31	AWG	Wire size for output 2
Output 3					
VOUT3			0.00	Volts	Output Voltage 3
IOUT3			0.000	Amperes	Output Current 3
POUT3			0.00	Watts	Output Power 3
VD3			0.70	Volts	Secondary diode forward voltage drop for output 3
NS3			1		Number of turns for output 3
ISRMS3			0.000	Amperes	Root mean squared value of the secondary current for output 3
IRIPPLE3			0.000	Amperes	Current ripple on the secondary waveform for output 3
PIV3			3.04	Volts	Peak inverse voltage on the secondary diode for output 3
DIODE3_RECOMMENDED			NA		Recommended diode for output 3

CMS3			0.0	Cmils	Bare conductor effective area in circular mils for output 3
AWGS3			0	AWG	Wire size output for 3
PO_TOTAL			6.60	Watts	Total power of all outputs
NEGATIVE OUTPUT			N/A		If negative output exists, enter the output number; e.g. If VO2 is negative output, select 2

Note:

For the intended application, the typical primary inductance was doubled.

Calculations:

LPRIMARY_TYP (original) = 1338 uH
LPRIMARY_TYP (new) = 2676 uH

BMAX_ACTUAL (original) = 1325 Gauss
BMAX_ACTUAL (new) = (LPRIMARY_TYP) (ILIM) / (NPRIMARY) (AE)
= (2676 uH) (518.15 mA) / (163 T) (32.1 mm^2) = 2650 Gauss (< 3000 G)

The VBIAS field has a "Warning" because the actual bias voltage is only 8V which is lower than the recommended 12V. This was chosen for improved efficiency and no-load performance.

9 Performance Data

9.1 No-Load Input Power

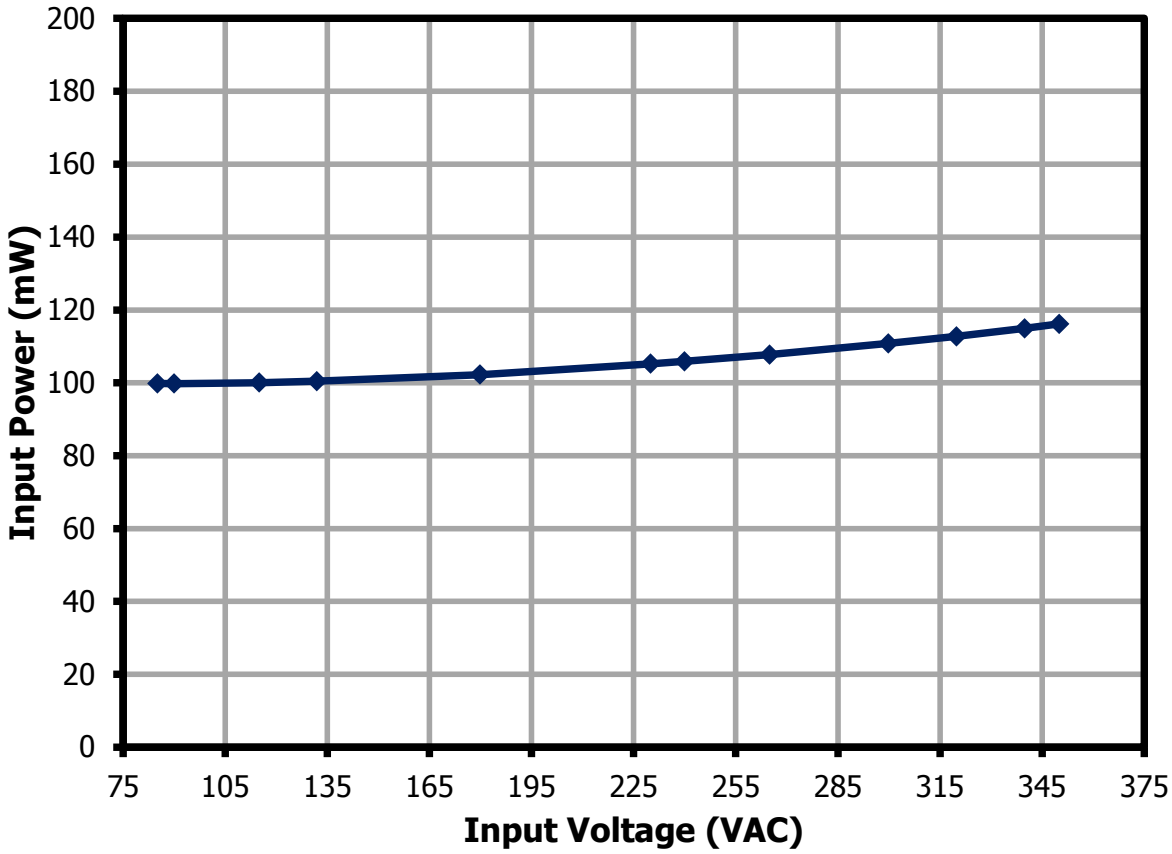


Figure 8 – No-Load Power vs. Input Line Voltage.

9.2 **Efficiency**

9.2.1 *Efficiency vs Line*

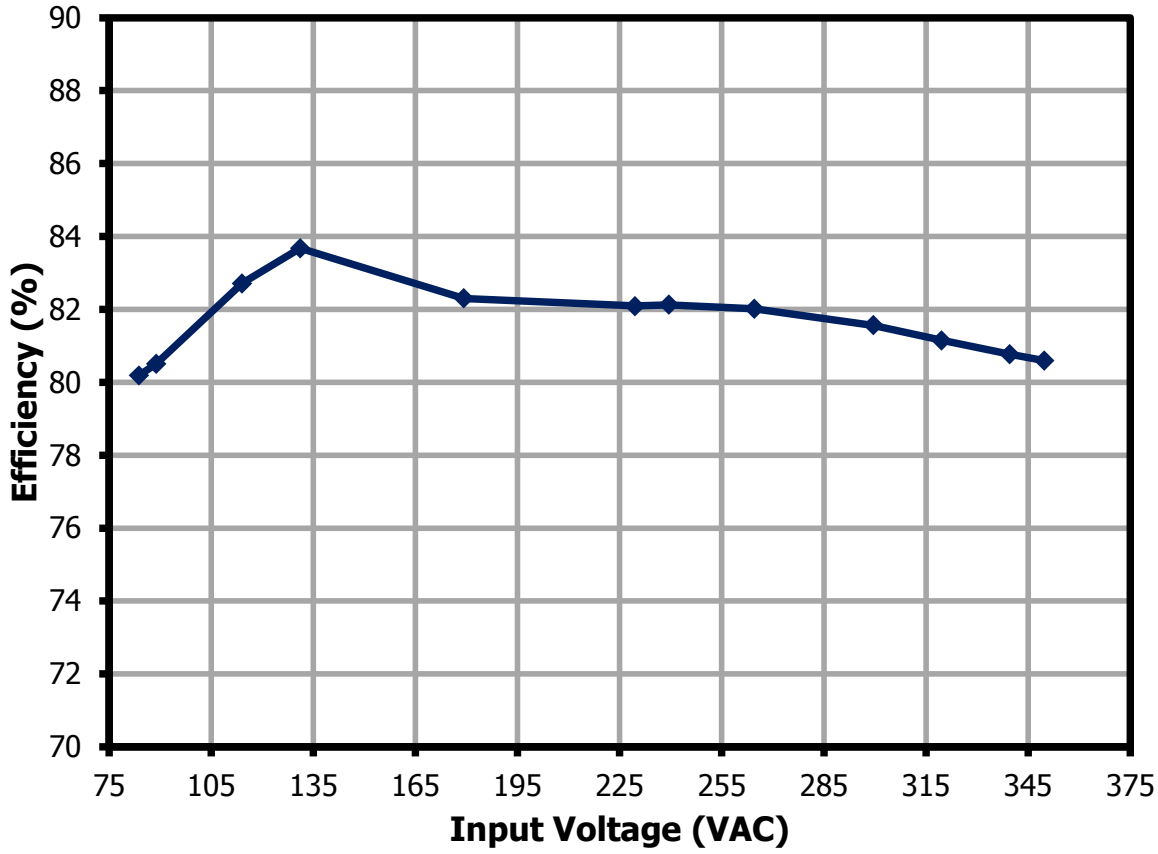


Figure 9 – Full Load Efficiency vs. Input Line Voltage.

9.2.2 *Efficiency vs Load*

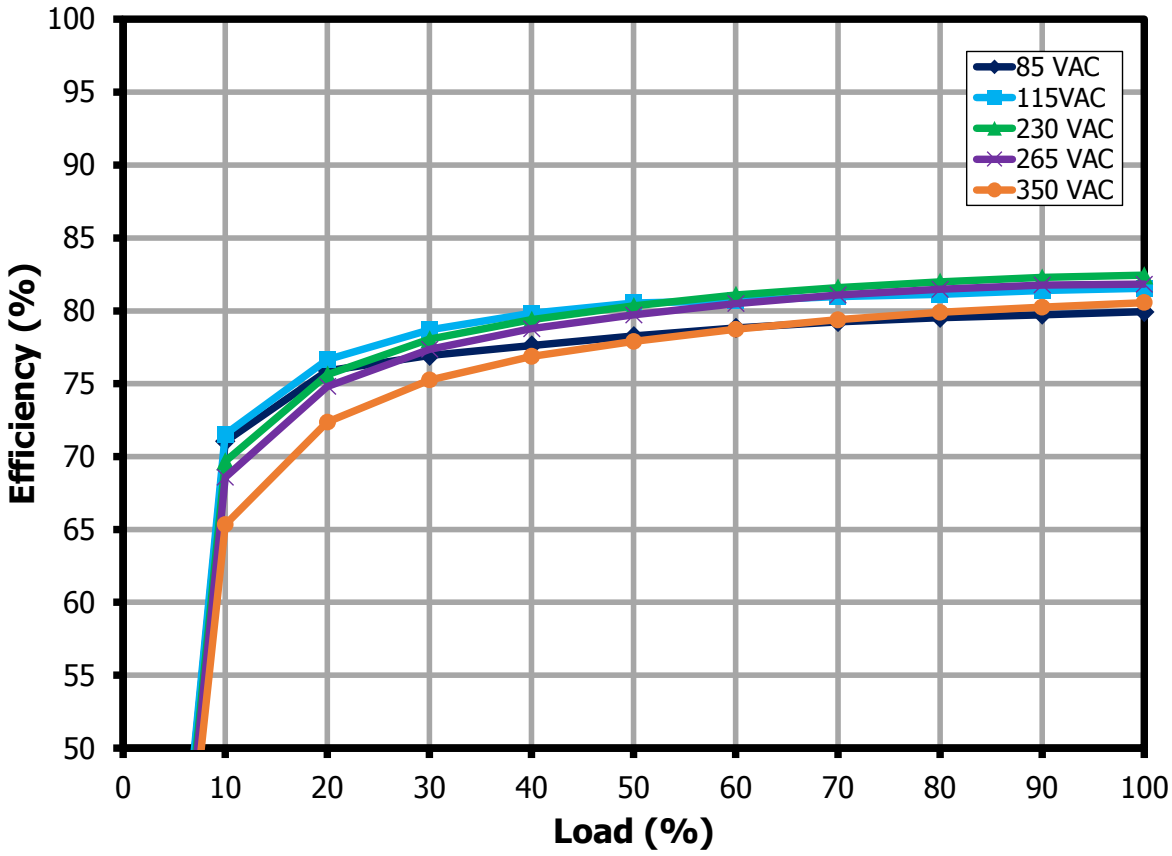


Figure 10 – Efficiency vs. Percent Load, at Different Input Line Voltages.

9.2.3 *Average Efficiency*

9.2.3.1 85 VAC Input

Input Measurement			Output 1 Measurement			Output 2 Measurement			Efficiency (%)
V_{IN} (RMS)	I_{IN} (mA)	P_{IN} (W)	V_{OUT} (V)	I_{OUT} (mA)	P_{OUT} (W)	V_{OUT} (V)	I_{OUT} (mA)	P_{OUT} (W)	
83.75	143.54	8.05	16.10	299.74	4.82	16.35	99.87	1.63	80.20
84.03	111.06	6.09	16.09	224.79	3.62	16.36	74.89	1.22	79.51
84.33	77.82	4.12	16.09	149.86	2.41	16.35	49.88	0.82	78.38
84.65	42.32	2.09	16.07	74.89	1.20	16.32	24.91	0.41	76.88
						Average Efficiency			**78.74**

9.2.3.2 115 VAC Input

Input Measurement			Output 1 Measurement			Output 2 Measurement			Efficiency (%)
V_{IN} (RMS)	I_{IN} (mA)	P_{IN} (W)	V_{OUT} (V)	I_{OUT} (mA)	P_{OUT} (W)	V_{OUT} (V)	I_{OUT} (mA)	P_{OUT} (W)	
114.02	108.76	7.80	16.10	299.69	4.82	16.35	99.88	1.63	82.75
114.23	84.49	5.90	16.09	224.74	3.62	16.35	74.89	1.22	82.04
114.46	59.60	4.00	16.08	149.86	2.41	16.34	49.88	0.81	80.55
114.69	33.14	2.08	16.07	74.89	1.20	16.31	24.90	0.41	77.50
						Average Efficiency			**80.71**

9.2.3.3 230 VAC Input

Input Measurement			Output 1 Measurement			Output 2 Measurement			Efficiency (%)
V_{IN} (RMS)	I_{IN} (mA)	P_{IN} (W)	V_{OUT} (V)	I_{OUT} (mA)	P_{OUT} (W)	V_{OUT} (V)	I_{OUT} (mA)	P_{OUT} (W)	
229.48	64.72	7.86	16.10	299.65	4.82	16.36	99.87	1.63	82.13
229.60	50.38	5.94	16.09	224.72	3.62	16.35	74.89	1.22	81.51
229.71	35.73	4.04	16.09	149.73	2.41	16.35	49.88	0.82	79.82
229.83	20.00	2.11	16.08	74.90	1.20	16.32	24.90	0.41	76.44
						Average Efficiency			**79.98**

9.2.3.4 265 VAC Input

Input Measurement			Output 1 Measurement			Output 2 Measurement			Efficiency (%)
V_{IN} (RMS)	I_{IN} (mA)	P_{IN} (W)	V_{OUT} (V)	I_{OUT} (mA)	P_{OUT} (W)	V_{OUT} (V)	I_{OUT} (mA)	P_{OUT} (W)	
264.46	58.04	7.88	16.10	299.69	4.83	16.36	99.87	1.63	82.01
264.56	45.44	5.99	16.10	224.74	3.62	16.36	74.89	1.23	80.91
264.66	32.25	4.07	16.09	149.75	2.41	16.36	49.88	0.82	79.19
264.76	18.08	2.13	16.08	74.90	1.20	16.33	24.90	0.41	75.71
						Average Efficiency			**79.46**

9.2.3.5 350 VAC Input

Input Measurement			Output 1 Measurement			Output 2 Measurement			Efficiency (%)
V_{IN} (RMS)	I_{IN} (mA)	P_{IN} (W)	V_{OUT} (V)	I_{OUT} (mA)	P_{OUT} (W)	V_{OUT} (V)	I_{OUT} (mA)	P_{OUT} (W)	
349.67	47.57	8.04	16.12	299.70	4.83	16.38	99.88	1.64	80.42
349.74	37.41	6.14	16.11	224.73	3.62	16.38	74.89	1.23	78.97
349.82	26.57	4.18	16.10	149.74	2.41	16.37	49.88	0.82	77.16
349.90	14.94	2.20	16.09	74.89	1.21	16.35	24.90	0.41	73.34
						Average Efficiency			**77.47**

9.3 Output Voltage Regulation

9.3.1 *16.5 V_{OUT1} Load Regulation with Balanced Load*

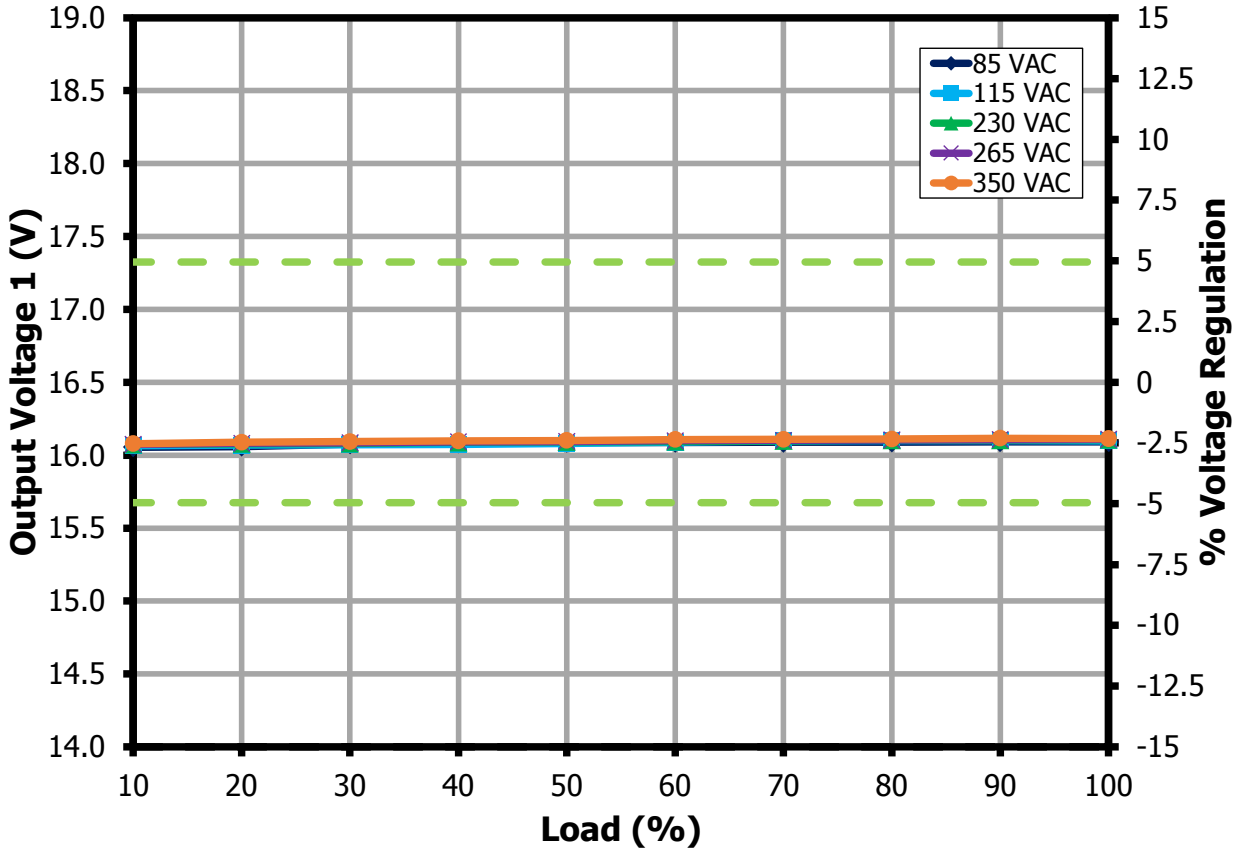


Figure 11 – 16.5 V_{OUT1} Load Regulation.
Condition: Simultaneous Load Decrement.

9.3.2 *16.5 V_{OUT2} Load Regulation with Balanced Load*

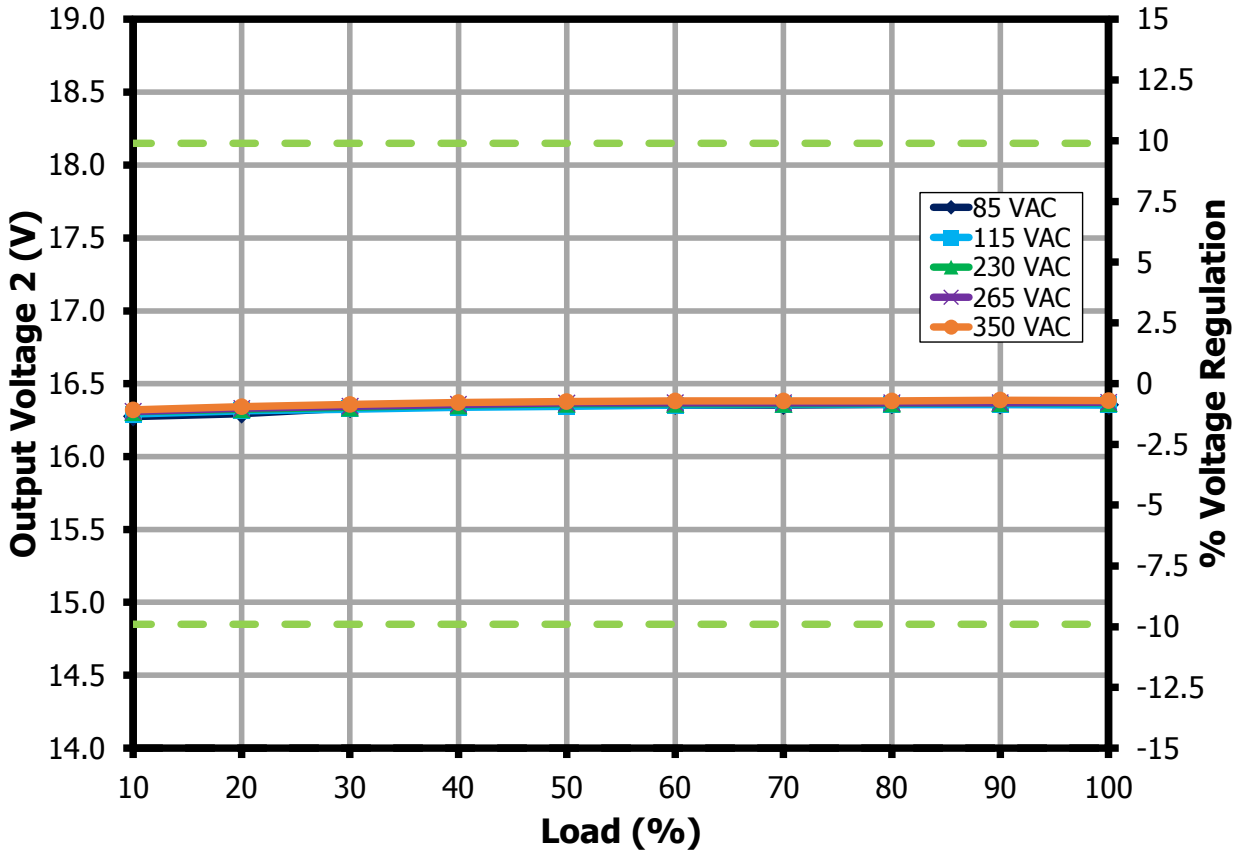


Figure 12 – 16.5 V_{OUT2} Load Regulation.
Condition: Simultaneous Load Decrement.

9.3.3 *16.5 V_{OUT1} Load Regulation with Unbalanced Load*

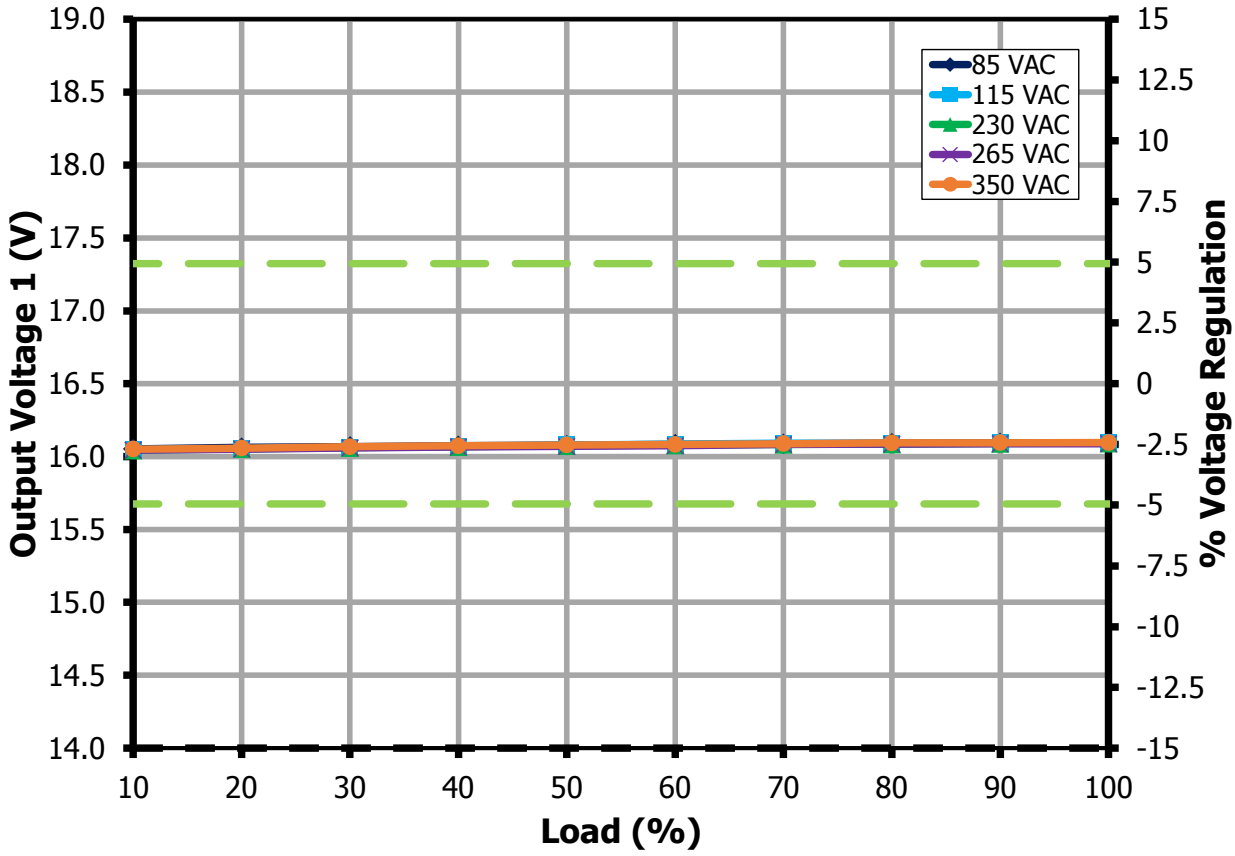


Figure 13 – 16.5 V_{OUT1} Load Regulation.
Condition: 16.5 V_{OUT2} at 100 mA, 16.5 V_{OUT1} Load Sweep.

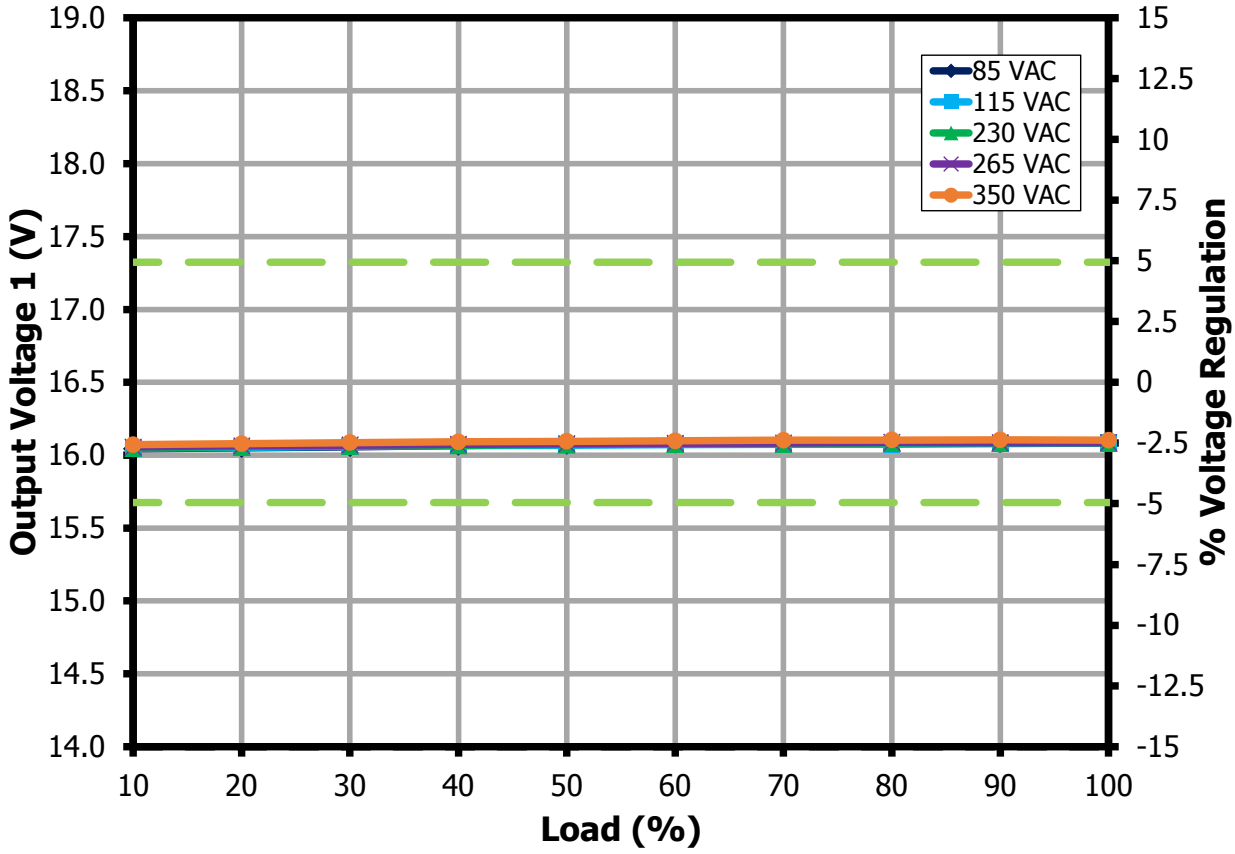


Figure 14 – 16.5 V_{OUT1} Load Regulation.
Condition: 16.5 V_{OUT2} at 10 mA, 16.5 V_{OUT1} Load Sweep.

9.3.4 *16.5 V_{OUT2} Load Regulation with Unbalanced Load*

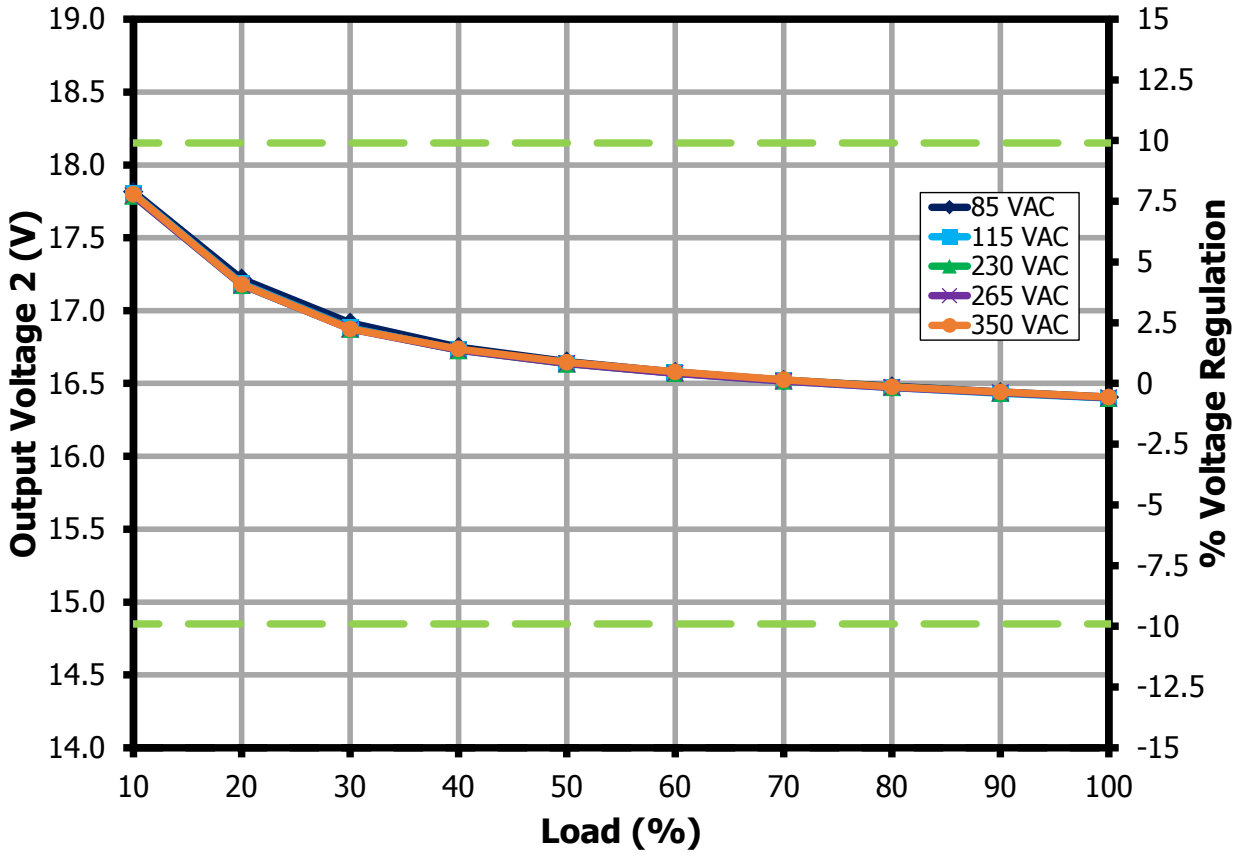


Figure 15 – 16.5 V_{OUT2} Load Regulation.
Condition: 16.5 V_{OUT1} at 300 mA, 16.5 V_{OUT2} Load Sweep.

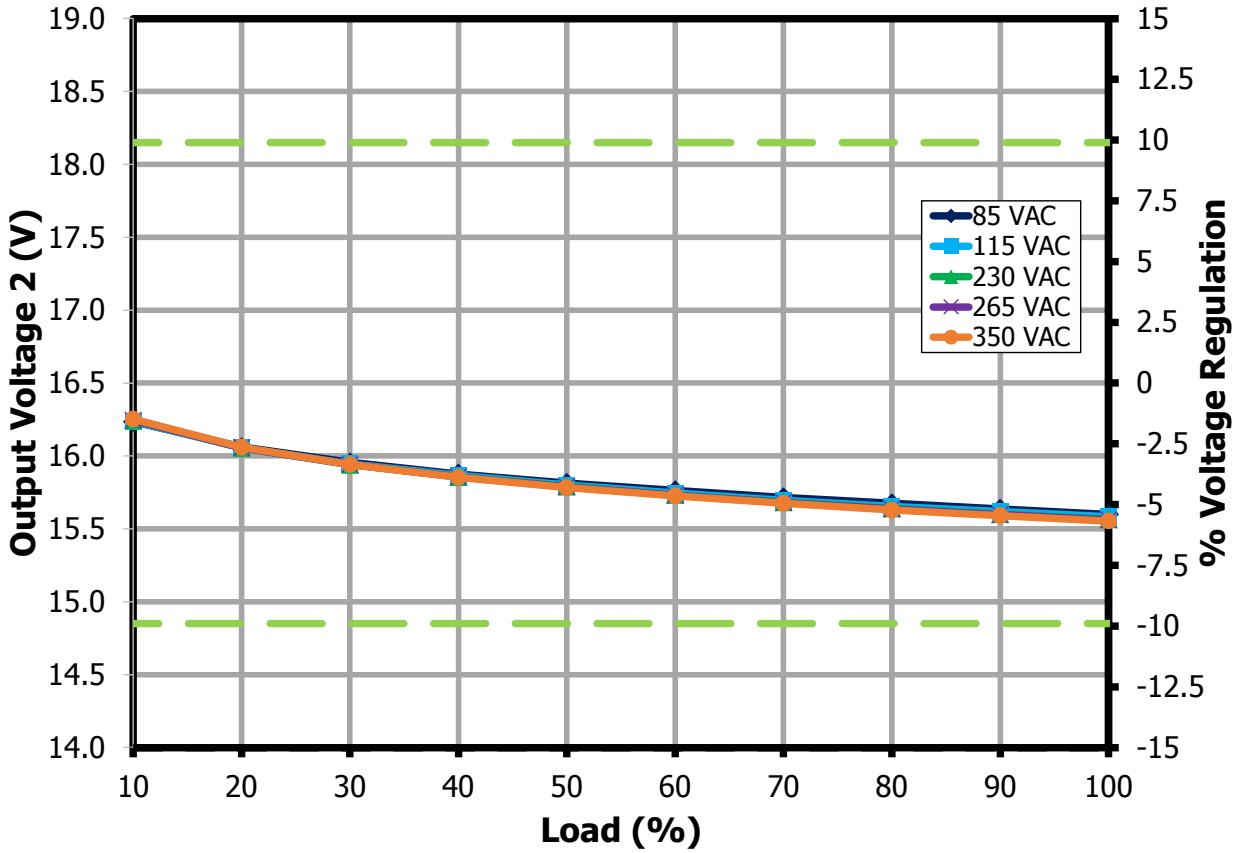


Figure 16 – 16.5 V_{OUT2} Load Regulation.
Condition: 16.5 V_{OUT1} at 30 mA, 16.5 V_{OUT2} Load Sweep.

9.3.5 *Line Regulation*

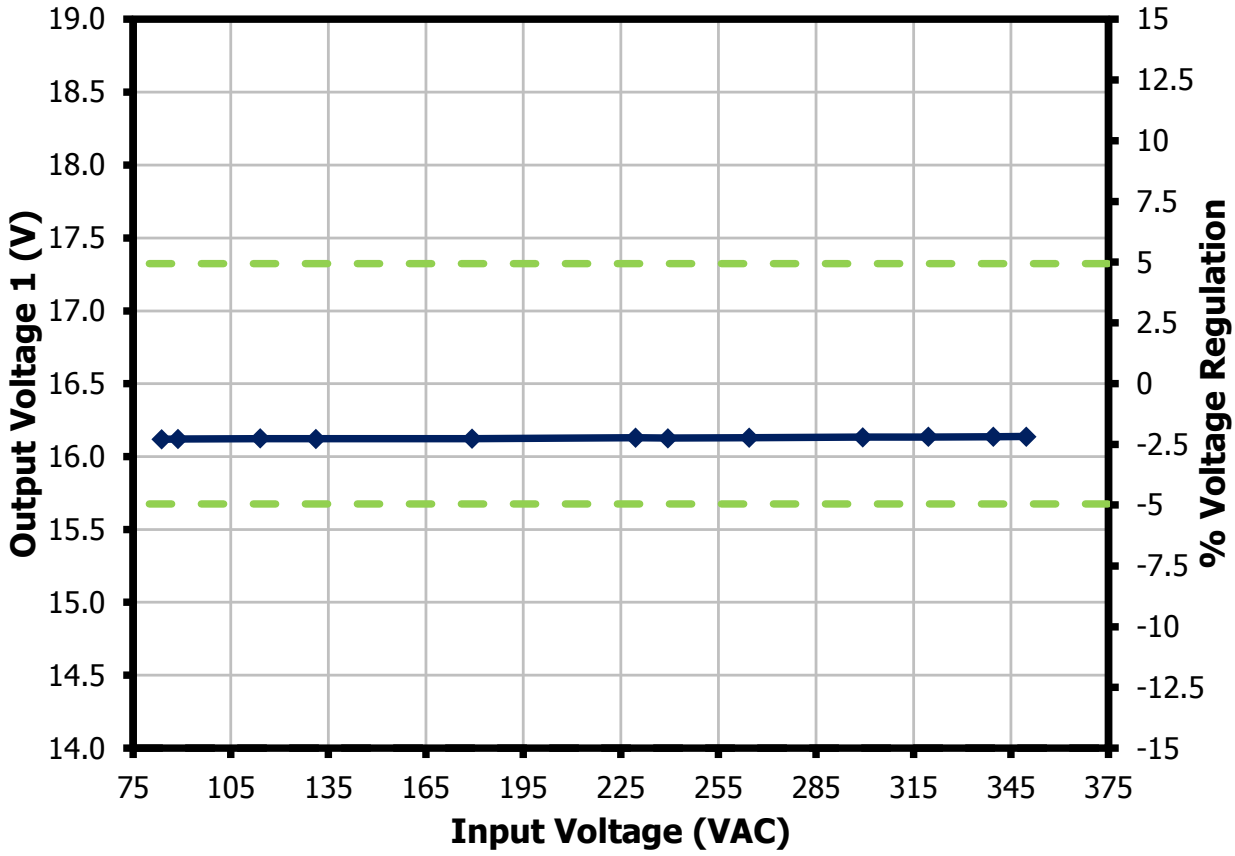


Figure 17 – 16.5 V_{OUT1} Output Regulation vs. Input Line Voltage.

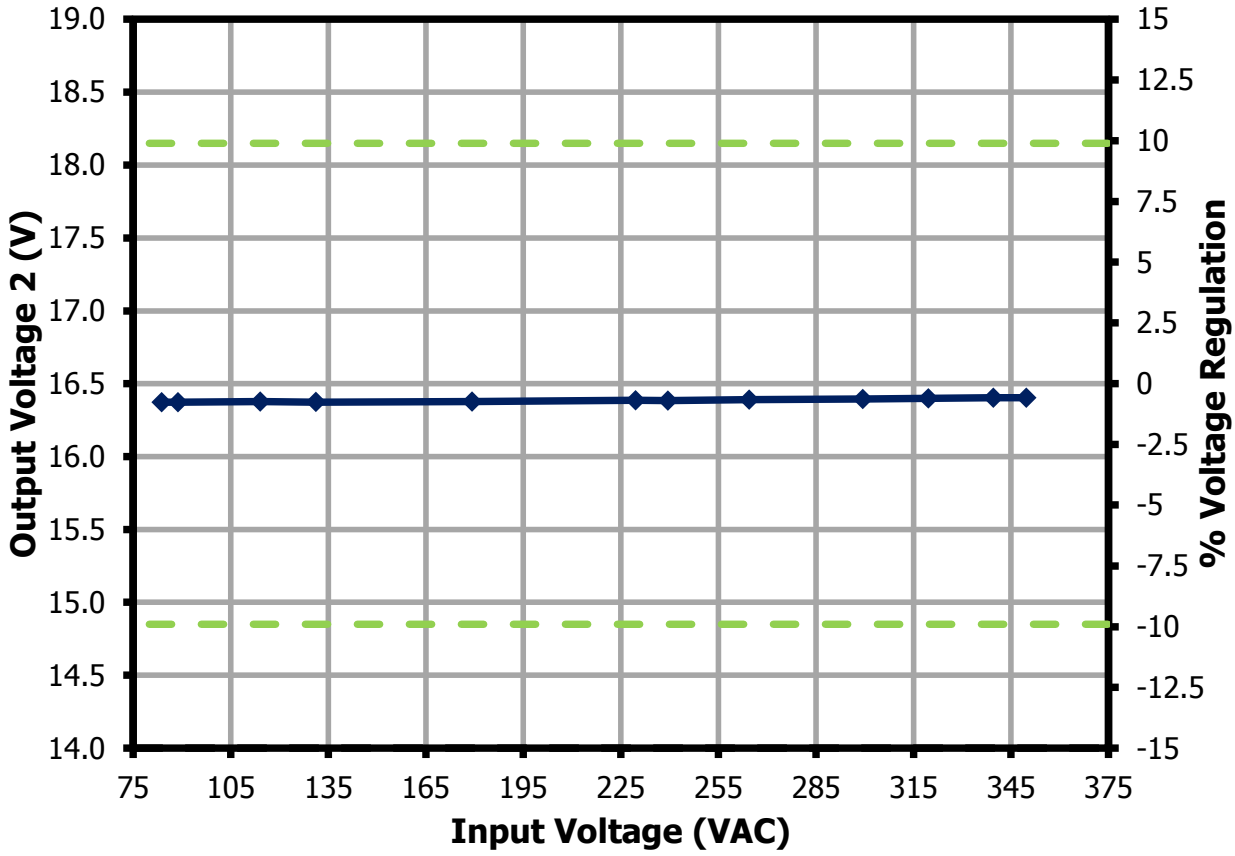


Figure 18 – 16.5 V_{OUT2} Output Regulation vs. Input Line Voltage.

10 Waveforms

10.1 Output Voltage Ripple

10.1.1 *Ripple Measurement Technique*

For DC output ripple measurements, a modified oscilloscope test probe must be utilized to reduce spurious signals due to pick-up. Details of the probe modification are provided in the Figures below.

The 4987BA probe adapter is affixed with two capacitors tied in parallel across the probe tip. The capacitors include one (1) 0.1 μF / 50 V ceramic type and one (1) 47 μF / 50 V aluminum electrolytic. The aluminum electrolytic type capacitor is polarized, so proper polarity across DC outputs must be maintained (see below). Ripple measurement was done at the end of the PCB.

Figure 19 – Oscilloscope Probe Prepared for Ripple Measurement. (End Cap and Ground Lead Removed.)

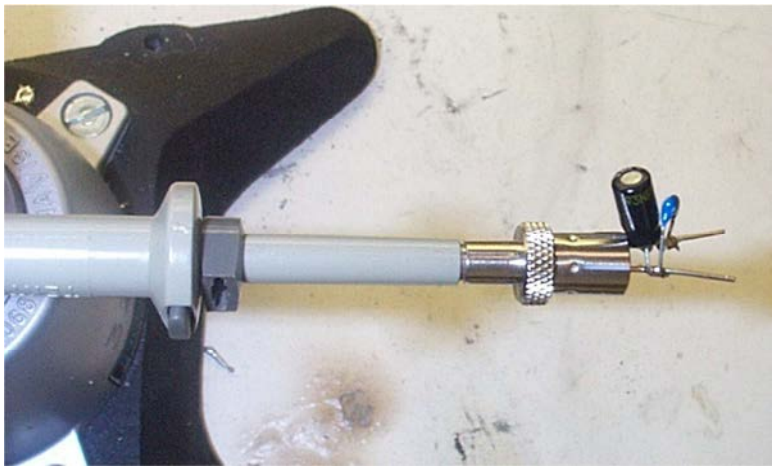


Figure 20 – Oscilloscope Probe with Probe Master (www.probemaster.com) 4987A BNC Adapter. (Modified with wires for ripple measurement, and two parallel decoupling capacitors added.)

10.1.2 *Ripple Waveforms at Full Load*

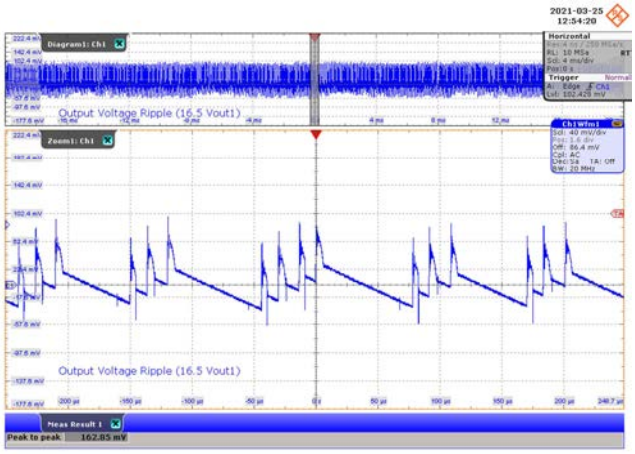


Figure 21 – 85 VAC Input.
Vertical: 40 mV / div.
Horizontal: 4 ms / div., 50 µs / div.
16.5 V_{OUT1} Ripple: 162.85 $mV_{PK-PK.}$

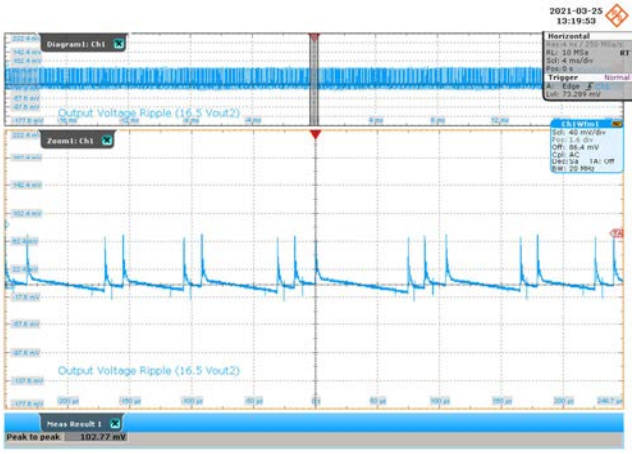


Figure 22 – 85 VAC Input.
Vertical: 40 mV / div.
Horizontal: 4 ms / div., 50 µs / div.
16.5 V_{OUT2} Ripple: 102.77 $mV_{PK-PK.}$

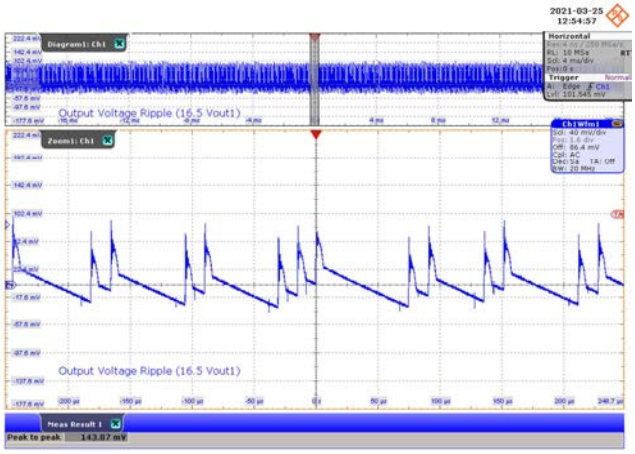


Figure 23 – 115 VAC Input.
Vertical: 40 mV / div.
Horizontal: 4 ms / div., 50 µs / div.
16.5 V_{OUT1} Ripple: 143.87 $mV_{PK-PK.}$

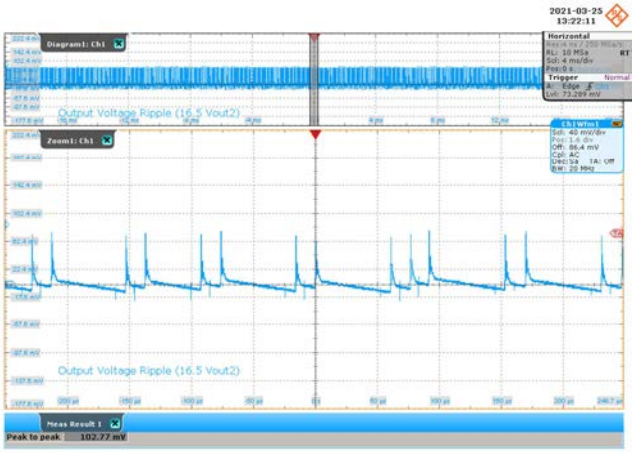


Figure 24 – 115 VAC Input.
Vertical: 40 mV / div.
Horizontal: 4 ms / div., 50 µs / div.
16.5 V_{OUT2} Ripple: 102.77 $mV_{PK-PK.}$

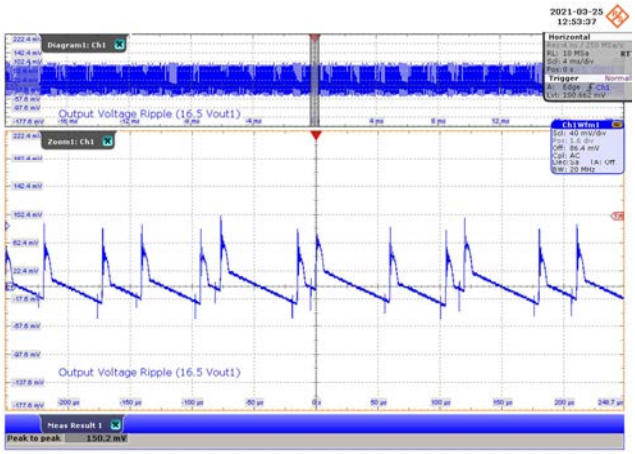


Figure 25 – 230 VAC Input.
Vertical: 40 mV / div.
Horizontal: 4 ms / div., 50 µs / div.
16.5 V_{OUT1} Ripple: 150.2 $mV_{PK-PK.}$

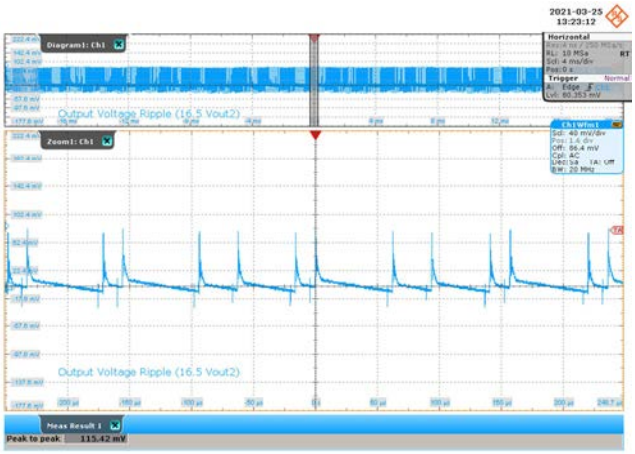


Figure 26 – 230 VAC Input.
Vertical: 40 mV / div.
Horizontal: 4 ms / div., 50 µs / div.
16.5 V_{OUT2} Ripple: 115.42 $mV_{PK-PK.}$

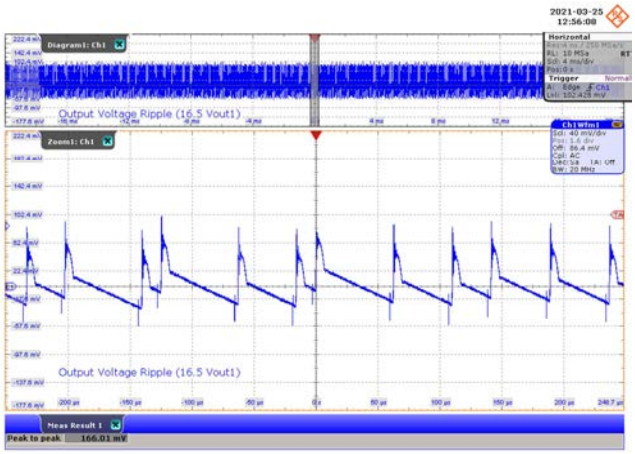


Figure 27 – 350 VAC Input.
Vertical: 40 mV / div.
Horizontal: 4 ms / div., 50 µs / div.
16.5 V_{OUT1} Ripple: 166.01 $mV_{PK-PK.}$

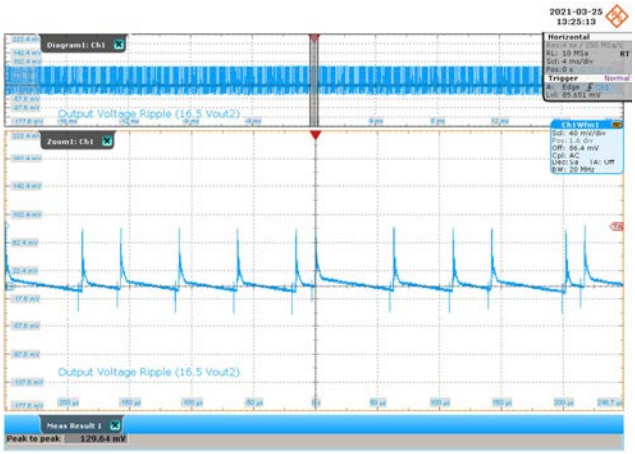


Figure 28 – 350 VAC Input.
Vertical: 40 mV / div.
Horizontal: 4 ms / div., 50 µs / div.
16.5 V_{OUT2} Ripple: 129.64 $mV_{PK-PK.}$

10.1.3 *Ripple Waveforms at No-Load*

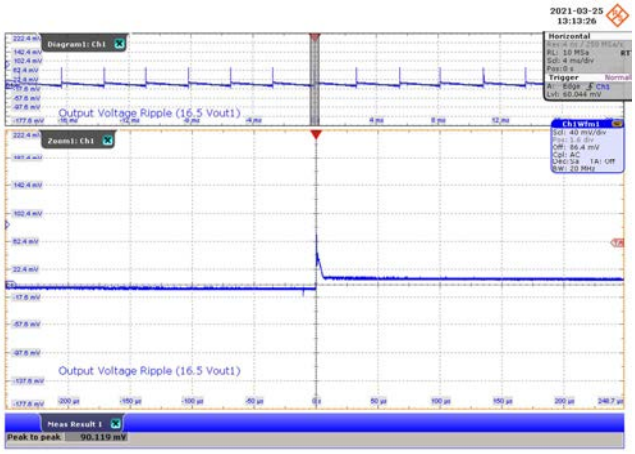


Figure 29 – 85 VAC Input.
Vertical: 40 mV / div.
Horizontal: 4 ms / div., 50 µs / div.
16.5 V_{OUT1} Ripple: 90.119 $mV_{PK-PK.}$

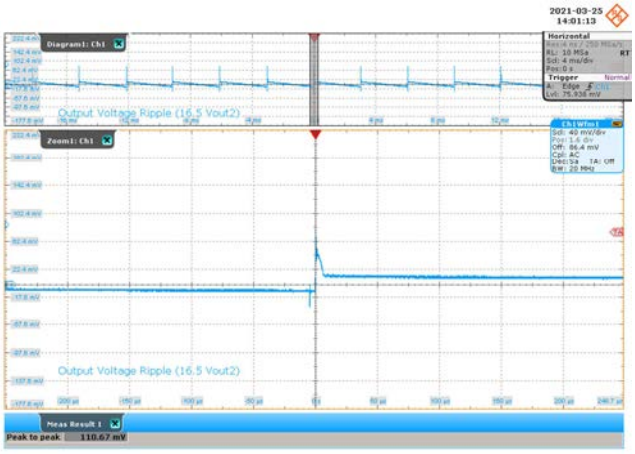


Figure 30 – 85 VAC Input.
Vertical: 40 mV / div.
Horizontal: 4 ms / div., 50 µs / div.
16.5 V_{OUT2} Ripple: 110.67 $mV_{PK-PK.}$

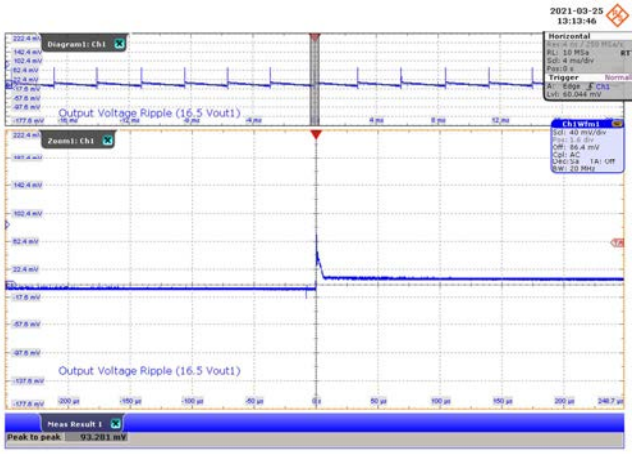


Figure 31 – 115 VAC Input.
Vertical: 40 mV / div.
Horizontal: 4 ms / div., 50 µs / div.
16.5 V_{OUT1} Ripple: 93.281 $mV_{PK-PK.}$

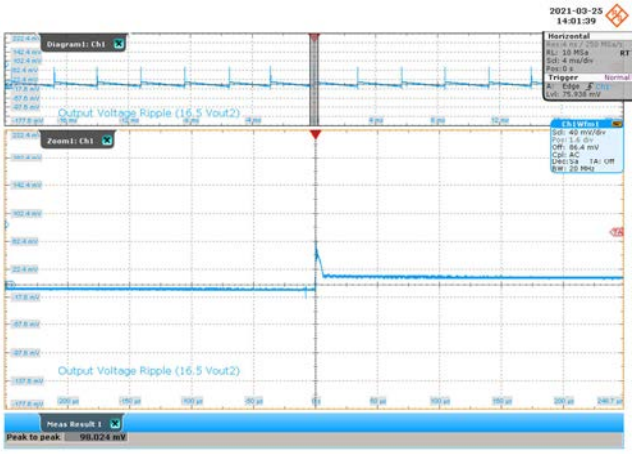


Figure 32 – 115 VAC Input.
Vertical: 40 mV / div.
Horizontal: 4 ms / div., 50 µs / div.
16.5 V_{OUT2} Ripple: 98.024 $mV_{PK-PK.}$

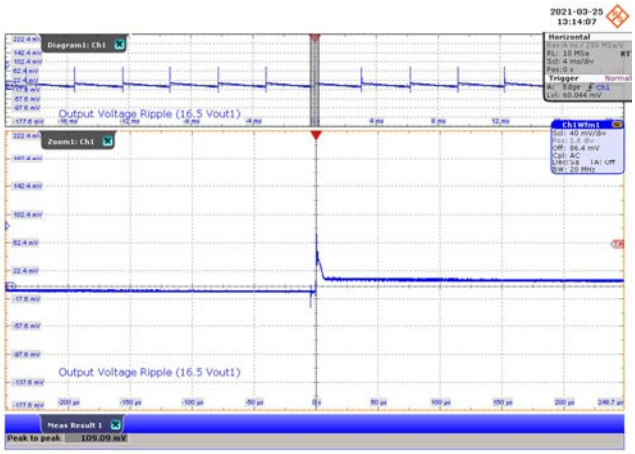


Figure 33 – 230 VAC Input.
Vertical: 40 mV / div.
Horizontal: 4 ms / div., 50 µs / div.
16.5 V_{OUT1} Ripple: 109.09 $mV_{PK-PK.}$

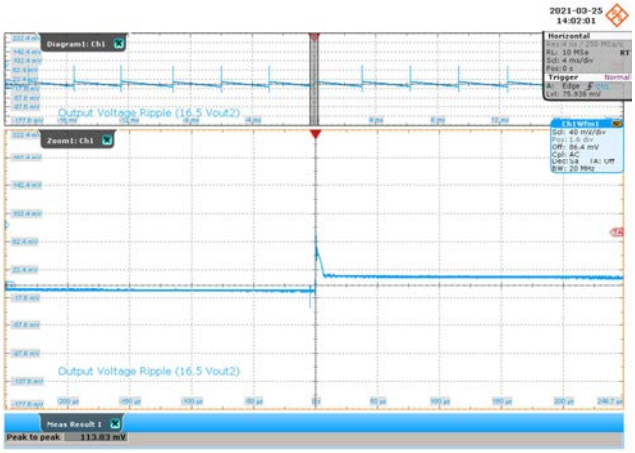


Figure 34 – 230 VAC Input.
Vertical: 40 mV / div.
Horizontal: 4 ms / div., 50 µs / div.
16.5 V_{OUT2} Ripple: 113.83 $mV_{PK-PK.}$

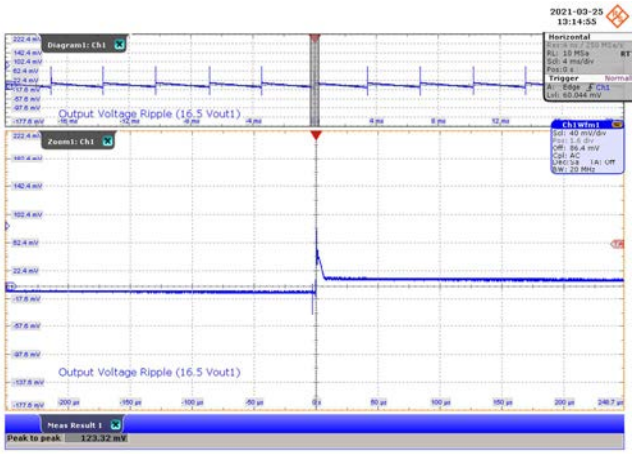


Figure 35 – 350 VAC Input.
Vertical: 40 mV / div.
Horizontal: 4 ms / div., 50 µs / div.
16.5 V_{OUT1} Ripple: 123.32 $mV_{PK-PK.}$

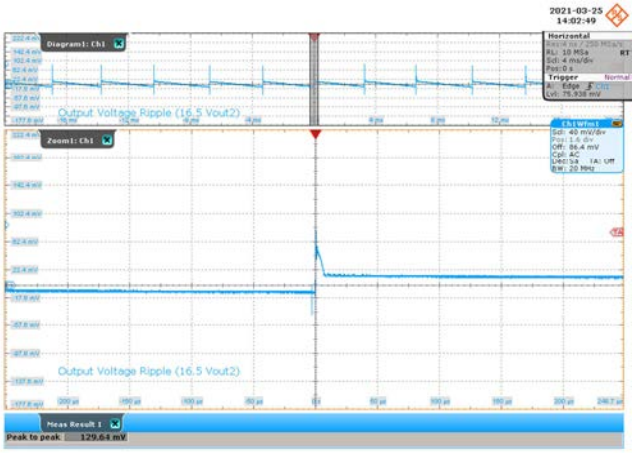


Figure 36 – 350 VAC Input.
Vertical: 40 mV / div.
Horizontal: 4 ms / div., 50 µs / div.
16.5 V_{OUT2} Ripple: 129.64 $mV_{PK-PK.}$

10.1.4 *Ripple vs. Load*

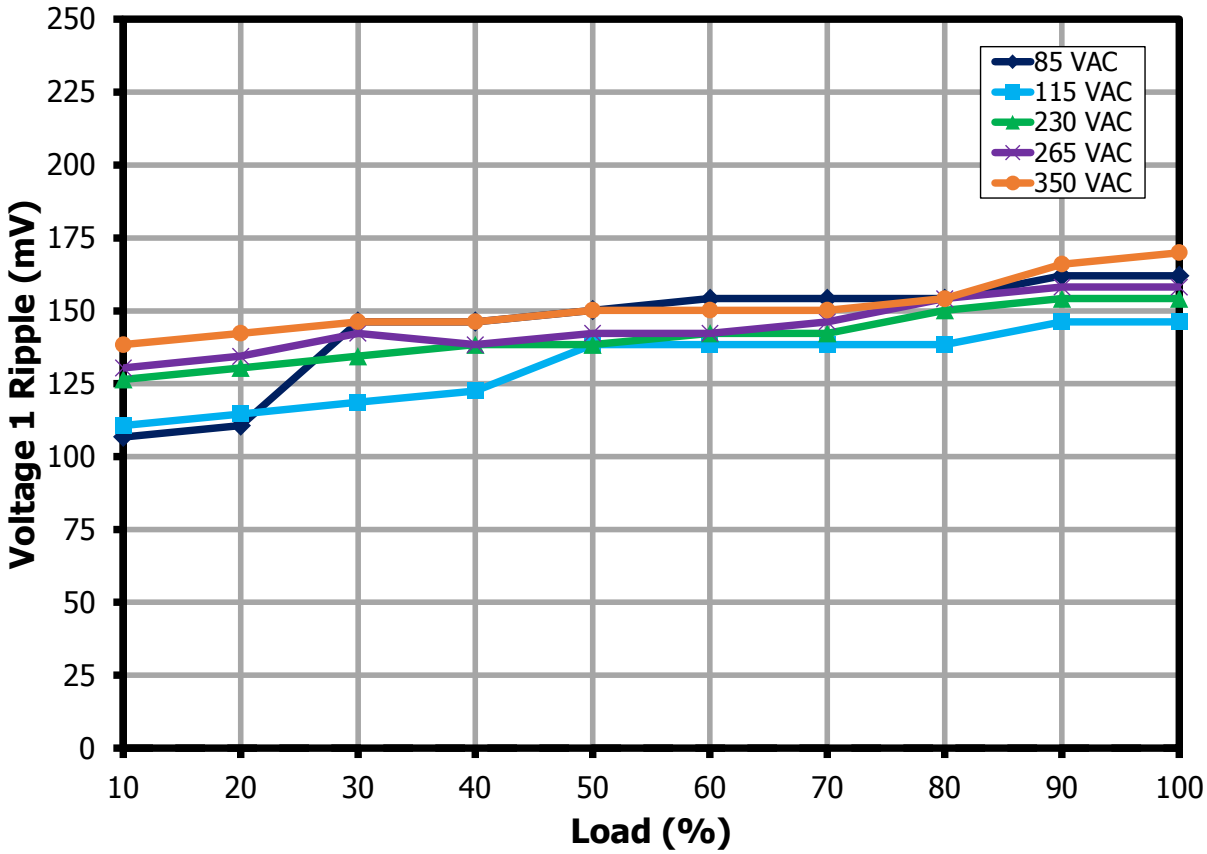


Figure 37 – 16.5 V_{OUT1} Output Ripple vs. Percent Load.

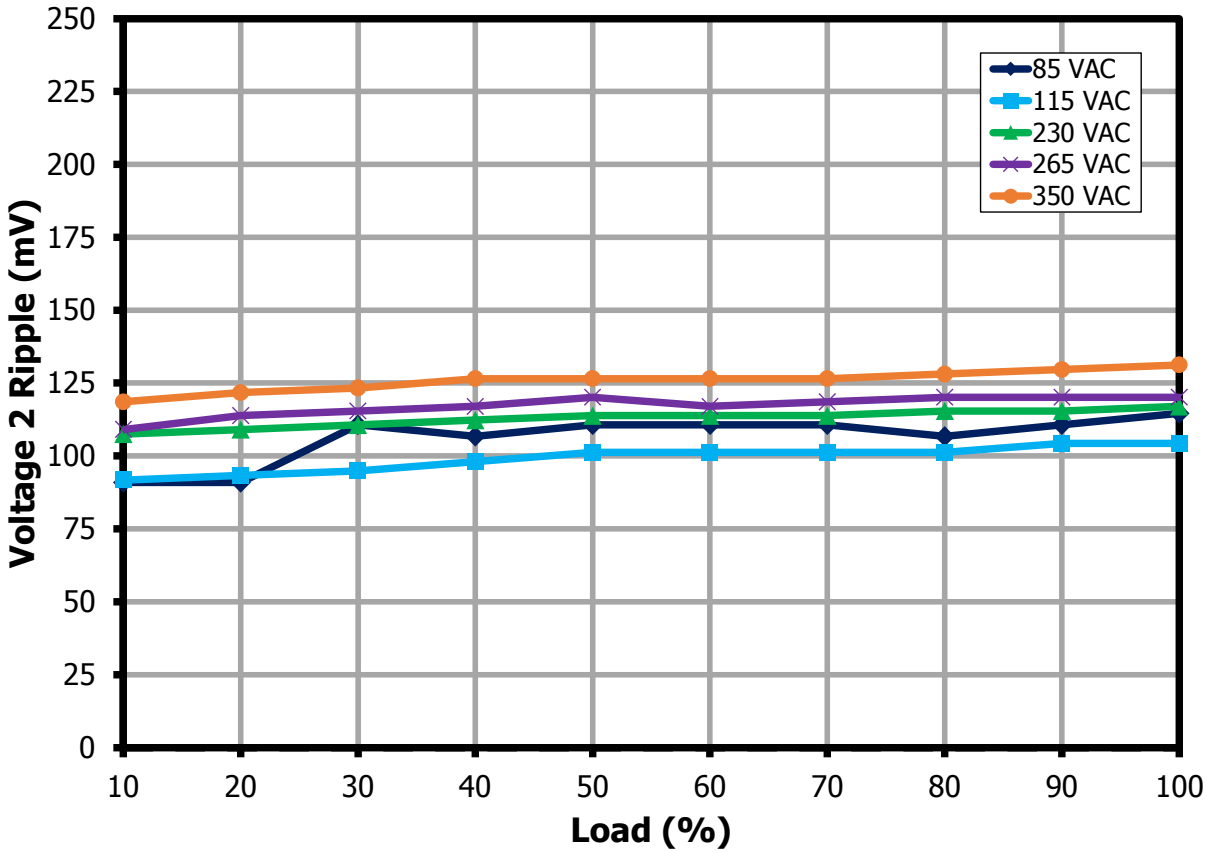


Figure 38 – 16.5 V_{OUT2} Output Ripple vs. Percent Load.

10.2 **Switching Waveforms**

10.2.1 *Drain Current and Drain Voltage*

Test conditions: 16.5 V_{OUT1} load set to CC at 300 mA, 16.5 V_{OUT2} load set to CC at 100 mA

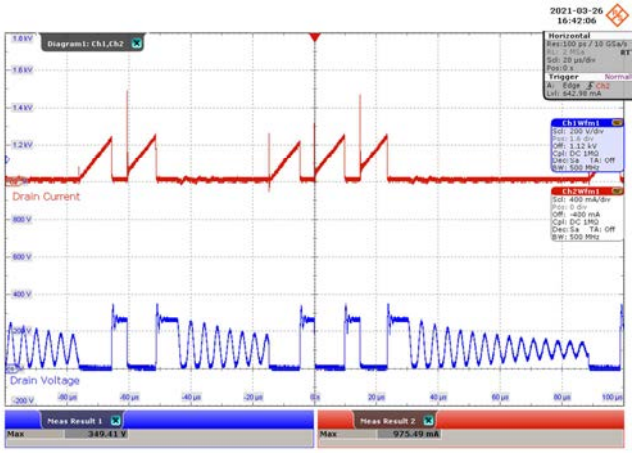


Figure 39 – 85 VAC Input.
Drain Voltage: 200 V / div., 20 µs / div.
Drain Current: 400 mA / div.
$V_{DS(MAX)}$: 349.41 V.
$I_{DS(MAX)}$: 975.49 mA.

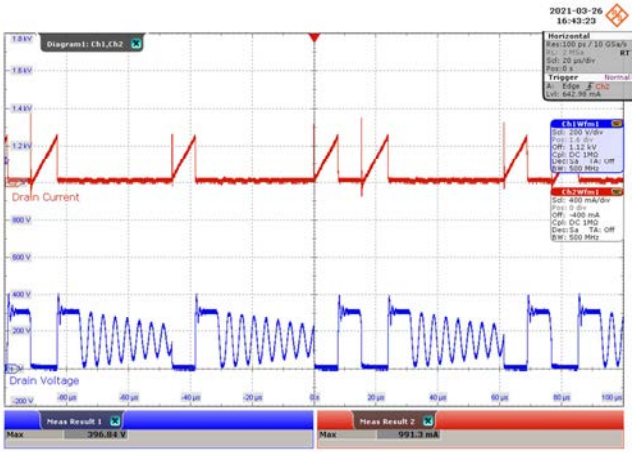


Figure 40 – 115 VAC Input.
Drain Voltage: 200 V / div., 20 µs / div.
Drain Current: 400 mA / div.
$V_{DS(MAX)}$: 396.84 V.
$I_{DS(MAX)}$: 991.3 mA.

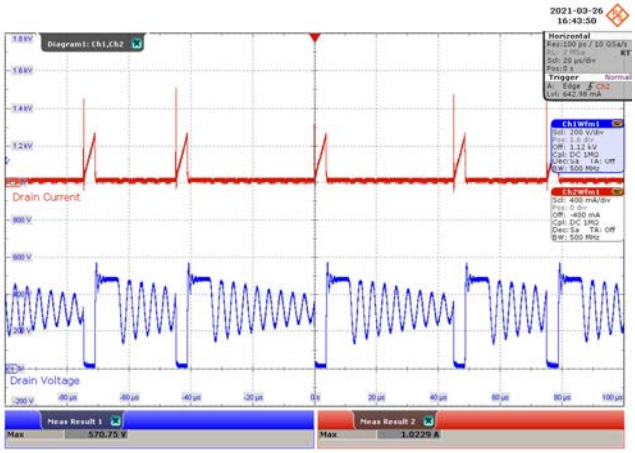


Figure 41 – 230 VAC Input.
Drain Voltage: 200 V / div., 20 µs / div.
Drain Current: 400 mA / div.
$V_{DS(MAX)}$: 570.75 V.
$I_{DS(MAX)}$: 1.0229 A.

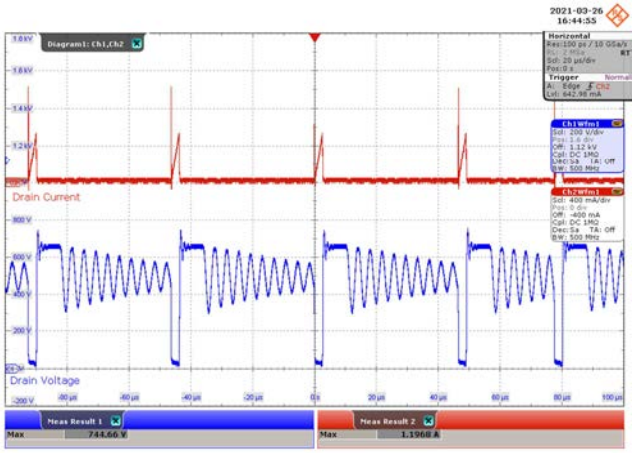


Figure 42 – 350 VAC Input.
Upper: V_{DS}, 200 V / div., 20 µs / div.
Lower: I_{DS}, 400 mA / div.
$V_{DS(MAX)}$: 744.66 V.
$I_{DS(MAX)}$: 1.1968 A.

10.2.2 *16.5 V_{OUT1} Output Diode Voltage and Current*

Test conditions: 16.5 V_{OUT1} load set to CC at 300 mA, 16.5 V_{OUT2} load set to CC at 100 mA

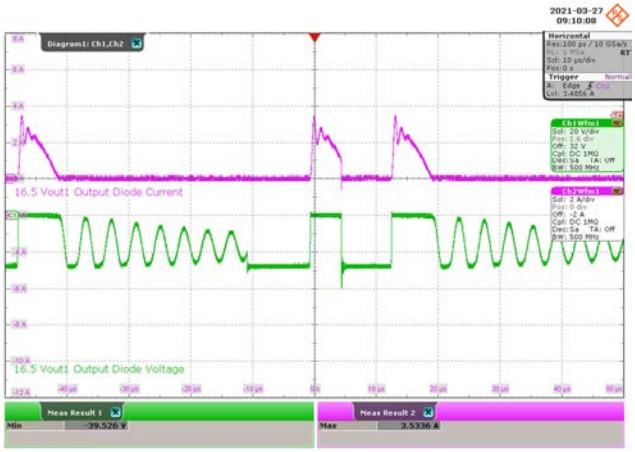


Figure 43 – 85 VAC Input.
Diode 1 Voltage: 20 V / div., 10 µs / div.
Diode 1 Current: 2 A / div.
PIV: 39.526 V.
$I_{D(MAX)}$: 3.5336 A.

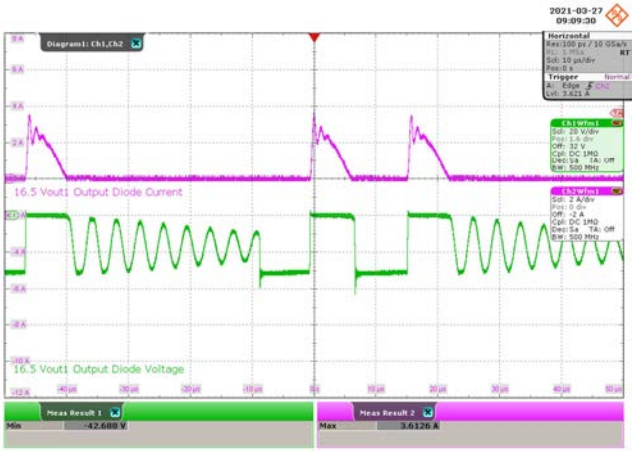


Figure 44 – 115 VAC Input.
Diode 1 Voltage: 20 V / div., 10 µs / div.
Diode 1 Current: 2 A / div.
PIV: 42.688 V.
$I_{D(MAX)}$: 3.6126 A.

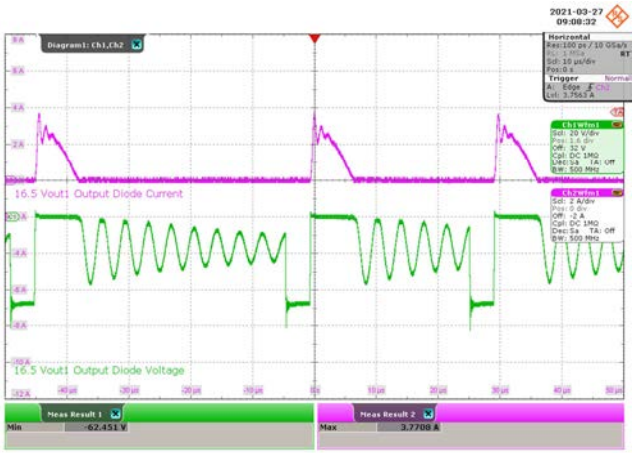


Figure 45 – 230 VAC Input.
Diode 1 Voltage: 20 V / div., 10 µs / div.
Diode 1 Current: 2 A / div.
PIV: 62.451 V.
$I_{D(MAX)}$: 3.7708 A.

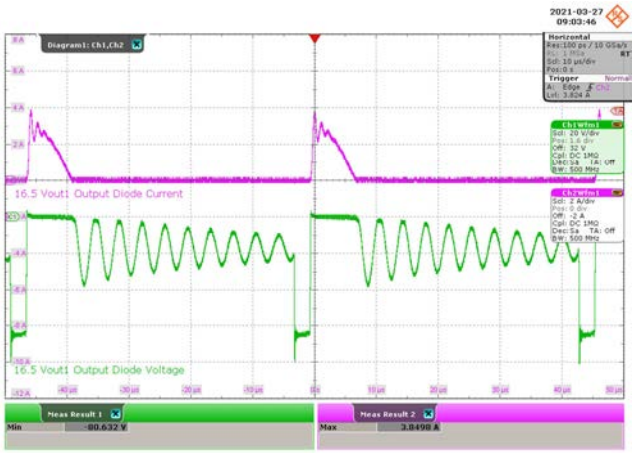


Figure 46 – 350 VAC Input.
Diode 1 Voltage: 20 V / div., 10 µs / div.
Diode 1 Current: 2 A / div.
PIV: 80.632 V.
$I_{D(MAX)}$: 3.8498 A.

10.2.3 *16.5 V_{OUT2} Output Diode Voltage and Current*

Test conditions: 16.5 V_{OUT1} load set to CC at 300 mA, 16.5 V_{OUT2} load set to CC at 100 mA

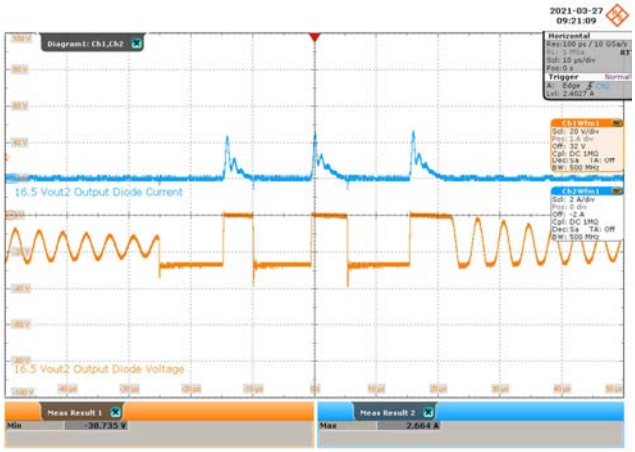


Figure 47 – 85 VAC Input.
Diode 1 Voltage: 20 V / div., 10 µs / div.
Diode 1 Current: 2 A / div.
PIV: 38.735 V.
$I_{D(MAX)}$: 2.664 A.

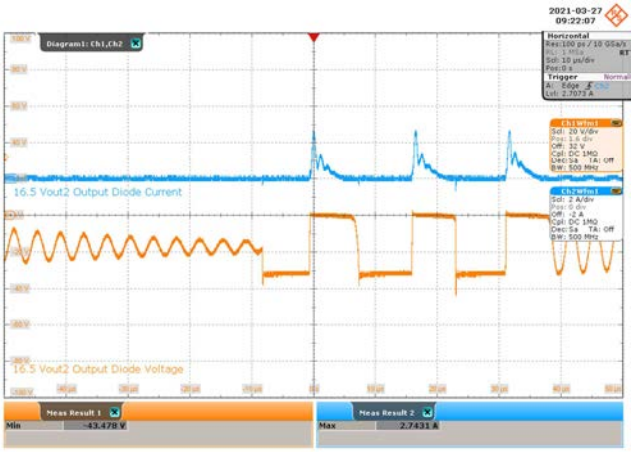


Figure 48 – 115 VAC Input.
Diode 1 Voltage: 20 V / div., 10 µs / div.
Diode 1 Current: 2 A / div.
PIV: 43.478 V.
$I_{D(MAX)}$: 2.7431 A.

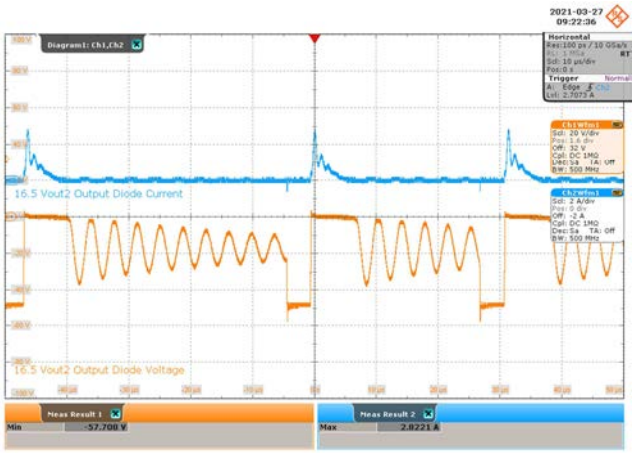


Figure 49 – 230 VAC Input.
Diode 1 Voltage: 20 V / div., 10 µs / div.
Diode 1 Current: 2 A / div.
PIV: 57.708 V.
$I_{D(MAX)}$: 2.8221 A.

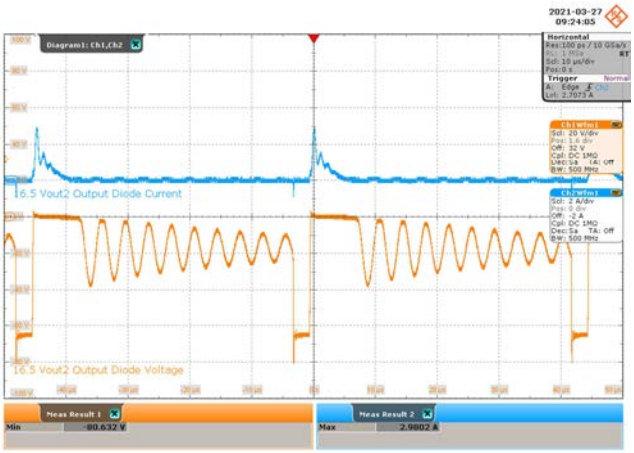


Figure 50 – 350 VAC Input.
Diode 1 Voltage: 20 V / div., 10 µs / div.
Diode 1 Current: 2 A / div.
PIV: 80.632 V.
$I_{D(MAX)}$: 2.9802 A.

10.3 **Start-up Performance**

10.3.1 *16.5 V_{OUT1} Start-up Operation V_{IN}, V_{OUT} and I_{OUT}*

Test conditions: 16.5 V_{OUT1} load set to CR at 55 Ω, 16.5 V_{OUT2} load set to CR at 165 Ω

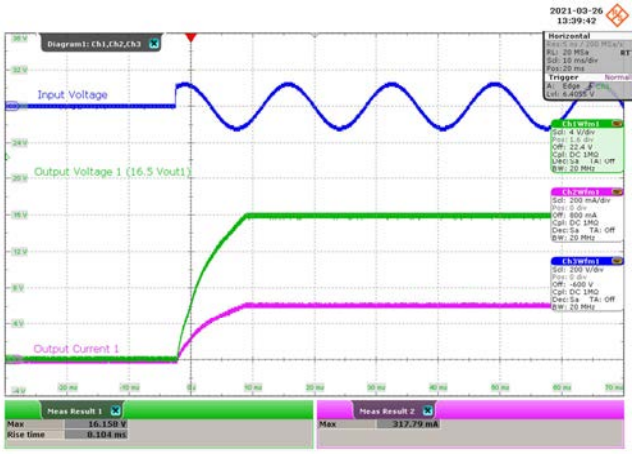


Figure 51 – 85 VAC Input.
Upper: V_{IN}, 200 V / div., 10 ms / div.
Middle: V_{OUT}, 4 V / div.
Lower: I_{OUT}, 200 mA / div.

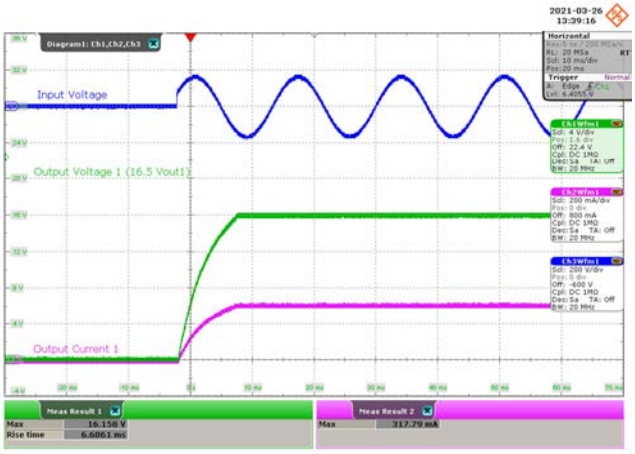


Figure 52 – 115 VAC Input.
Upper: V_{IN}, 200 V / div., 10 ms / div.
Middle: V_{OUT}, 4 V / div.
Lower: I_{OUT}, 200 mA / div.

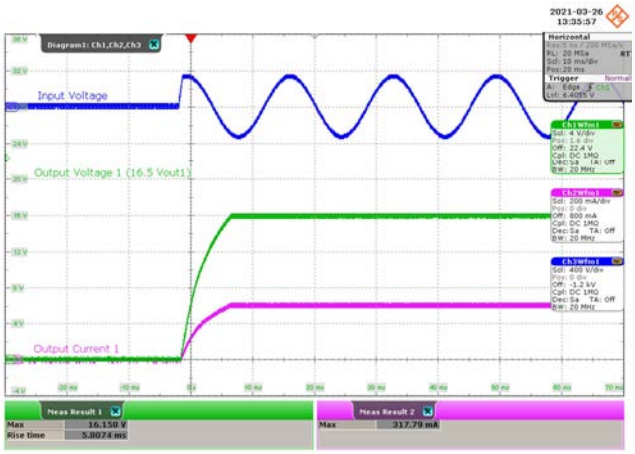


Figure 53 – 230 VAC Input.
Upper: V_{IN}, 400 V / div., 10 ms / div.
Middle: V_{OUT}, 4 V / div.
Lower: I_{OUT}, 200 mA / div.

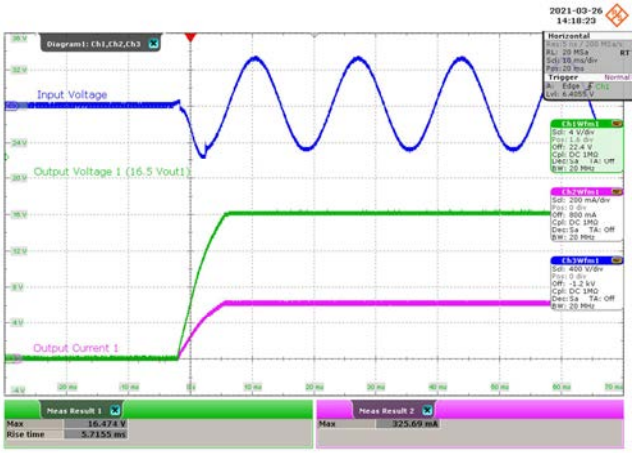


Figure 54 – 350 VAC Input.
Upper: V_{IN}, 400 V / div., 10 ms / div.
Middle: V_{OUT}, 4 V / div.
Lower: I_{OUT}, 200 mA / div.

10.3.2 *16.5 V_{OUT2} Start-up Operation V_{IN}, V_{OUT} and I_{OUT}*

Test conditions: 16.5 V_{OUT1} load set to CR at 55 Ω, 16.5 V_{OUT2} load set to CR at 165 Ω

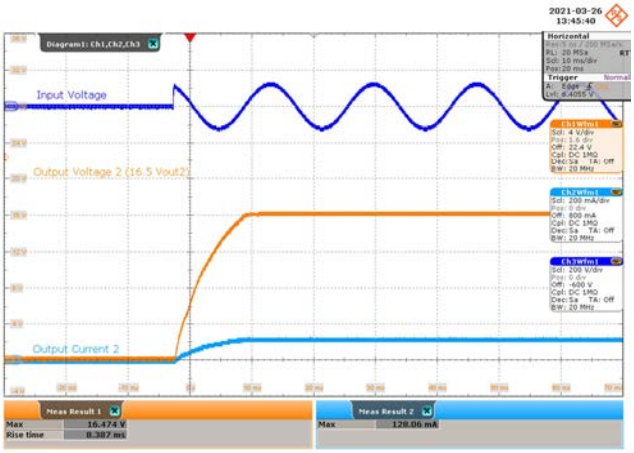


Figure 55 – 85 VAC Input.
Upper: V_{IN}, 200 V / div., 10 ms / div.
Middle: V_{OUT}, 4 V / div.
Lower: I_{OUT}, 200 mA / div.

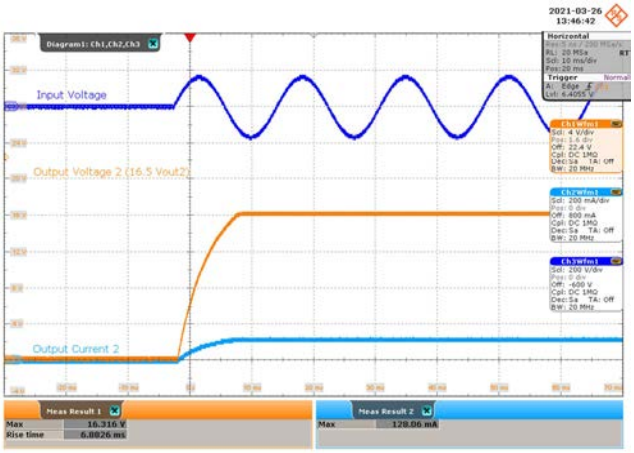


Figure 56 – 115 VAC Input.
Upper: V_{IN}, 200 V / div., 10 ms / div.
Middle: V_{OUT}, 4 V / div.
Lower: I_{OUT}, 200 mA / div.

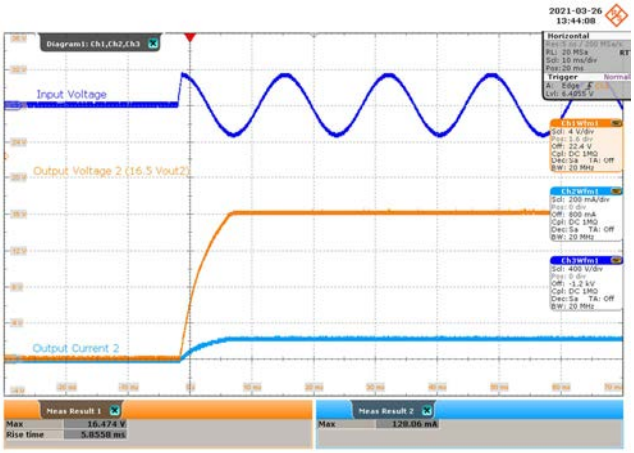


Figure 57 – 230 VAC Input.
Upper: V_{IN}, 400 V / div., 10 ms / div.
Middle: V_{OUT}, 4 V / div.
Lower: I_{OUT}, 200 mA / div.

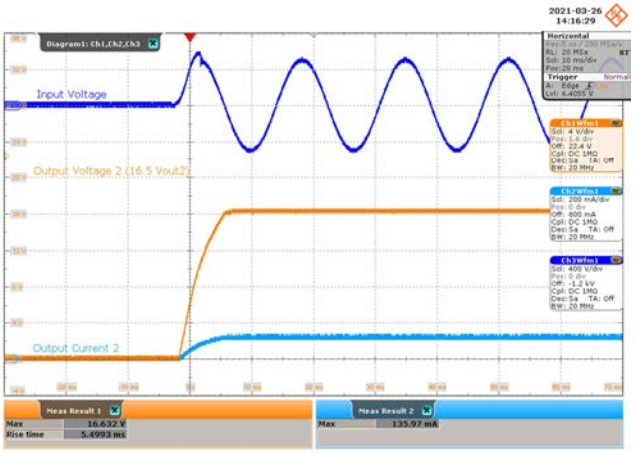


Figure 58 – 350 VAC Input.
Upper: V_{IN}, 400 V / div., 10 ms / div.
Middle: V_{OUT}, 4 V / div.
Lower: I_{OUT}, 200 mA / div.

10.3.3 *Drain Current and Drain Voltage Start-up Operation*

Test conditions: 16.5 V_{OUT1} load set to CC at 300 mA, 16.5 V_{OUT2} load set to CC at 100 mA

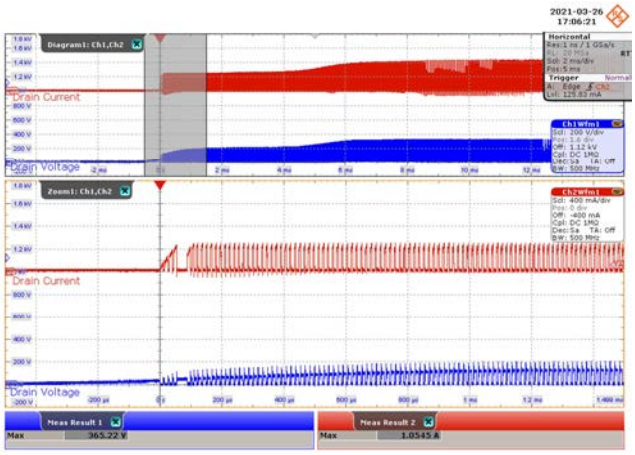


Figure 59 – 85 VAC Input.
Drain Voltage: 200 V / div., 2 ms / div.
Drain Current: 400 mA / div.
Zoom: 200 µs / div.
$V_{DS(MAX)}$: 365.22 V.
$I_{DS(MAX)}$: 1.0545 A.

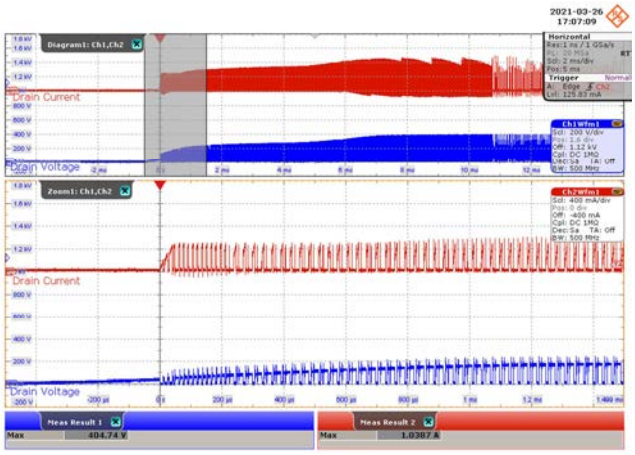


Figure 60 – 115 VAC Input.
Drain Voltage: 200 V / div., 2 ms / div.
Drain Current: 400 mA / div.
Zoom: 200 µs / div.
$V_{DS(MAX)}$: 404.74 V.
$I_{DS(MAX)}$: 1.0387 A.

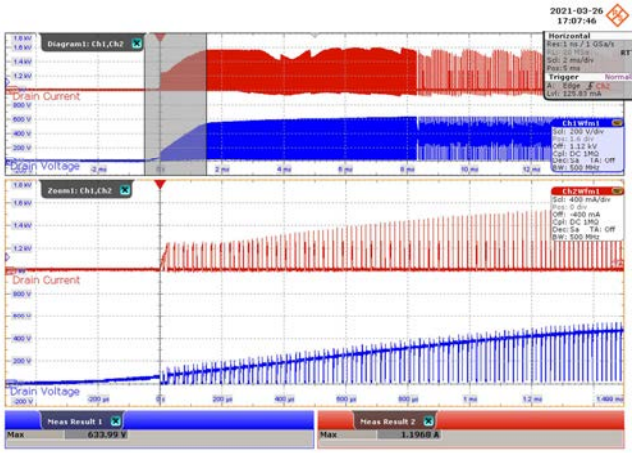


Figure 61 – 230 VAC Input.
Drain Voltage: 200 V / div., 2 ms / div.
Drain Current: 400 mA / div.
Zoom: 200 µs / div.
$V_{DS(MAX)}$: 633.99 V.
$I_{DS(MAX)}$: 1.1968 A.

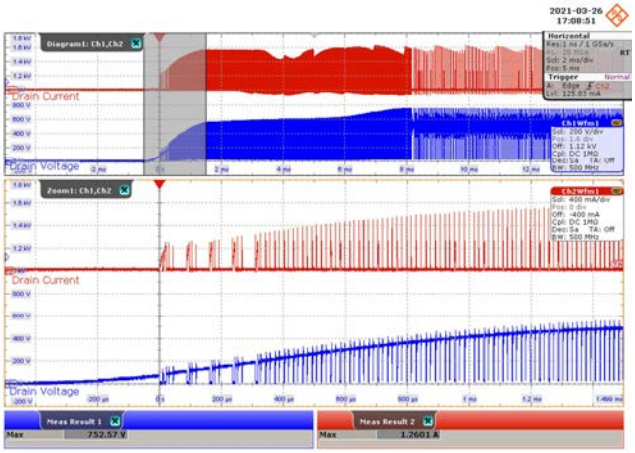


Figure 62 – 350 VAC Input.
Drain Voltage: 200 V / div., 2 ms / div.
Drain Current: 400 mA / div.
Zoom: 200 µs / div.
$V_{DS(MAX)}$: 752.57 V.
$I_{DS(MAX)}$: 1.2601 A.

10.4 **Output Load Transient**

10.4.1 *16.5 V_{OUT1} Output Transient*

Test conditions: 16.5 V_{OUT1} load swings from 30 mA to full load, 16.5 V_{OUT2} at full load

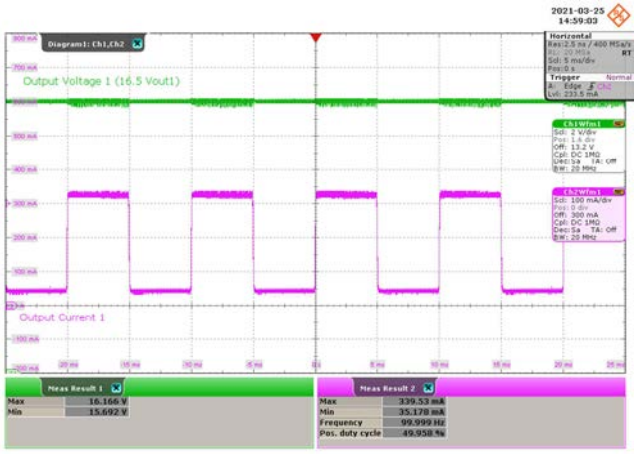


Figure 63 – 85 VAC Input.
16.5 V_{OUT1}: 2 V / div., 5 ms / div.
16.5 I_{OUT1}: 100 mA / div.
V_{MAX}: 16.166 V.
V_{MIN}: 15.692 V.

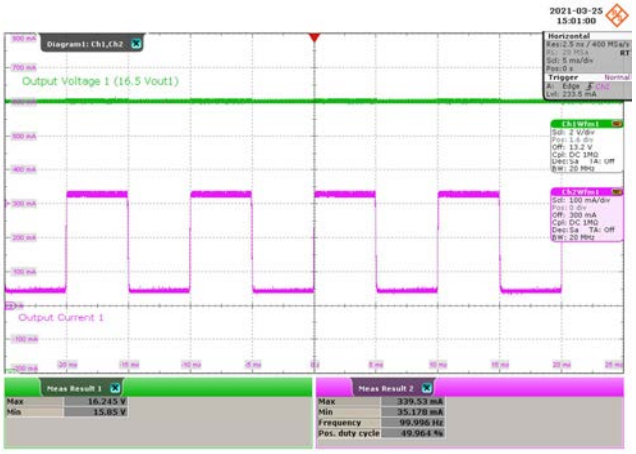


Figure 64 – 115 VAC Input.
16.5 V_{OUT1}: 2 V / div., 5 ms / div.
16.5 I_{OUT1}: 100 mA / div.
V_{MAX}: 16.245 V.
V_{MIN}: 15.85 V.

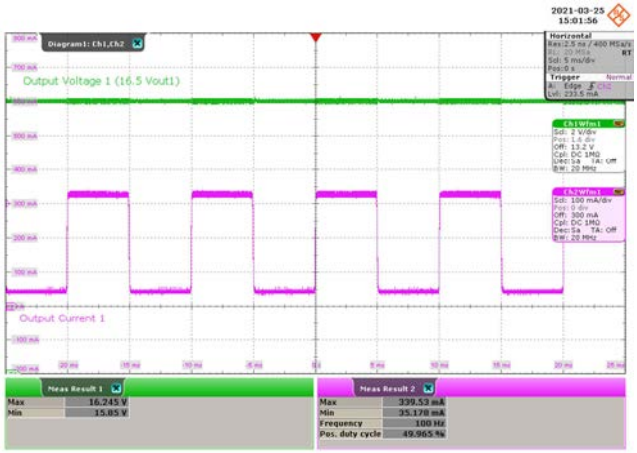


Figure 65 – 230 VAC Input.
16.5 V_{OUT1}: 2 V / div., 5 ms / div.
16.5 I_{OUT1}: 100 mA / div.
V_{MAX}: 16.245 V.
V_{MIN}: 15.85 V.

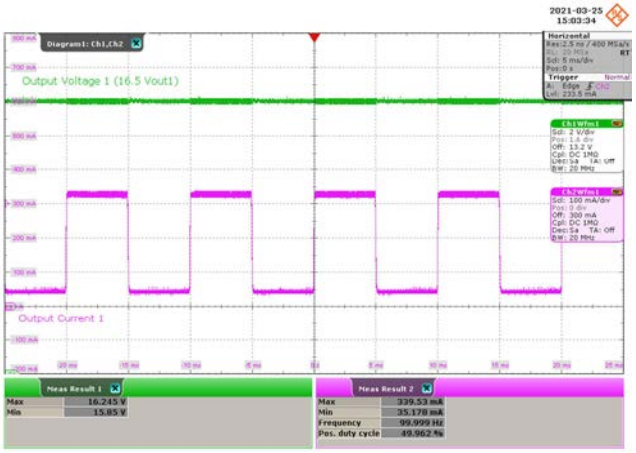


Figure 66 – 350 VAC Input.
16.5 V_{OUT1}: 2 V / div., 5 ms / div.
16.5 I_{OUT1}: 100 mA / div.
V_{MAX}: 16.245 V.
V_{MIN}: 15.85 V.

10.4.2 *16.5 V_{OUT2} Output Transient*

Test conditions: 16.5 V_{OUT2} load swings from 10 mA to full load, 16.5 V_{OUT1} at full load

Figure 67 – 85 VAC Input.
16.5 V_{OUT2}: 2 V / div., 5.2 ms / div.
16.5 I_{OUT2}: 100 mA / div.
V_{MAX}: 17.036 V.
V_{MIN}: 16.245 V.

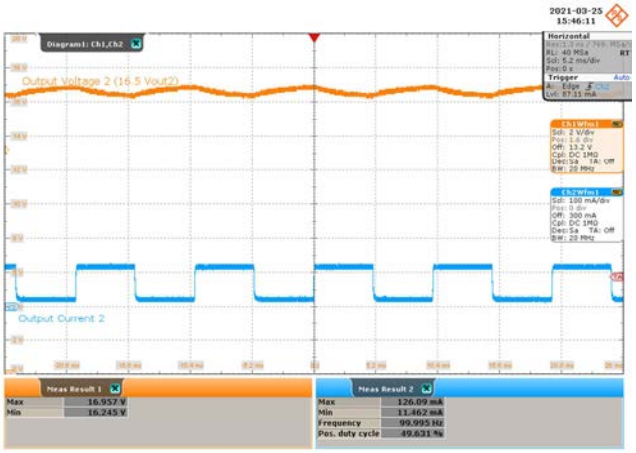


Figure 68 – 115 VAC Input.
16.5 V_{OUT2}: 2 V / div., 5.2 ms / div.
16.5 I_{OUT2}: 100 mA / div.
V_{MAX}: 16.957 V.
V_{MIN}: 16.245 V.

Figure 69 – 230 VAC Input.
16.5 V_{OUT2}: 2 V / div., 5.2 ms / div.
16.5 I_{OUT2}: 100 mA / div.
V_{MAX}: 17.036 V.
V_{MIN}: 16.245 V.

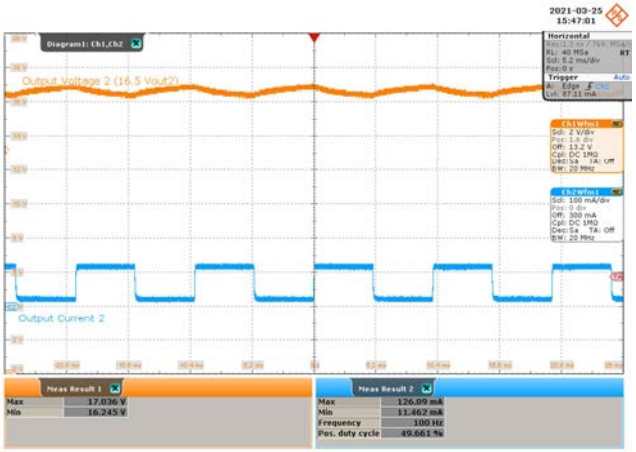


Figure 70 – 350 VAC Input.
16.5 V_{OUT2}: 2 V / div., 5.2 ms / div.
16.5 I_{OUT2}: 100 mA / div.
V_{MAX}: 17.036 V.
V_{MIN}: 16.245 V.

10.5 **Fault Waveforms**

10.5.1 *16.5 V_{OUT1} Output Short*

Test conditions: Both outputs at full load before short

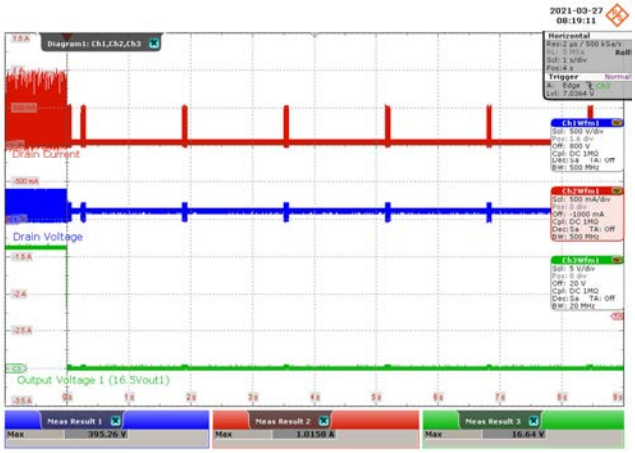


Figure 71 – 85 VAC Input.
16.5 V_{OUT1}: 5 V / div., 1 s / div.
Drain Current: 500 mA / div.
Drain Voltage: 500 V / div.

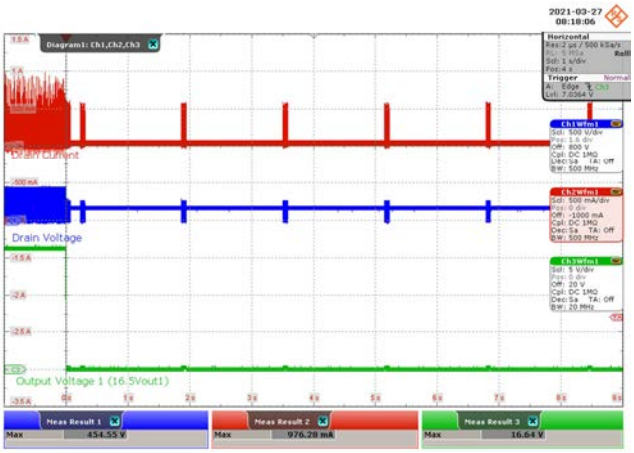


Figure 72 – 115 VAC Input.
16.5 V_{OUT1}: 5 V / div., 1 s / div.
Drain Current: 500 mA / div.
Drain Voltage: 500 V / div.

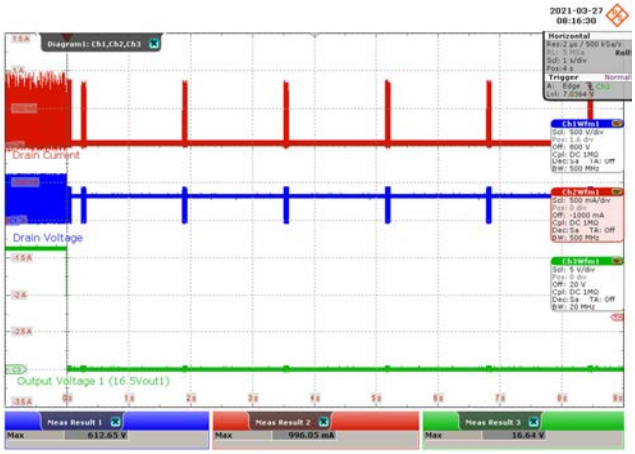


Figure 73 – 230 VAC Input.
16.5 V_{OUT1}: 5 V / div., 1 s / div.
Drain Current: 500 mA / div.
Drain Voltage: 500 V / div.

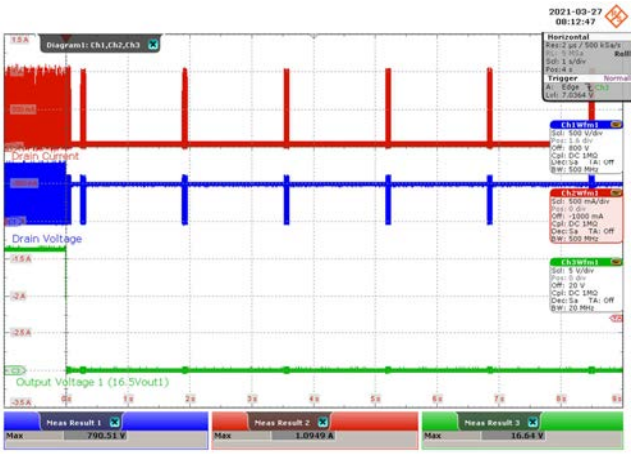


Figure 74 – 350 VAC Input.
16.5 V_{OUT1}: 5 V / div., 1 s / div.
Drain Current: 500 mA / div.
Drain Voltage: 500 V / div.

10.5.2 *16.5 V_{OUT2} Output Short*

Test conditions: Both outputs at full load before short

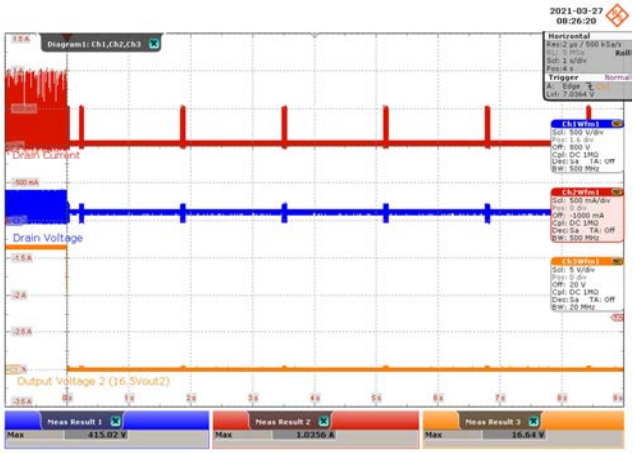


Figure 75 – 85 VAC Input.
16.5 V_{OUT2}: 5 V / div., 1 s / div.
Drain Current: 500 mA / div.
Drain Voltage: 500 V / div.

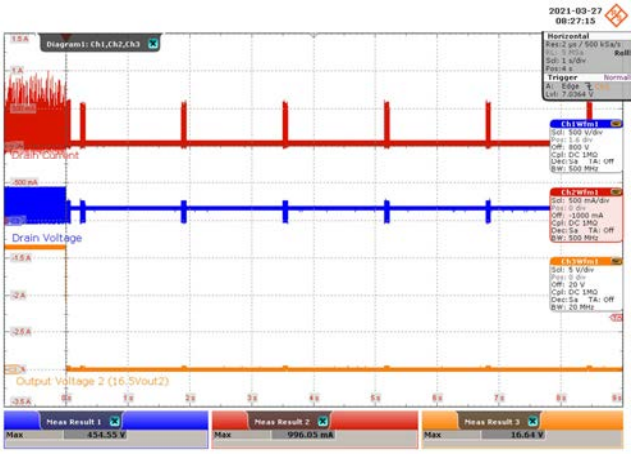


Figure 76 – 115 VAC Input.
16.5 V_{OUT2}: 5 V / div., 1 s / div.
Drain Current: 500 mA / div.
Drain Voltage: 500 V / div.

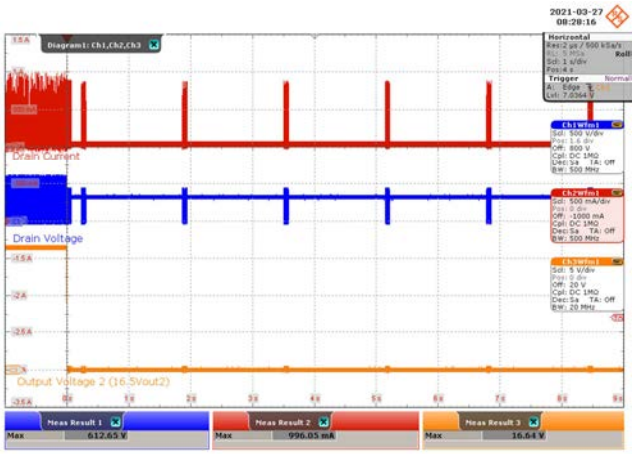


Figure 77 – 230 VAC Input.
16.5 V_{OUT2}: 5 V / div., 1 s / div.
Drain Current: 500 mA / div.
Drain Voltage: 500 V / div.

Figure 78 – 350 VAC Input.
16.5 V_{OUT2}: 5 V / div., 1 s / div.
Drain Current: 500 mA / div.
Drain Voltage: 500 V / div.

11 Thermal Performance

11.1 Test Set-Up

Thermal evaluation was performed under two conditions: (1) room temperature with the circuit board enclosed inside an acrylic box and (2), 50 ºC ambient inside a thermal chamber. In both conditions, the circuit is soaked for two hours under full load conditions.

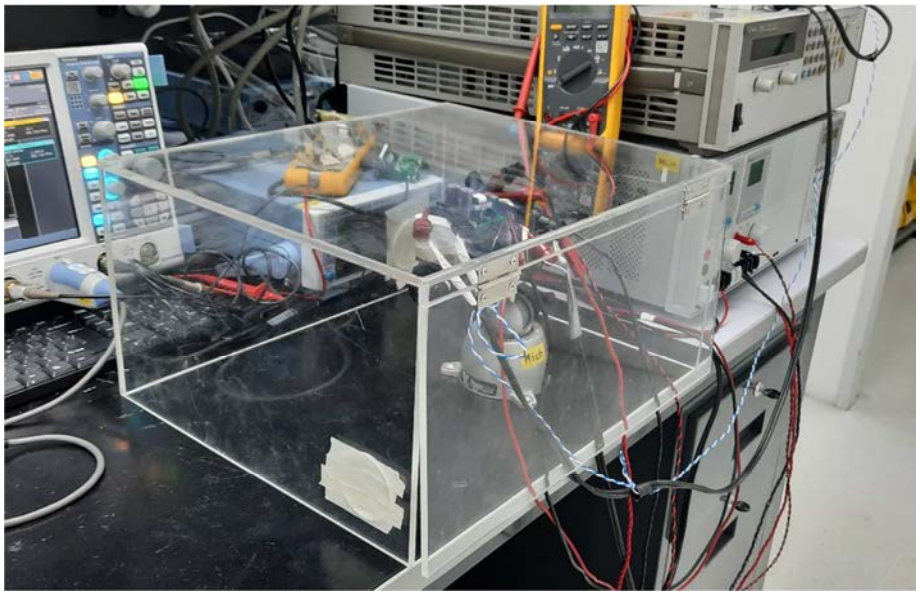


Figure 79 – Thermal Performance Set-up Using an Acrylic Box.

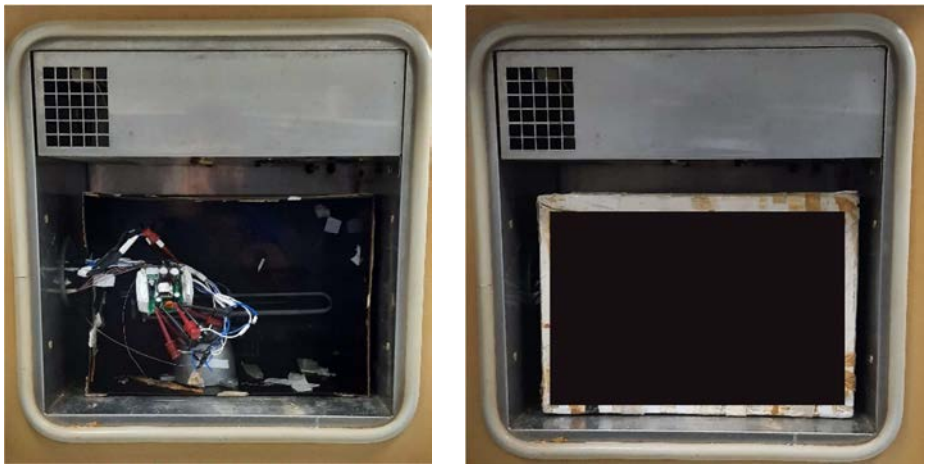


Figure 80 – Thermal Performance Set-up Using Thermal Chamber.

11.2 **Room Temperature**

11.2.1 *85 VAC, Room Temperature*

Test conditions: 16.5 V_{OUT1} load set to CC at 300 mA, 16.5 V_{OUT2} load set to CC at 100 mA

LinkSwitch-XT2 900 V (U1)	Transformer (T1)	Bridge Rectifier (BR1)	Clamp Diode (D1)	16.5 V_{OUT1} Output Diode (D3)	16.5 V_{OUT2} Output Diode (D4)	Ambient Temperature
51.6 ºC	53.8 ºC	43.5 ºC	52.1 ºC	58.0 ºC	48.9 ºC	26.7 ºC

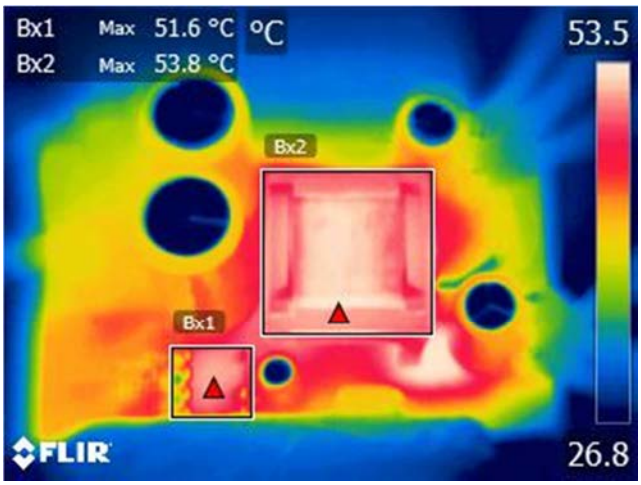


Figure 81 – Ambient = 26.8 ºC.
Bx1, U1: 51.6 ºC.
Bx2, T1: 53.8 ºC.

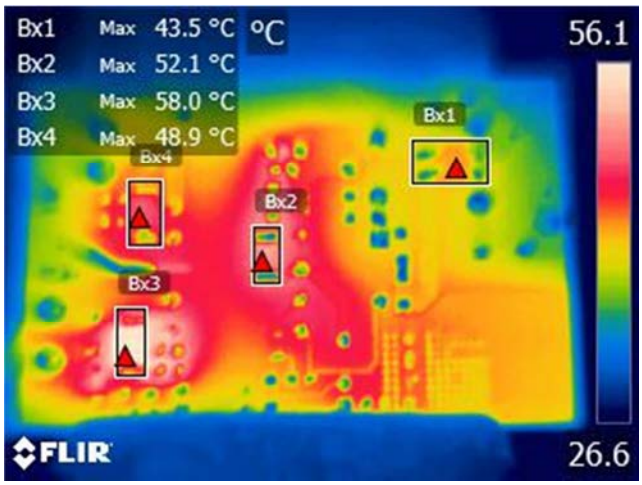


Figure 82 – Ambient = 26.6 ºC.
Bx1, BR1: 43.5 ºC.
Bx2, D1: 52.1 ºC.
Bx3, D3: 58.0 ºC.
Bx4, D4: 48.9 ºC.

11.2.2 *350 VAC, Room Temperature*

Test conditions: 16.5 V_{OUT1} load set to CC at 300 mA, 16.5 V_{OUT2} load set to CC at 100 mA

LinkSwitch-XT2 900 V (U1)	Transformer (T1)	Bridge Rectifier (BR1)	Clamp Diode (D1)	16.5 V_{OUT1} Output Diode (D3)	16.5 V_{OUT2} Output Diode (D4)	Ambient Temperature
48.6 ºC	52.4 ºC	36.4 ºC	48.2 ºC	57.9 ºC	48.5 ºC	24.8 ºC

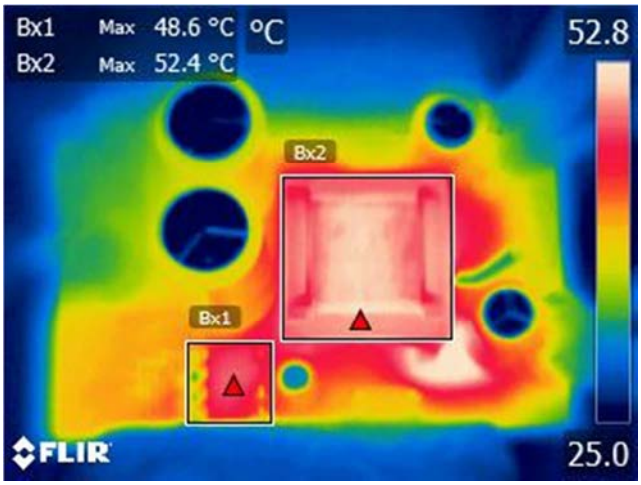


Figure 83 – Ambient = 25.0 ºC.
Bx1, U1: 48.6 ºC.
Bx2, T1: 52.4 ºC.

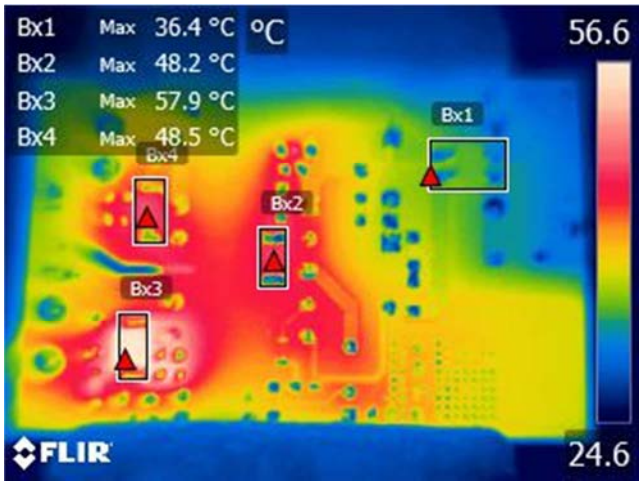


Figure 84 – Ambient = 24.6 ºC.
Bx1, BR1: 36.4 ºC.
Bx2, D1: 48.2 ºC.
Bx3, D3: 57.9 ºC.
Bx4, D4: 48.5 ºC.

11.3 **50 ºC Ambient**

11.3.1 *85 VAC, 50 ºC*

Test conditions: 16.5 V_{OUT1} load set to CC at 300 mA, 16.5 V_{OUT2} load set to CC at 100 mA

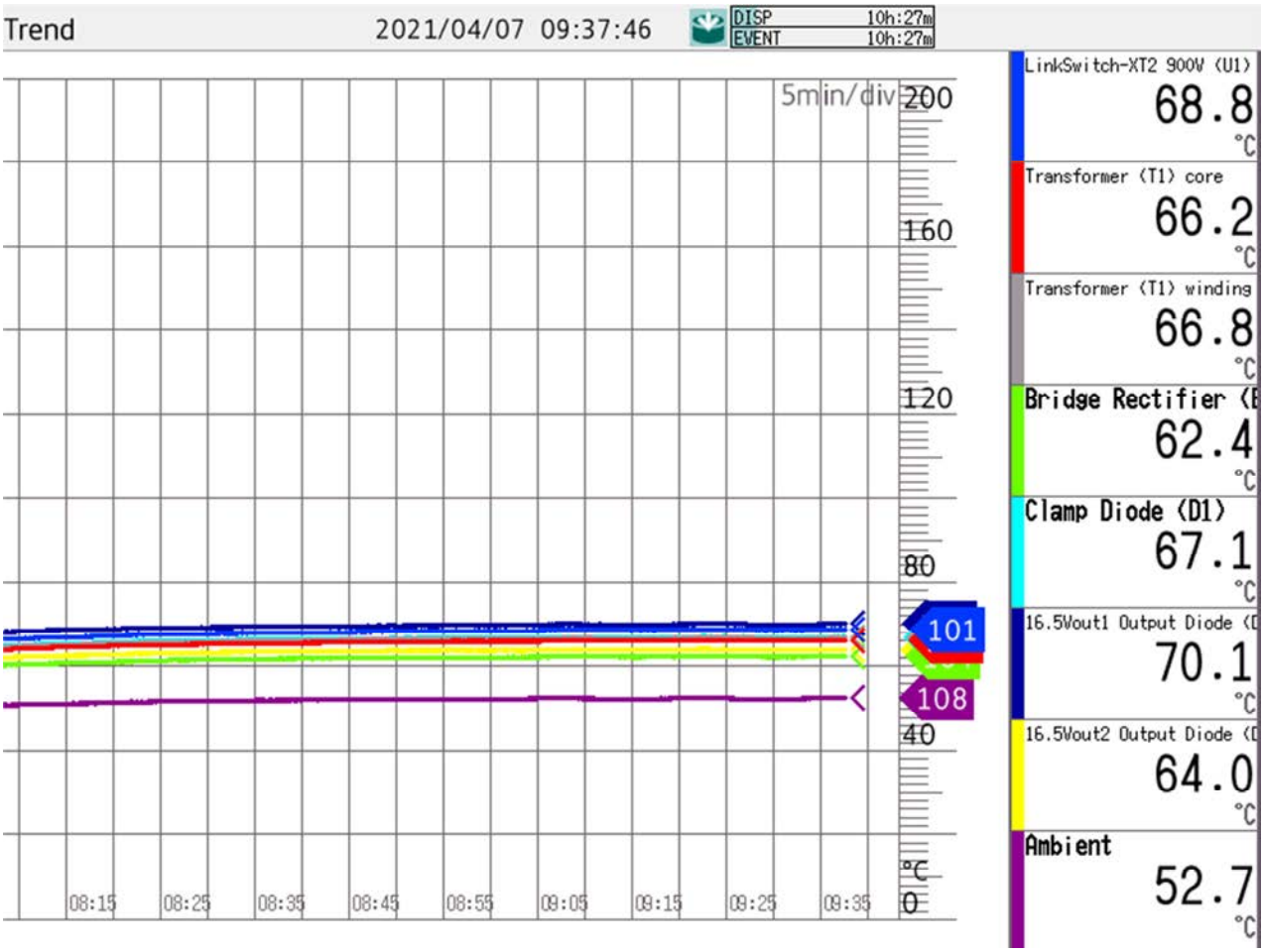


Figure 85 – Component Temperatures at 50 ºC Ambient.

11.3.2 *350 VAC, 50 ºC*

Test conditions: 16.5 V_{OUT1} load set to CC at 300 mA, 16.5 V_{OUT2} load set to CC at 100 mA

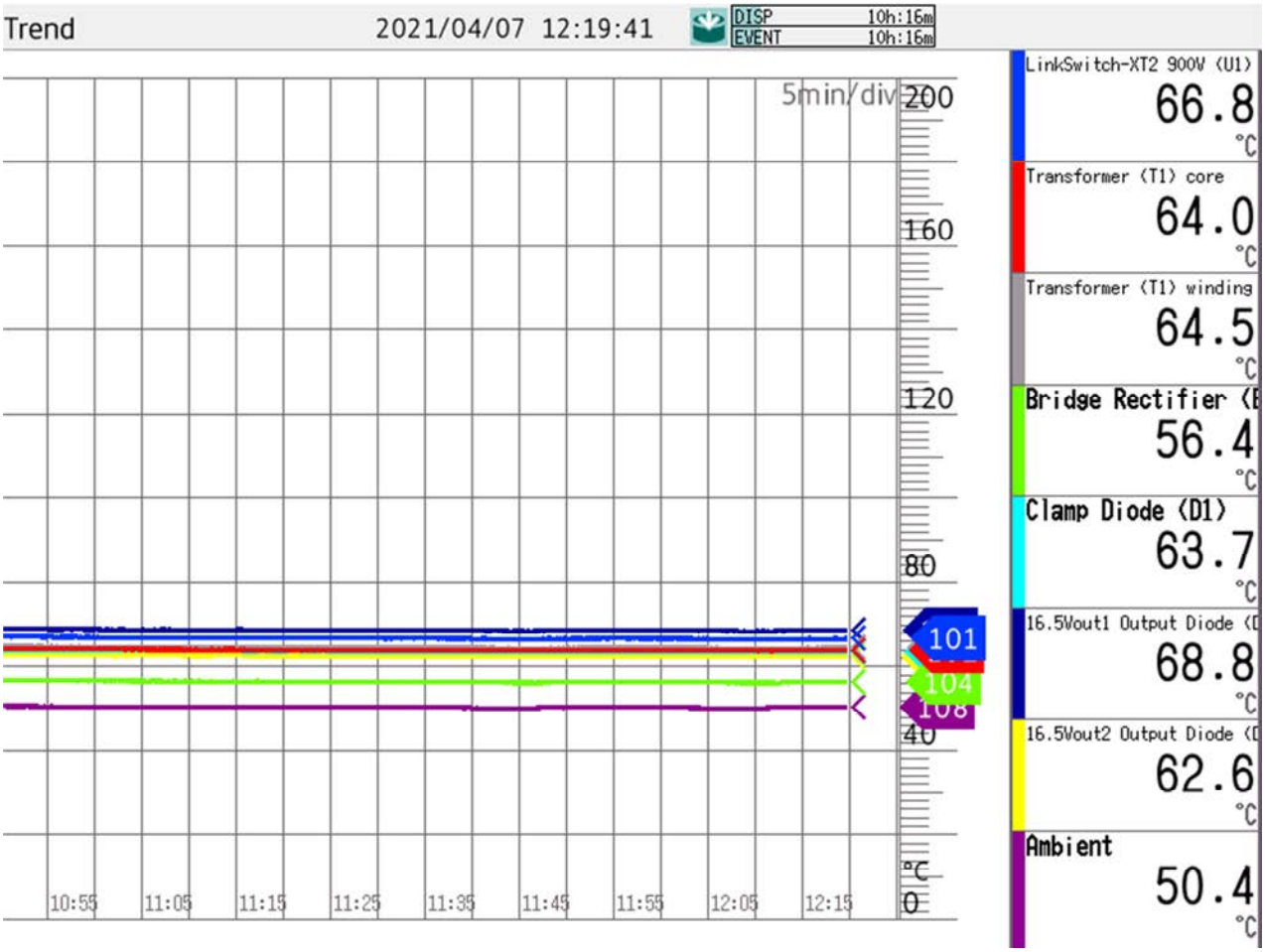


Figure 86 – Component Temperatures at 50 ºC Ambient.

12 Conducted EMI

12.1 EMI Equipment and Load

1. Rohde and Schwarz ENV216 two line V-network.
2. Rohde and Schwarz ESRP EMI test receiver.
3. Yokogawa W310E digital power meter.
4. Chroma measurement test fixture, model A662003.
5. Resistor load with input voltage set at 115 VAC.

12.2 Test Set-up

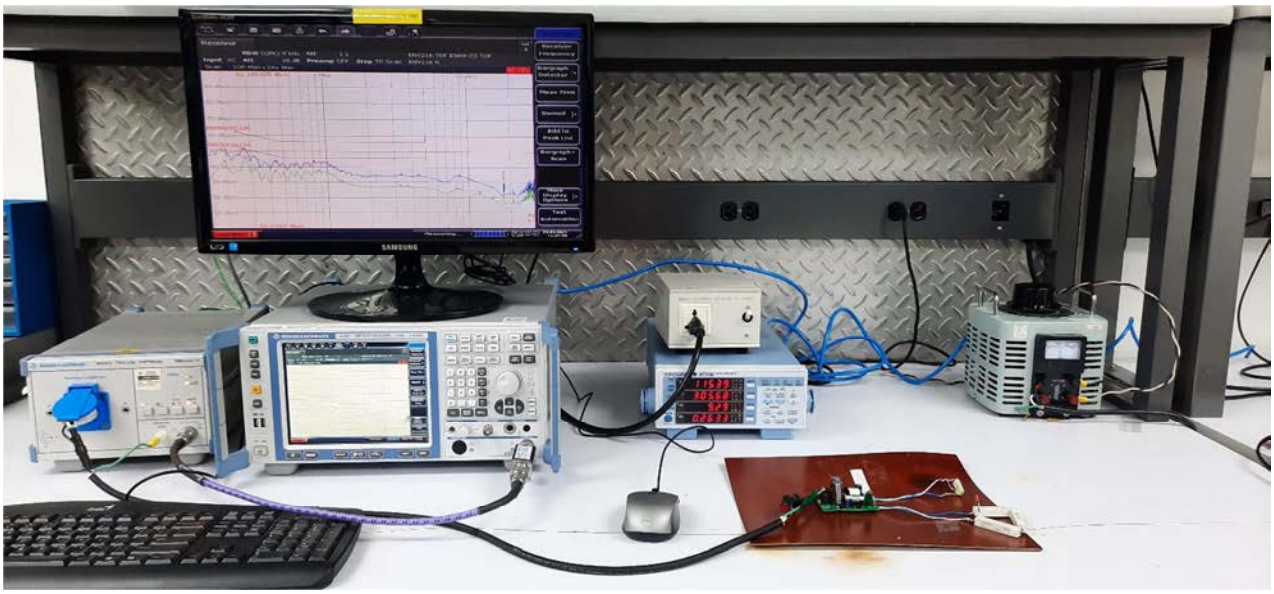


Figure 87 – Conducted EMI Test Set-up.

12.3 **EMI Test Results**

12.3.1 *115 VAC, Floating Output*

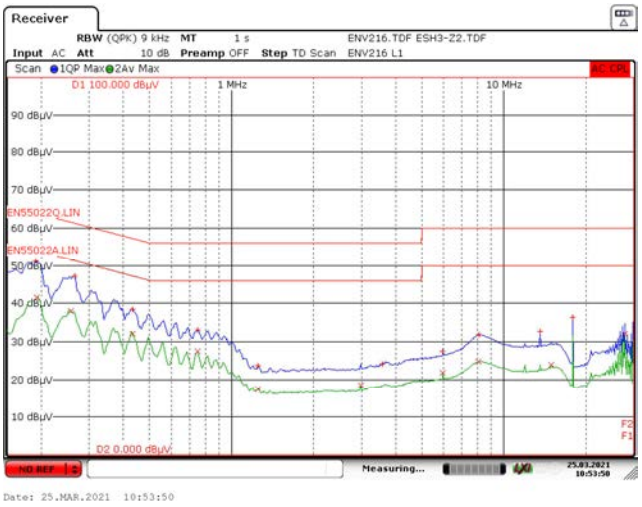


Figure 88 – Line.
Upper: Lowest Peak Delta Limit:
-12.90 dB, 190.60 kHz.
Lower: Lowest Average Delta Limit:
-12.31 dB, 192.85 kHz.

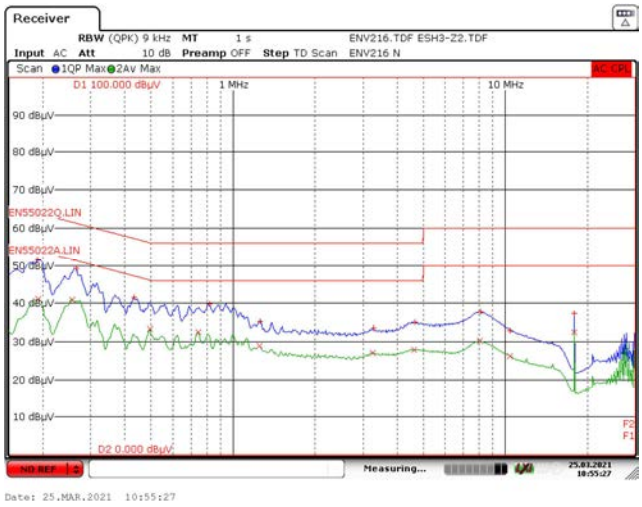


Figure 89 – Neutral.
Upper: Lowest Peak Delta Limit:
-11.99 dB, 264.85 kHz.
Lower: Lowest Average Delta Limit:
-10.69 dB, 255.85 kHz.

12.3.2 *230 VAC, Floating Output*

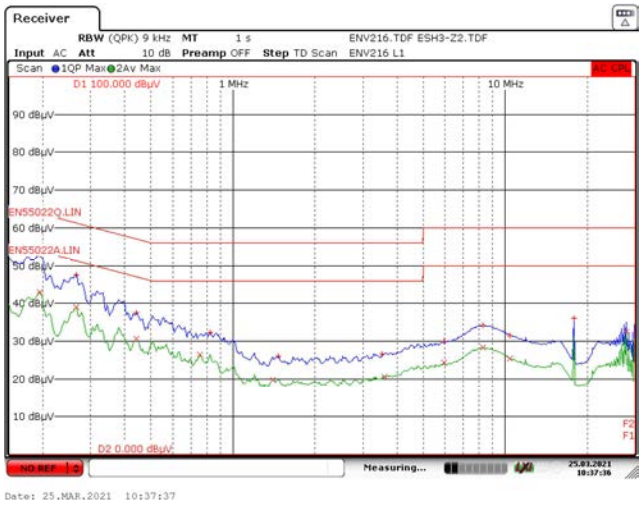


Figure 90 – Line.
Upper: Lowest Peak Delta Limit:
-11.13 dB, 190.60 kHz.
Lower: Lowest Average Delta Limit:
-10.94 dB, 195.10 kHz.

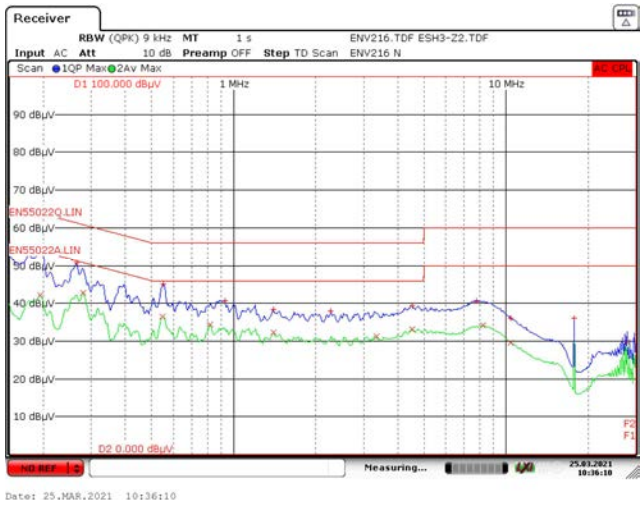


Figure 91 – Neutral.
Upper: Lowest Peak Delta Limit:
-10.55 dB, 190.60 kHz.
Lower: Lowest Average Delta Limit:
-8.07 dB, 280.60 kHz.

13 Line Surge

The unit was subject to ±6000 V differential surge test using 10 strikes at each condition. A test failure is defined as a non-recoverable interruption of output requiring repair or recycling of input voltage.

13.1 Differential Surge Test

Surge Voltage (kV)	Phase Angle (°)	IEC Coupling	Generator Impedance (Ω)	Number Strikes	Result
+6	0	L1 / L2	2	10	PASS
-6	0	L1 / L2	2	10	PASS
+6	90	L1 / L2	2	10	PASS
-6	90	L1 / L2	2	10	PASS
+6	180	L1 / L2	2	10	PASS
-6	180	L1 / L2	2	10	PASS
+6	270	L1 / L2	2	10	PASS
-6	270	L1 / L2	2	10	PASS

Note: In all PASS results, no damage and no auto-restart was observed.

14 Performance with External Magnetizing Interference

14.1 Test Set-up

A Neodymium Iron Boron (NdFeB) square magnet with N35 Grade, dimensions of 6.35 mm x 6.35 mm, and Gauss strength (surface Gauss) of 3451 G was placed on the transformer core such that the typical primary inductance was reduced by at least 50%.

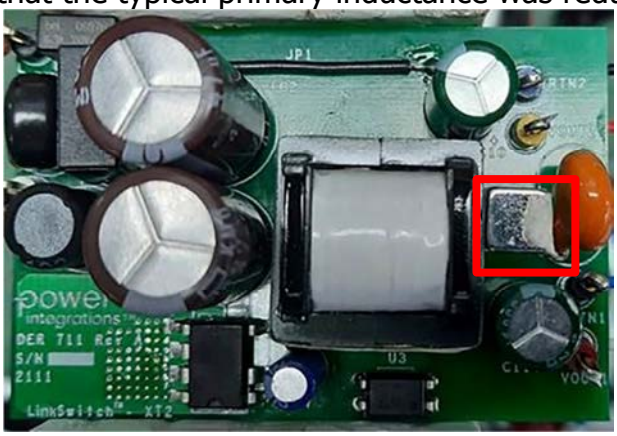


Figure 92 – Performance with External Magnetizing Interference Test Set-up.

14.2 No-Load Input Power with External Magnetizing Interference

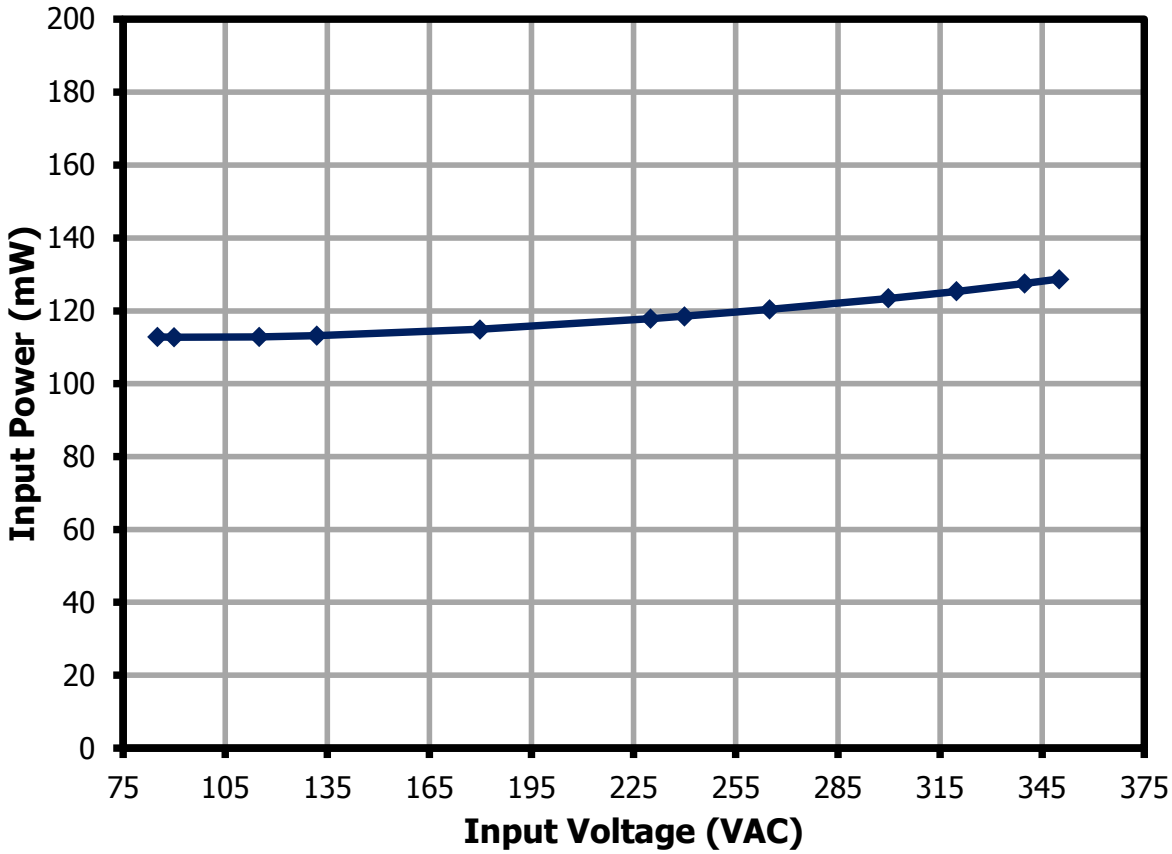


Figure 93 – No-Load Power vs. Input Line Voltage.

14.3 **Efficiency with External Magnetizing Interference**

14.3.1 *Efficiency vs Line with External Magnetizing Interference*

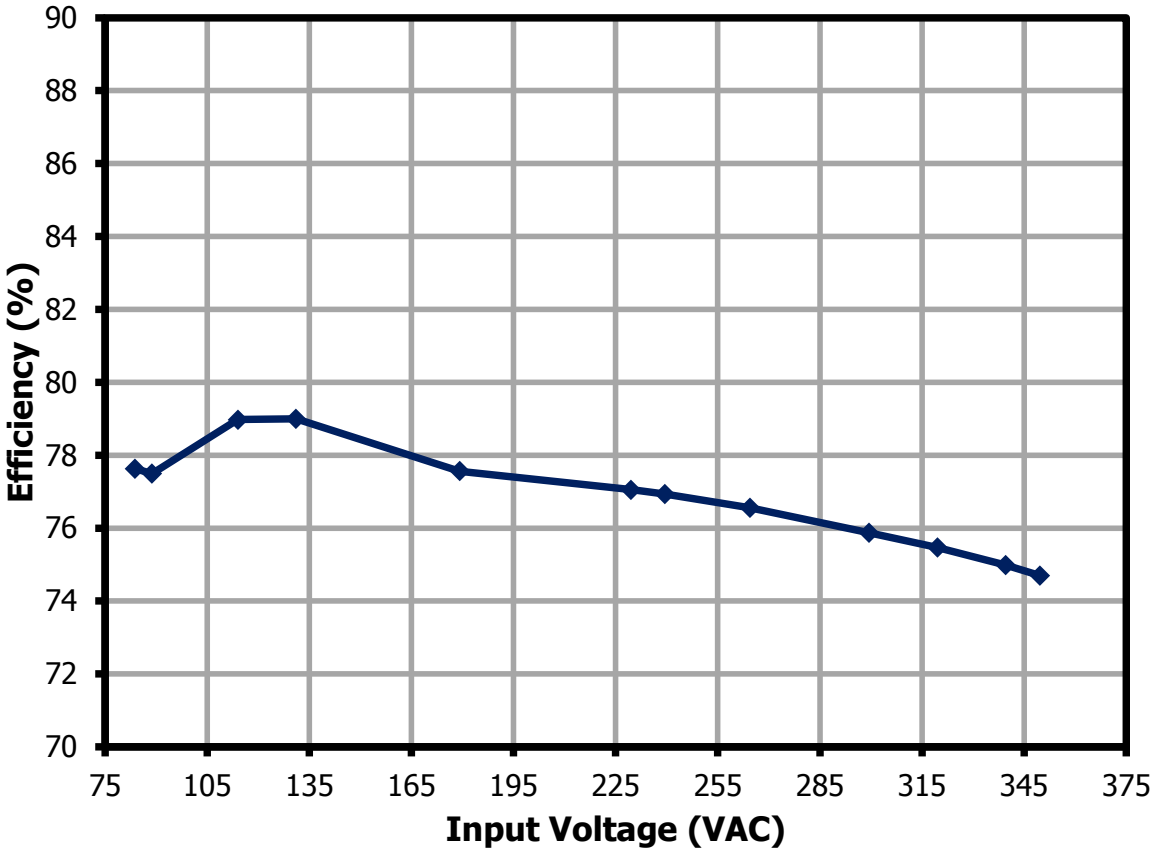


Figure 94 – Full Load Efficiency vs. Input Line Voltage.

14.3.2 *Efficiency vs Load with External Magnetizing Interference*

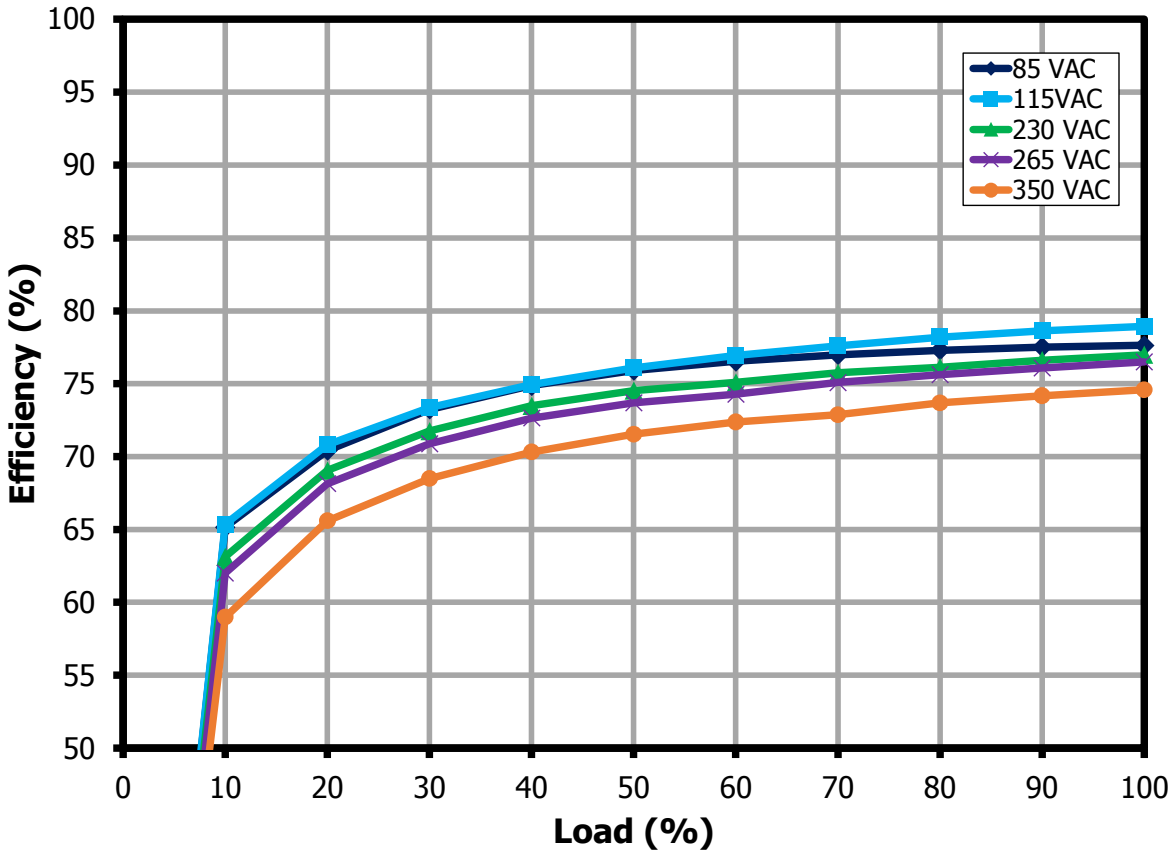


Figure 95 – Efficiency vs. Percent Load, at Different Input Line Voltages.

14.4 Output Voltage Regulation with External Magnetizing Interference

14.4.1 *16.5 V_{OUT1} Load Regulation with Balanced Load with External Magnetizing Interference*

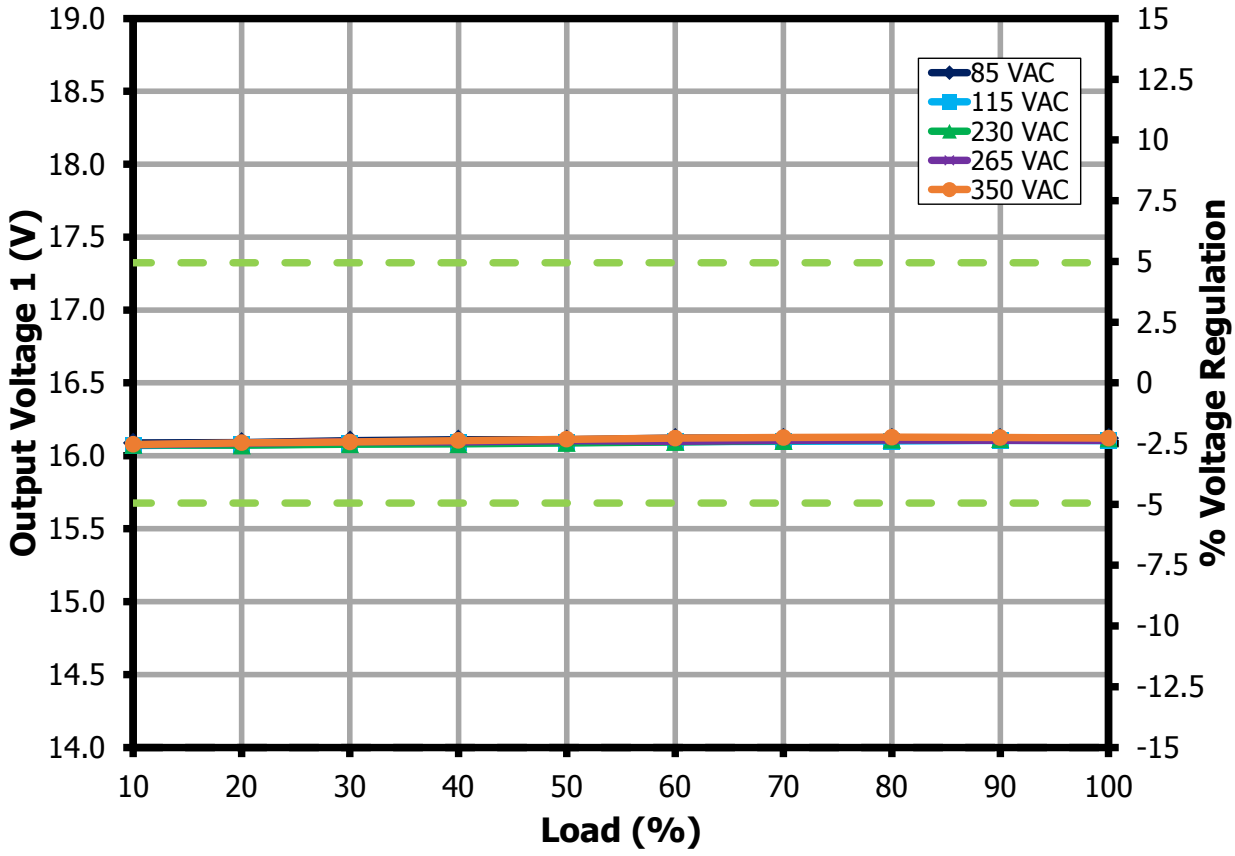


Figure 96 – 16.5 V_{OUT1} Load Regulation.
Condition: Simultaneous Load Decrement.

14.4.2 *16.5 V_{OUT2} Load Regulation with Balanced Load with External Magnetizing Interference*

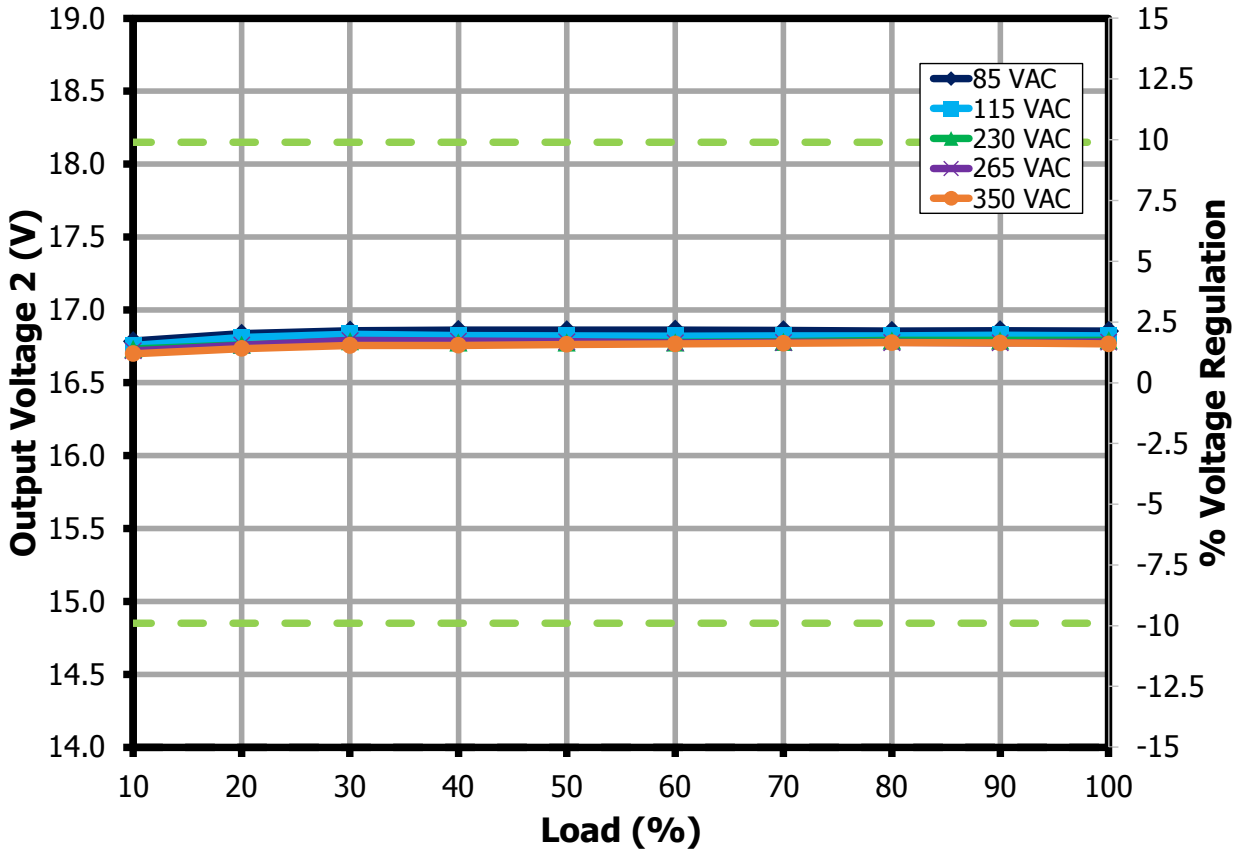


Figure 97 – 16.5 V_{OUT2} Load Regulation.
Condition: Simultaneous Load Decrement.

14.4.3 *Line Regulation with External Magnetizing Interference*

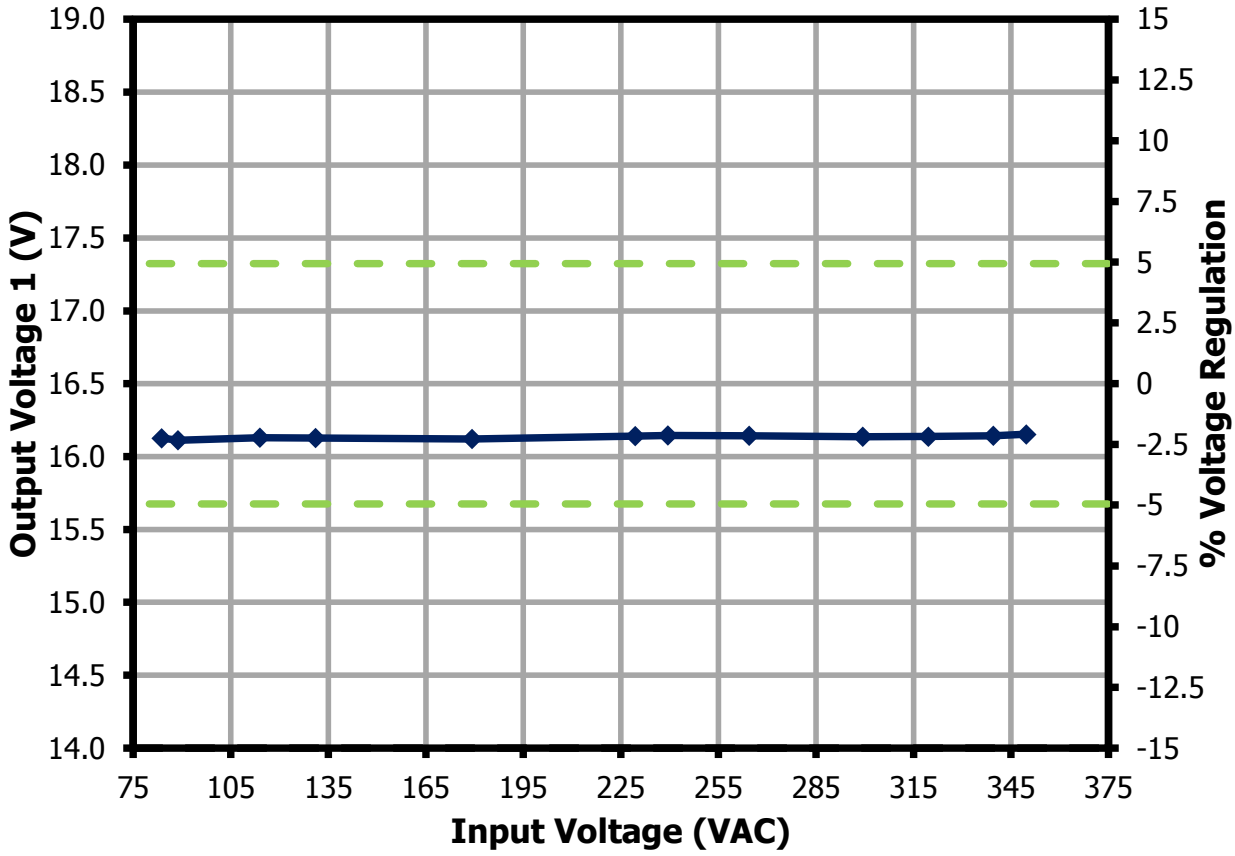


Figure 98 – 16.5 V_{OUT1} Output Regulation vs. Input Line Voltage.

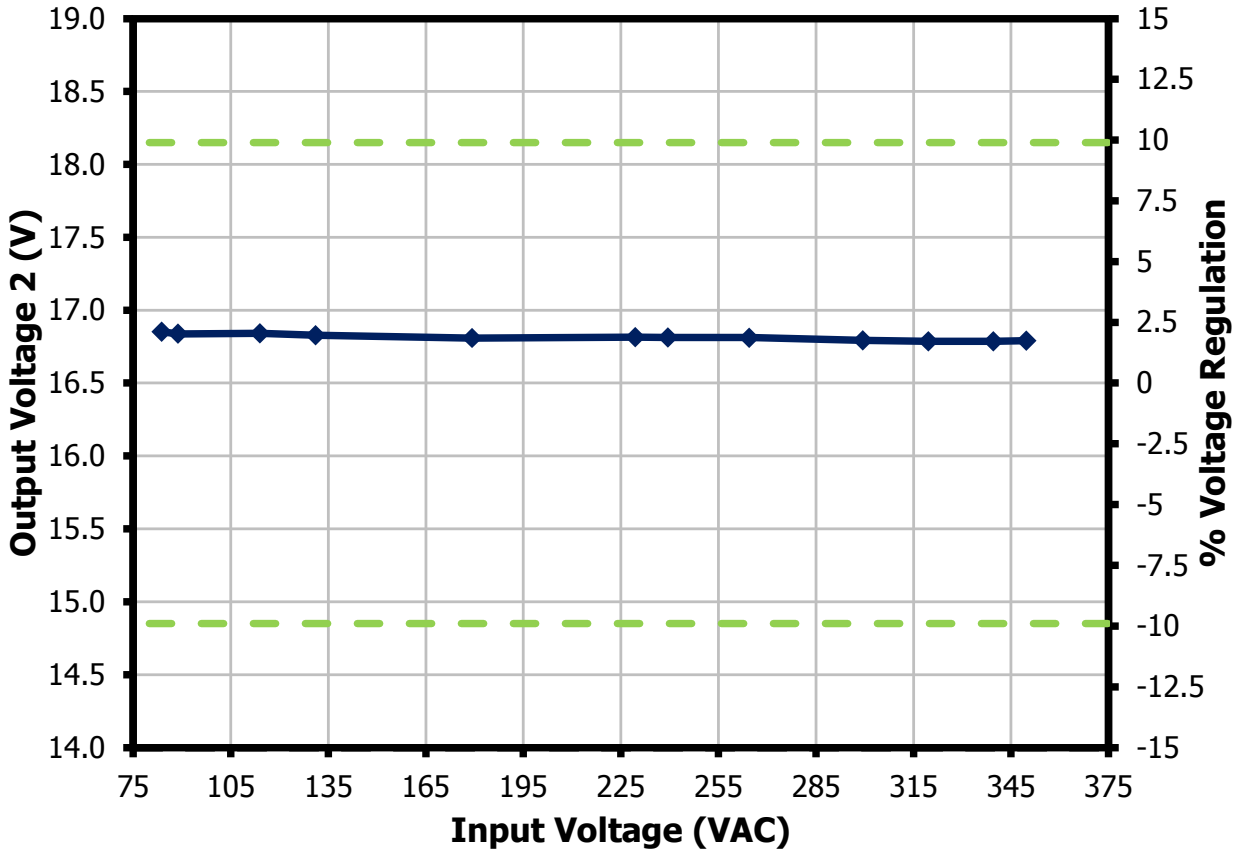


Figure 99 – 16.5 V_{OUT2} Output Regulation vs. Input Line Voltage.

14.5 Drain Current and Voltage with External Magnetizing Interference

Test conditions: 16.5 V_{OUT1} load set to CC at 300 mA, 16.5 V_{OUT2} load set to CC at 100 mA

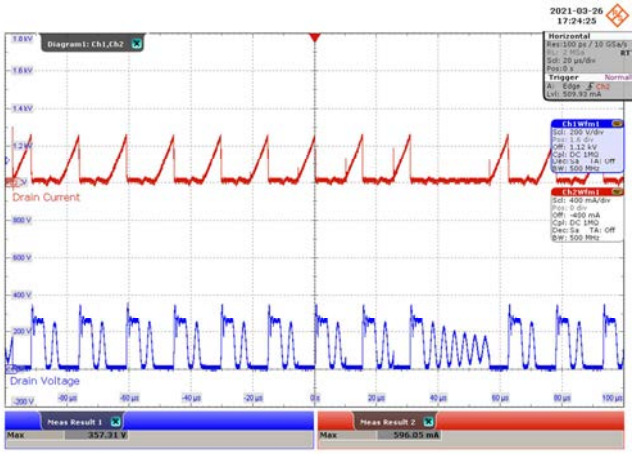


Figure 100 – 85 VAC Input.
Drain Voltage: 200 V / div., 20 µs / div.
Drain Current: 400 mA / div.
$V_{DS(MAX)}$: 357.31 V.
$I_{DS(MAX)}$: 596.05 mA.

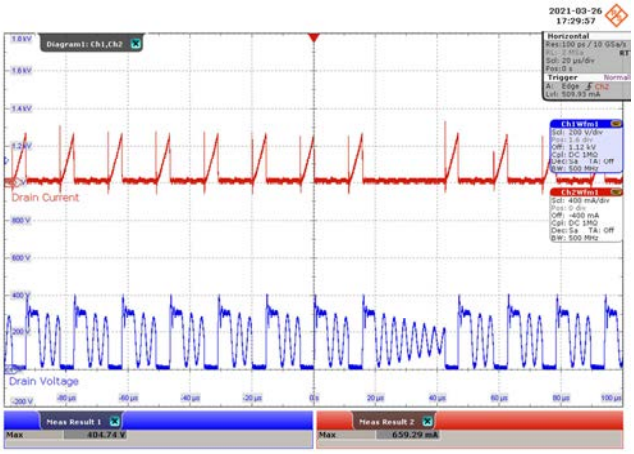


Figure 101 – 115 VAC Input.
Drain Voltage: 200 V / div., 20 µs / div.
Drain Current: 400 mA / div.
$V_{DS(MAX)}$: 404.74 V.
$I_{DS(MAX)}$: 659.29 mA.

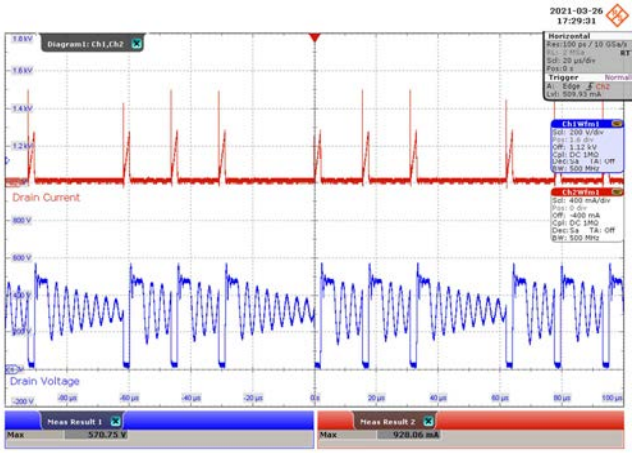


Figure 102 – 230 VAC Input.
Drain Voltage: 200 V / div., 20 µs / div.
Drain Current: 400 mA / div.
$V_{DS(MAX)}$: 570.75 V.
$I_{DS(MAX)}$: 928.06 mA.

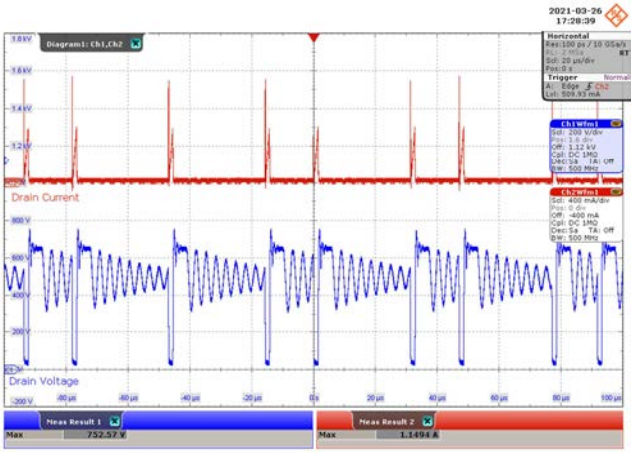


Figure 103 – 350 VAC Input.
Upper: V_{DS}, 200 V / div., 20 µs / div.
Lower: I_{DS}, 400 mA / div.
$V_{DS(MAX)}$: 752.57 V.
$I_{DS(MAX)}$: 1.1494 A.

14.6 **Start-up Performance with External Magnetizing Interference**

14.6.1 *16.5 V_{OUT1} Start-up Operation V_{IN}, V_{OUT} and I_{OUT}*

Test conditions: 16.5 V_{OUT1} load set to CR at 55 Ω, 16.5 V_{OUT2} load set to CR at 165 Ω

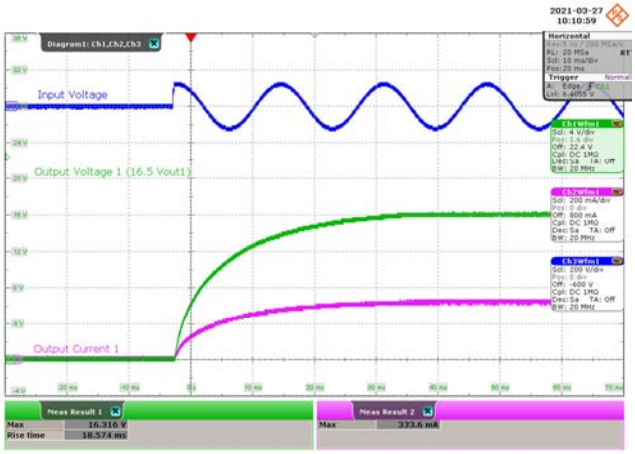


Figure 104 – 85 VAC Input.
Upper: V_{IN}, 200 V / div., 10 ms / div.
Middle: V_{OUT}, 4 V / div.
Lower: I_{OUT}, 200 mA / div.

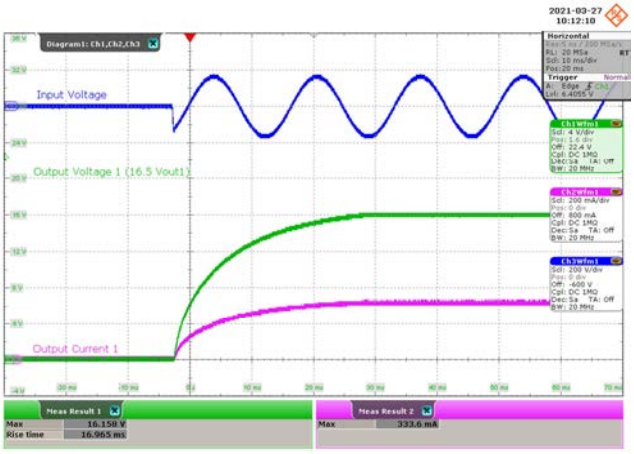


Figure 105 – 115 VAC Input.
Upper: V_{IN}, 200 V / div., 10 ms / div.
Middle: V_{OUT}, 4 V / div.
Lower: I_{OUT}, 200 mA / div.

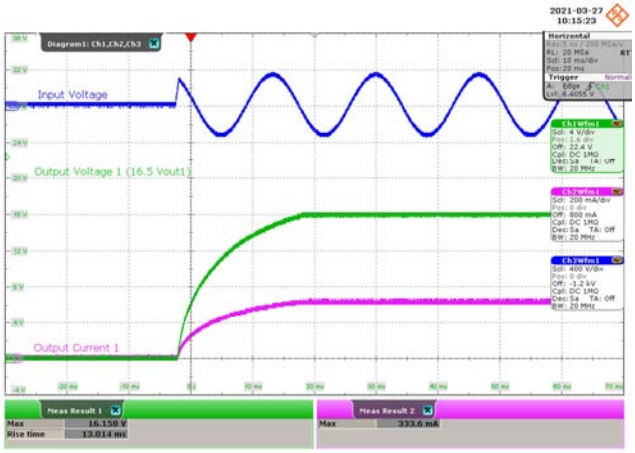


Figure 106 – 230 VAC Input.
Upper: V_{IN}, 400 V / div., 10 ms / div.
Middle: V_{OUT}, 4 V / div.
Lower: I_{OUT}, 200 mA / div.

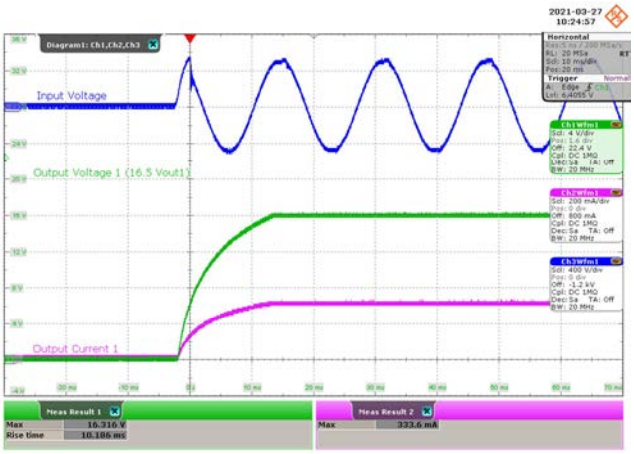


Figure 107 – 350 VAC Input.
Upper: V_{IN}, 400 V / div., 10 ms / div.
Middle: V_{OUT}, 4 V / div.
Lower: I_{OUT}, 200 mA / div.

14.6.2 *16.5 V_{OUT2} Start-up Operation V_{IN}, V_{OUT} and I_{OUT}*

Test conditions: 16.5 V_{OUT1} load set to CR at 55 Ω, 16.5 V_{OUT2} load set to CR at 165 Ω

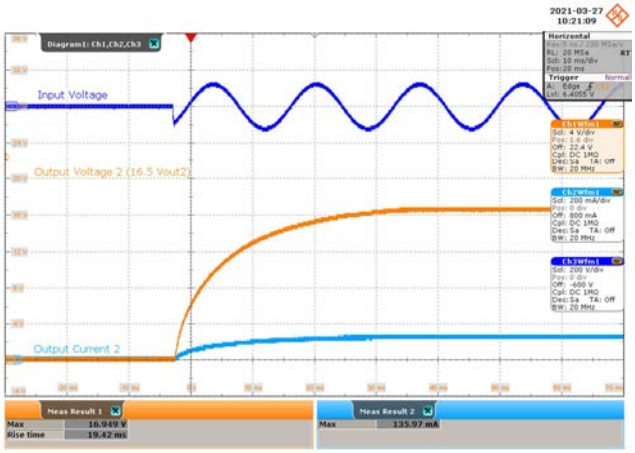


Figure 108 – 85 VAC Input.
Upper: V_{IN}, 200 V / div., 10 ms / div.
Middle: V_{OUT}, 4 V / div.
Lower: I_{OUT}, 200 mA / div.

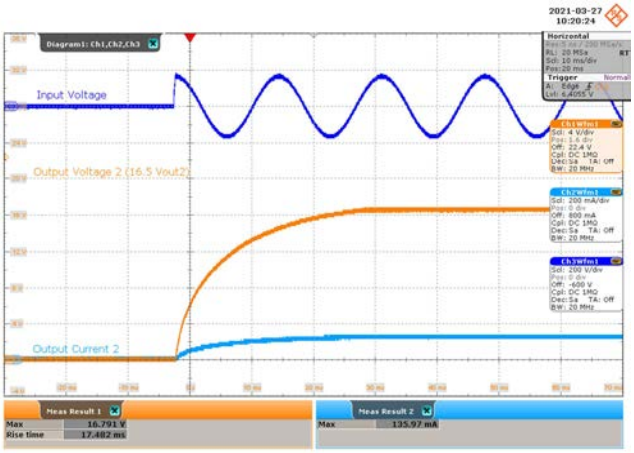


Figure 109 – 115 VAC Input.
Upper: V_{IN}, 200 V / div., 10 ms / div.
Middle: V_{OUT}, 4 V / div.
Lower: I_{OUT}, 200 mA / div.

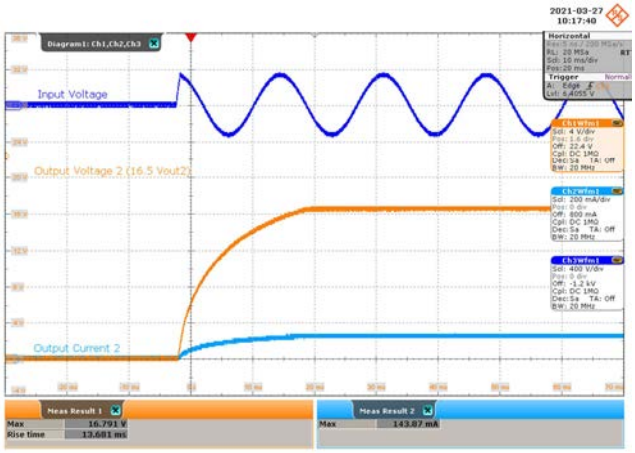


Figure 110 – 230 VAC Input.
Upper: V_{IN}, 400 V / div., 10 ms / div.
Middle: V_{OUT}, 4 V / div.
Lower: I_{OUT}, 200 mA / div.

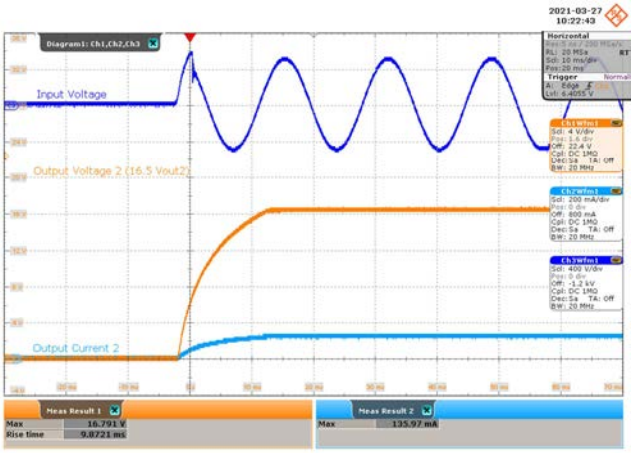


Figure 111 – 350 VAC Input.
Upper: V_{IN}, 400 V / div., 10 ms / div.
Middle: V_{OUT}, 4 V / div.
Lower: I_{OUT}, 200 mA / div.

14.6.3 *Drain Current and Drain Voltage Start-up Operation with External Magnetizing Interference*

Test conditions: 16.5 V_{OUT1} load set to CC at 300 mA, 16.5 V_{OUT2} load set to CC at 100 mA

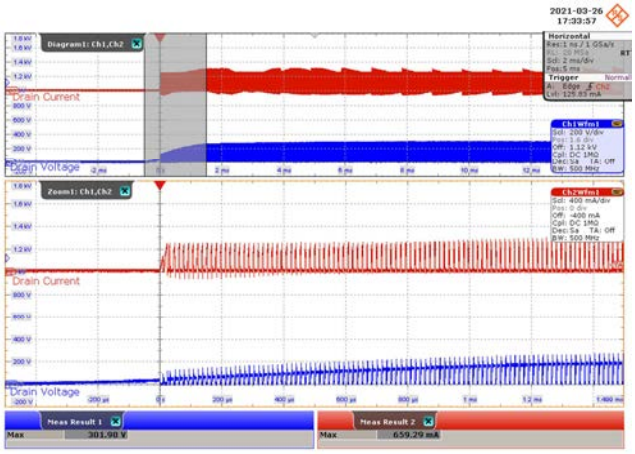


Figure 112 – 85 VAC Input.
Drain Voltage: 200 V / div., 2 ms / div.
Drain Current: 400 mA / div.
Zoom: 200 µs / div.
$V_{DS(MAX)}$: 301.98 V.
$I_{DS(MAX)}$: 659.29 mA.

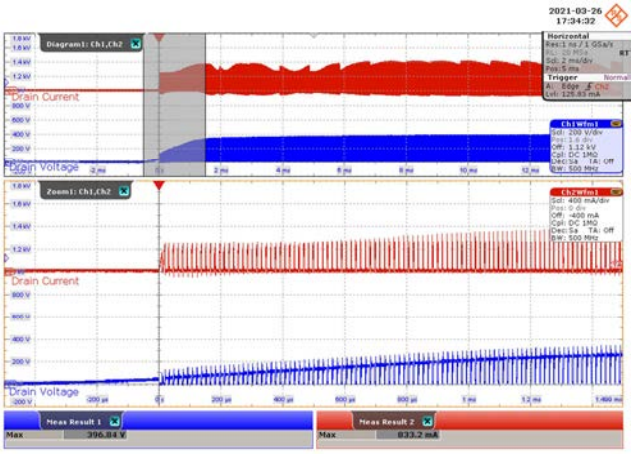


Figure 113 – 115 VAC Input.
Drain Voltage: 200 V / div., 2 ms / div.
Drain Current: 400 mA / div.
Zoom: 200 µs / div.
$V_{DS(MAX)}$: 396.84 V.
$I_{DS(MAX)}$: 833.2 mA.

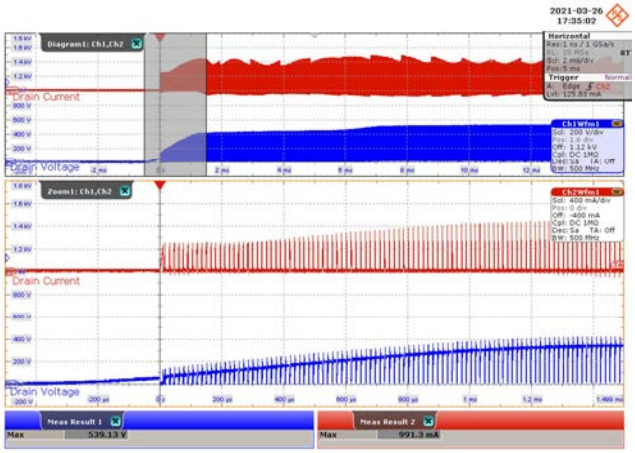


Figure 114 – 230 VAC Input.
Drain Voltage: 200 V / div., 2 ms / div.
Drain Current: 400 mA / div.
Zoom: 200 µs / div.
$V_{DS(MAX)}$: 539.13 V.
$I_{DS(MAX)}$: 991.3 mA.

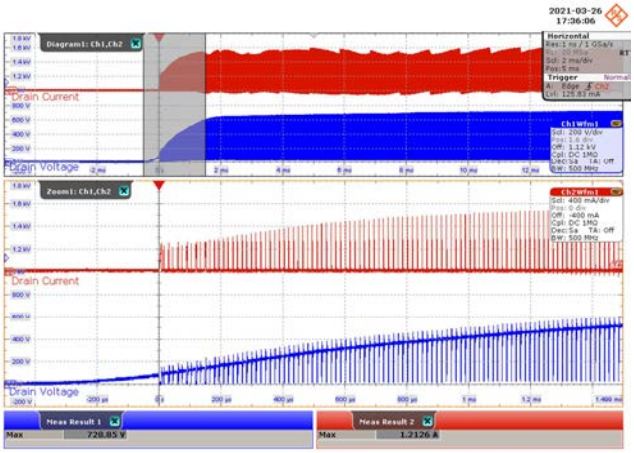


Figure 115 – 350 VAC Input.
Drain Voltage: 200 V / div., 2 ms / div.
Drain Current: 400 mA / div.
Zoom: 200 µs / div.
$V_{DS(MAX)}$: 728.85 V.
$I_{DS(MAX)}$: 1.2126 A.

14.7 Thermal Performance with External Magnetizing Interference at Room Temperature

14.7.1 *85 VAC @ Room Temperature*

Test conditions: 16.5 V_{OUT1} load set to CC at 300 mA, 16.5 V_{OUT2} load set to CC at 100 mA

LinkSwitch-XT2 900 V (U1)	Transformer (T1)	Bridge Rectifier (BR1)	Clamp Diode (D1)	16.5 V_{OUT1} Output Diode (D3)	16.5 V_{OUT2} Output Diode (D4)	Ambient Temperature
51.0 ºC	59.2 ºC	44.3 ºC	57.0 ºC	58.6 ºC	51.0 ºC	24.6 ºC

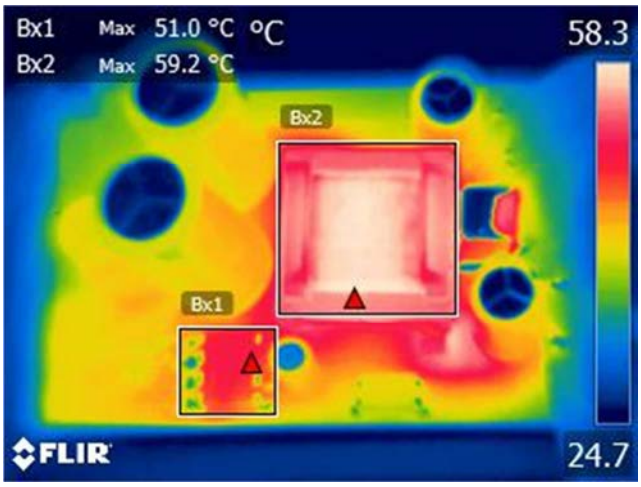


Figure 116 – Ambient = 24.7 ºC.
Bx1, U1: 51.0 ºC.
Bx2, T1: 59.2 ºC.

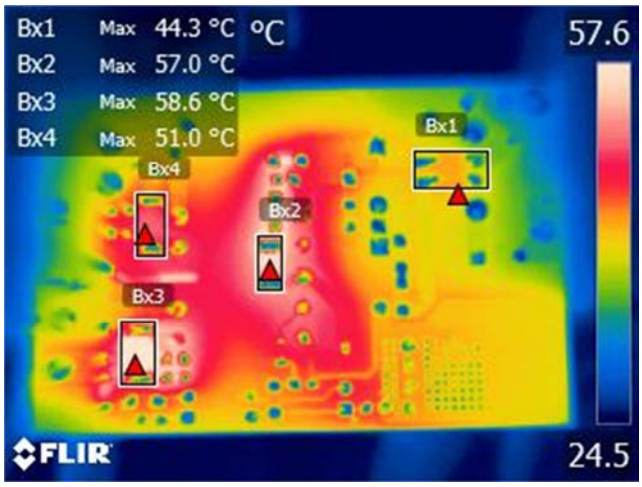


Figure 117 – Ambient = 24.5 ºC.
Bx1, BR1: 44.3 ºC.
Bx2, D1: 57.0 ºC.
Bx3, D3: 58.6 ºC.
Bx4, D4: 51.0 ºC.

14.7.2 *350 VAC @ Room Temperature*

Test conditions: 16.5 V_{OUT1} load set to CC at 300 mA, 16.5 V_{OUT2} load set to CC at 100 mA

LinkSwitch-XT2 900 V (U1)	Transformer (T1)	Bridge Rectifier (BR1)	Clamp Diode (D1)	16.5 V_{OUT1} Output Diode (D3)	16.5 V_{OUT2} Output Diode (D4)	Ambient Temperature
64.8 ºC	61.1 ºC	40.4 ºC	58.5 ºC	62.8 ºC	54.4 ºC	23.9 ºC

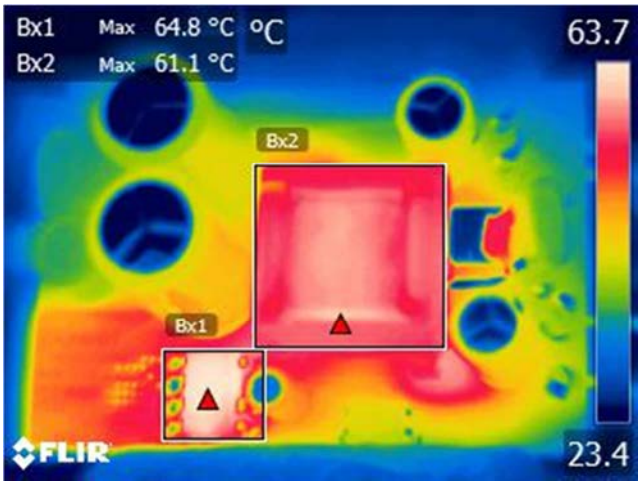


Figure 118 – Ambient = 23.4 ºC.
Bx1, U1: 64.8 ºC.
Bx2, T1: 61.1 ºC.

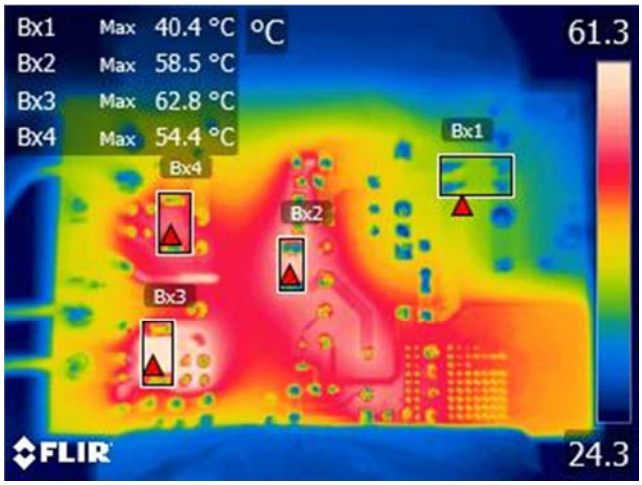


Figure 119 – Ambient = 24.3 ºC.
Bx1, BR1: 40.4 ºC.
Bx2, D1: 58.5 ºC.
Bx3, D3: 62.8 ºC.
Bx4, D4: 54.4 ºC.

14.8 **EMI with External Magnetizing Interference Test Results**

14.8.1 *115 VAC, Floating Output*

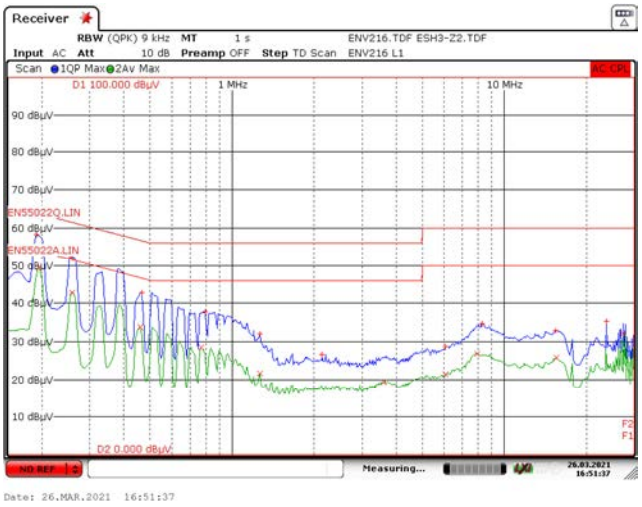


Figure 120 – Line.
Upper: Lowest Peak Delta Limit:
-5.76 dB, 190.60 kHz.
Lower: Lowest Average Delta Limit:
-4.62 dB, 195.10 kHz.

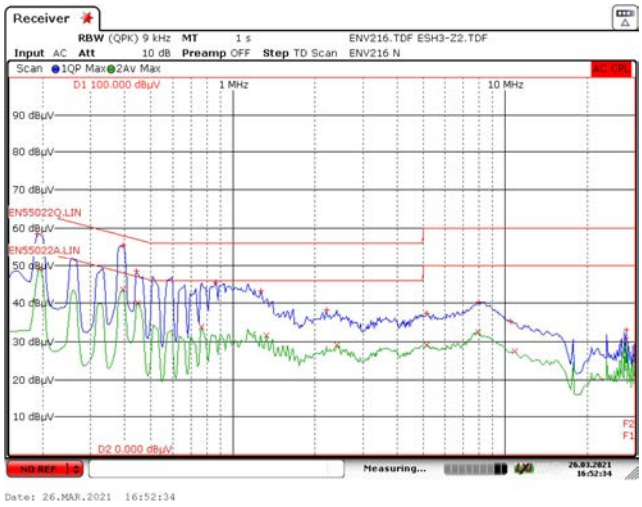


Figure 121 – Neutral.
Upper: Lowest Peak Delta Limit:
-2.60 dB, 395.35 kHz.
Lower: Lowest Average Delta Limit:
-4.42 dB, 395.35 kHz.

14.8.2 *230 VAC, Floating Output*

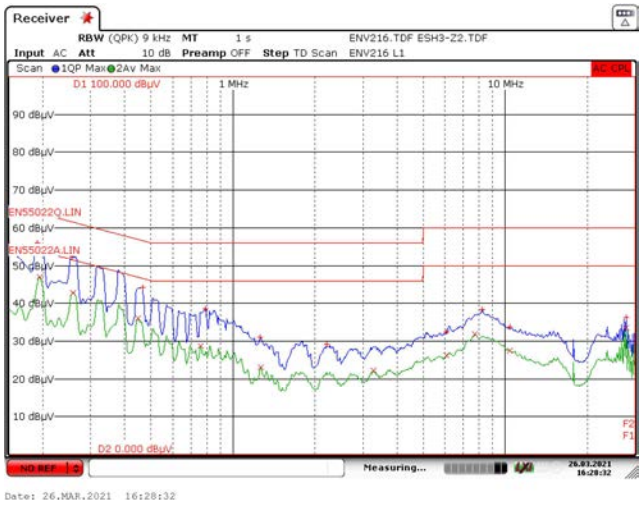


Figure 122 – Line.
Upper: Lowest Peak Delta Limit:
-7.99 dB, 190.60 kHz.
Lower: Lowest Average Delta Limit:
-6.92 dB, 195.10 kHz.

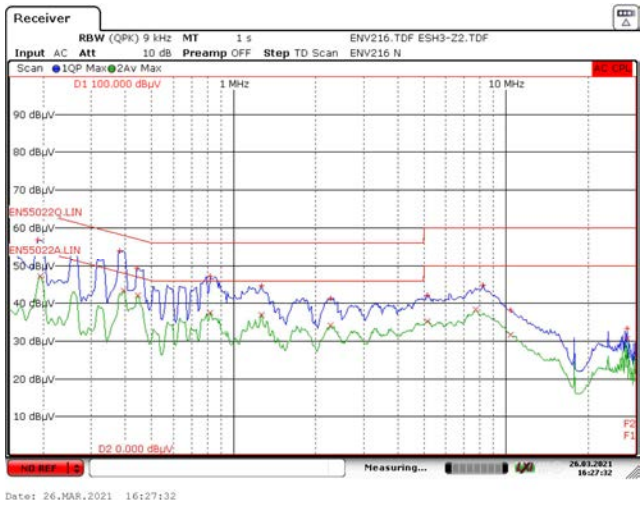


Figure 123 – Neutral.
Upper: Lowest Peak Delta Limit:
-4.26 dB, 381.85 kHz.
Lower: Lowest Average Delta Limit:
-4.55 dB, 395.35 kHz.

15 Revision History

Date	Author	Revision	Description & Changes	Reviewed
29-Apr-21	TAC	1.0	Initial Release.	Mktg & Apps
23-Jul021	KM	1.1	Minor Formatting Change	Mktg

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