SCALE™-2+ 2SC0115T
Preliminary Description & Application Manual

Dual-channel ultra-compact cost-effective SCALE™-2+ driver core

Abstract

The new cost-effective SCALE™-2+ dual-driver core 2SC0115T combines unrivalled compactness with broad applicability. The driver was designed for universal applications requiring high reliability. The 2SC0115T drives all IGBT modules up to 1400A/1200V and provides reinforced isolation between primary and either secondary sides.

The 2SC0115T is based on the SCALE-2+ chip set and offers AAC (Advanced Active Clamping) function. A high-efficient dual-channel DC/DC converter provides a secondary-side isolated voltage with +15V regulation.

The 2SC0115T is a compact driver core available for industrial applications, with a footprint of only 53.1mm x 31mm and an insertion height of 13mm. It allows even the most restricted insertion spaces to be efficiently used. The improved EMI design allows the user to place the 2SC0115T on top of an IGBT module. The 3mm long connection pins allow the use of PCBs up to 2mm thickness. Finally the 2SC0115T features an additional digital fault input and status output.

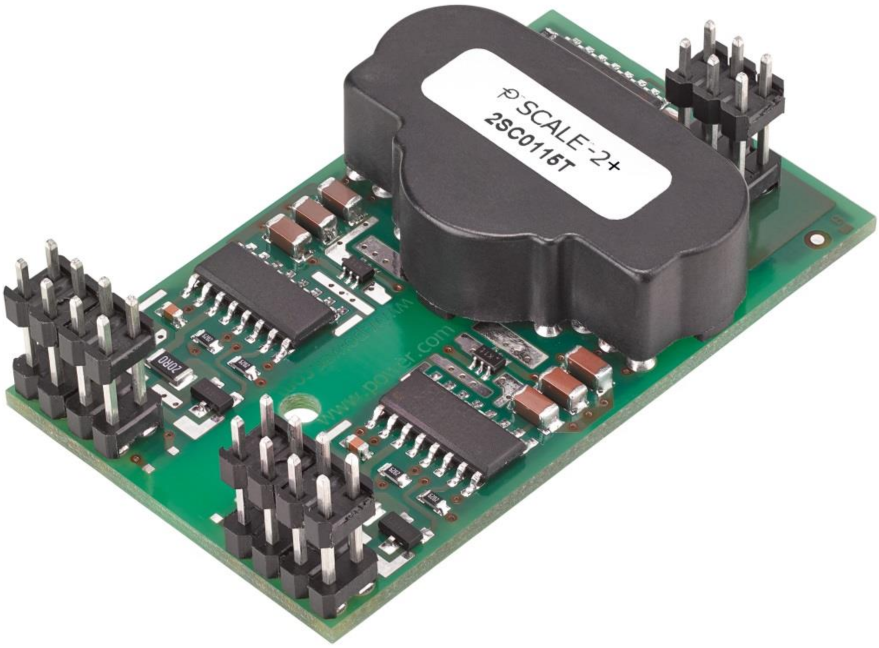

Fig. 1 2SC0115T driver core

Contents

Driver Overview

The 2SC0115T is a cost-effective driver core equipped with Power Integrations' latest SCALE-2+ chipset. The SCALE-2+ chipset consists of two application-specific integrated circuits (ASICs) that cover the main range of functions needed to design intelligent gate drivers. The driver core targets applications using 600V-1200V IGBTs such as AC drives, servo drives, UPS, PV converters, medical applications, welding, cutting and industrial EV's. The driver supports switching frequencies up to 50kHz. It comprises all functionality for an advanced dual-channel IGBT gate driver including an isolated DC/DC converter, short-circuit protection, Advanced Active Clamping, primary- and secondary-side supply-voltage monitoring.

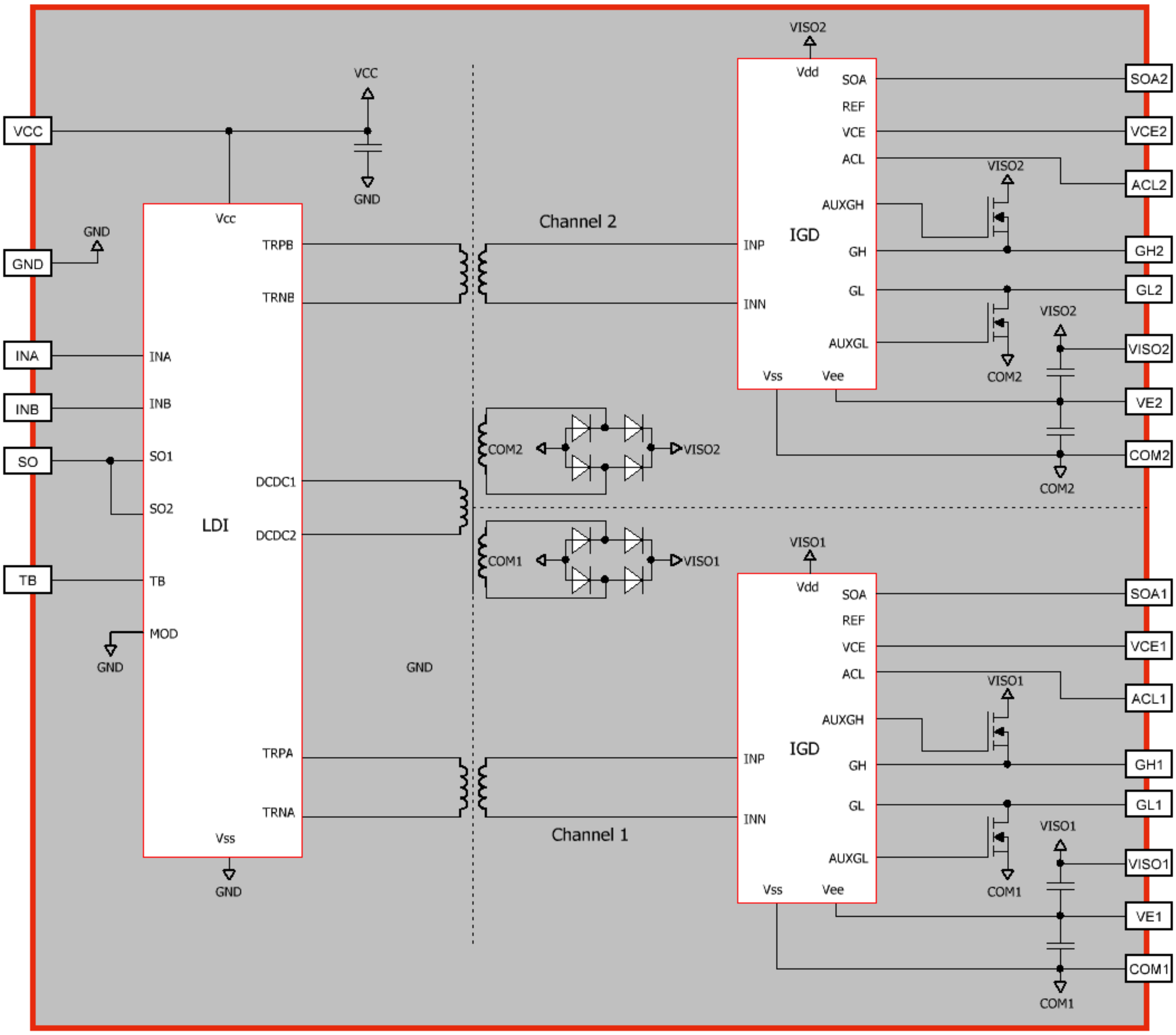

Fig. 2 Block diagram of driver core 2SC0115T

Mechanical Dimensions

The gate driver core must be mounted onto the carrier board with the transformer upside down. The header stacks must not be pressed together. The driver top side is free of components.

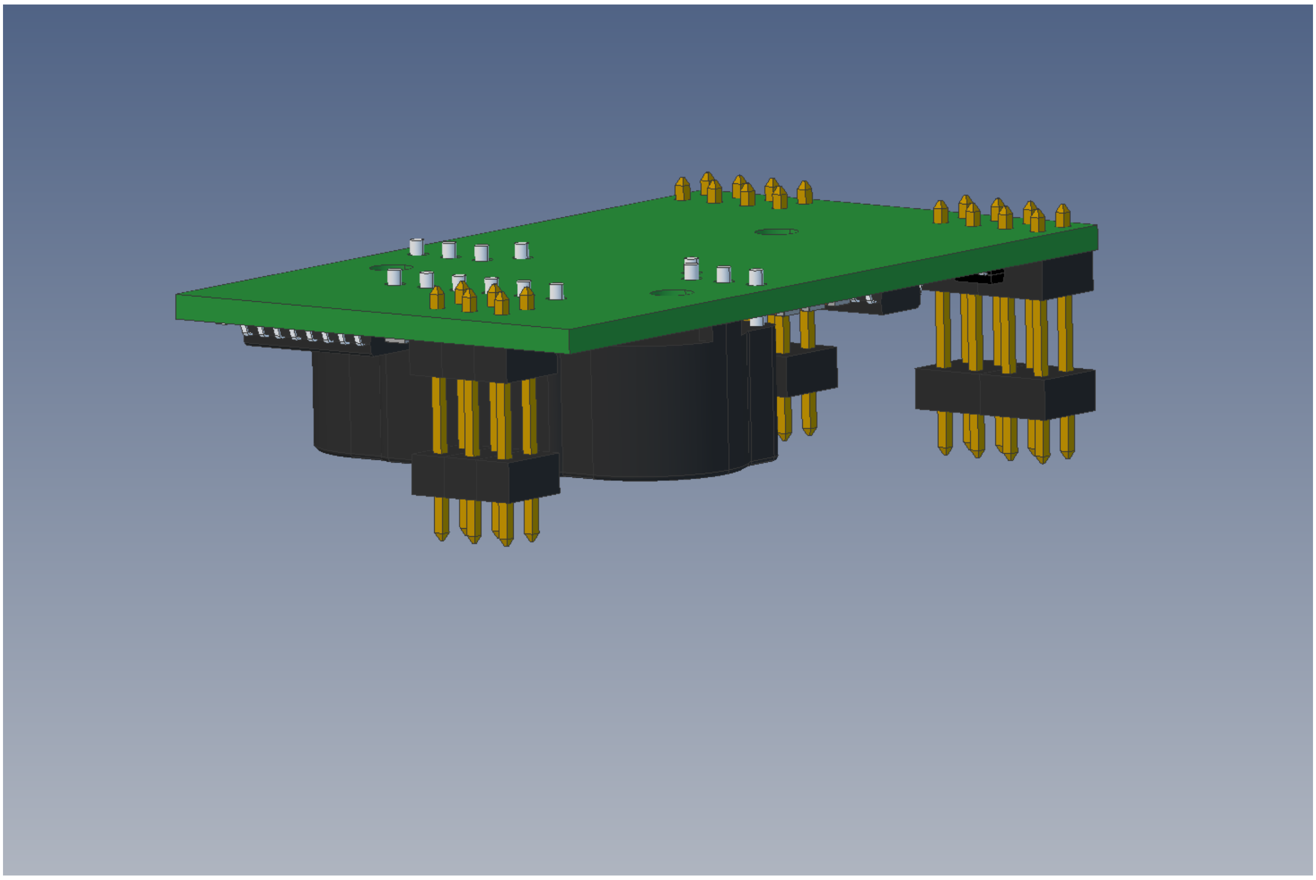

Fig. 3 Interactive 3D drawing of 2SC0115T

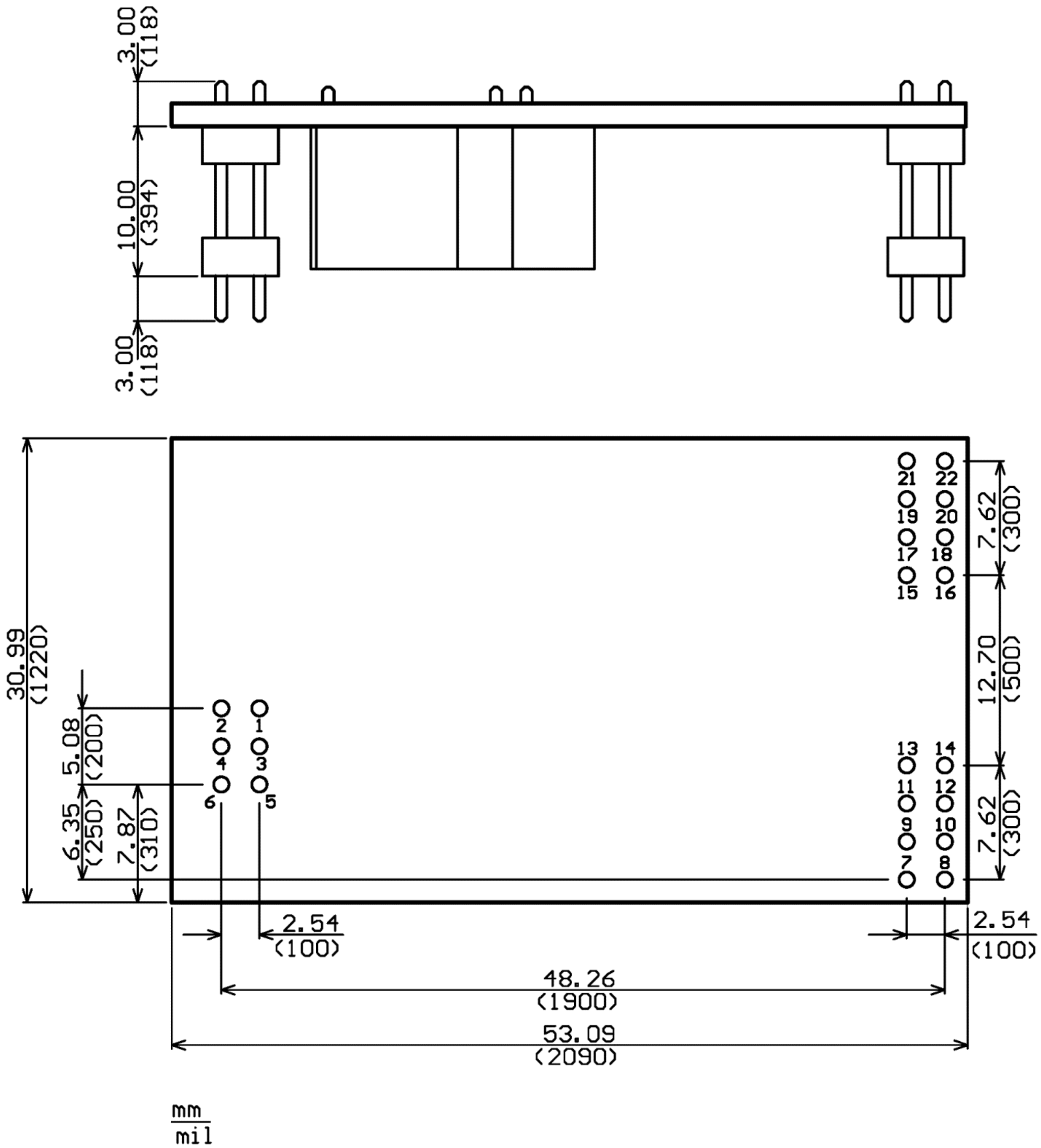

Fig. 4 Mechanical drawing of 2SC0115T (side view, top view)

The primary-side and secondary-side pin grid pitch is 2.54mm (100mil) with a pin cross section of 0.64mm x 0.64mm. Total outline dimensions of the board are 53.1mm x 31mm. The total height of the driver is 13mm measured from the bottom of the pin bodies to the maximum point of the driver.
Recommended diameter of solder pads: Ø 2mm (79mil)
Recommended diameter of drill holes: Ø 1mm (39mil)

Pin Designation

Pin No. and Name		Function
Primary Side		
1	TB	Set blocking time
2	SO	Status output channels 1 and 2 combined; normally high-impedance, pulled down to low on fault
3	VCC	Supply voltage; 15V supply for primary side
4	GND	Ground
5	INB	Signal input B (Channel 2); non-inverting input relative to GND
6	INA	Signal input A (Channel 1); non-inverting input relative to GND
Secondary Sides		
Channel 1		
7	VE1	Emitter channel 1; connect to (auxiliary) emitter of power switch
8	SOA1	Status output and external fault input channel 1; normally high-impedance
9	VISO1	DC/DC output channel 1 (referring to COM1)
10	GH1	Gate high channel 1; pulls gate high through turn-on resistor
11	VCE1	V_{CE} sense channel 1; connect to IGBT collector through resistor network
12	GL1	Gate low channel 1; pulls gate low through turn-off resistor
13	COM1	Secondary-side ground channel 1
14	ACL1	Active clamping feedback channel 1; leave open if not used
Channel 2		
15	VE2	Emitter channel 2; connect to (auxiliary) emitter of power switch
16	SOA2	Status output and external fault input channel 2; normally high-impedance
17	VISO2	DC/DC output channel 2 (referring to COM2)
18	GH2	Gate high channel 2; pulls gate high through turn-on resistor
19	VCE2	V_{CE} sense channel 2; connect to IGBT collector through resistor network
20	GL2	Gate low channel 2; pulls gate low through turn-off resistor
21	COM2	Secondary-side ground channel 2
22	ACL2	Active clamping feedback channel 2; leave open if not used

Recommended Interface Circuitry for the Primary-Side Connector

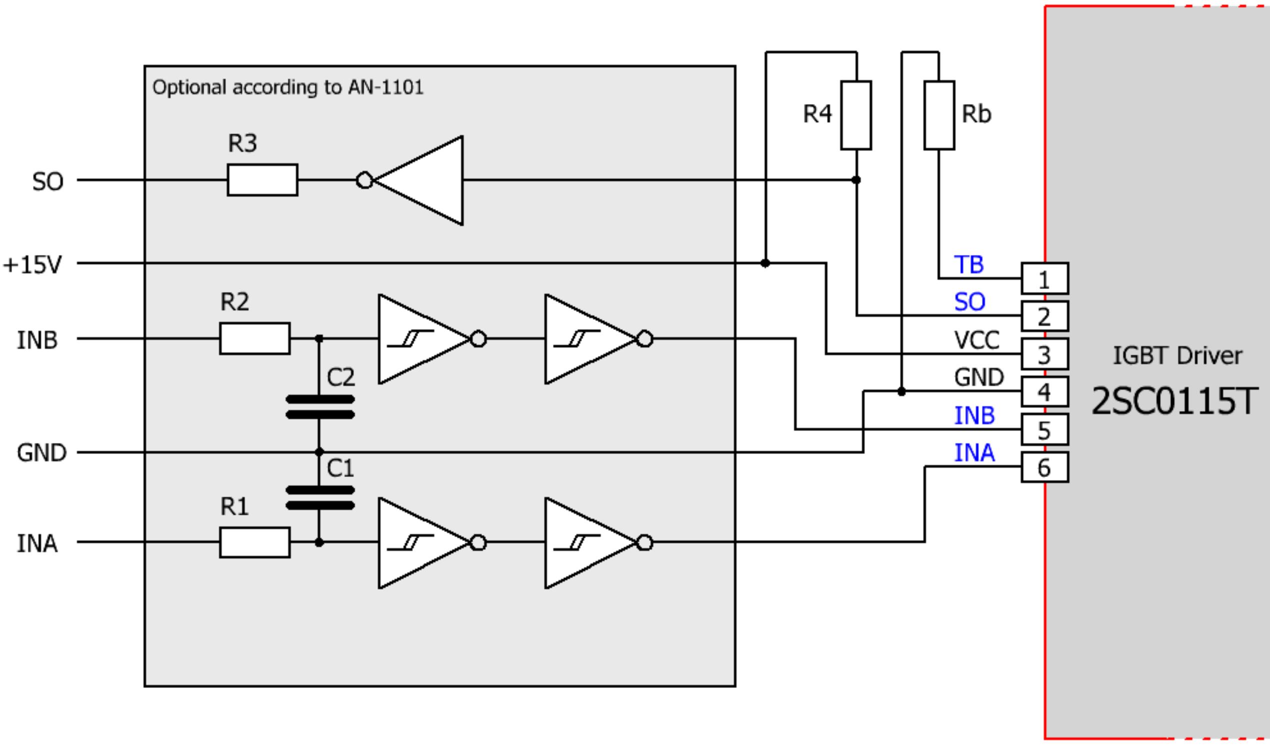

Fig. 5 Recommended user interface of 2SC0115T (primary side)

Note: 2SC0115T is an ultra-fast gate driver core. Any input noise on INA and INB with an amplitude of more than 2.6V will be transferred to a secondary-side gate switching signal. This can overload the DC/DC converter and damage the driver. The corresponding IGBTs or MOSFETs can also be damaged. Appropriate protection circuits are recommended according to the specific setup. Application note AN-1101 /1/ proposes corresponding protection circuits.

Description of Primary-Side Interface

General

The primary-side interface of the driver 2SC0115T is very simple and easy to use. The primary side is fully galvanic reinforced insulated from both secondary (high-voltage) sides. The driver channels work independently of each other.

The driver primary side is equipped with a 6-pin interface connector with the following terminals:

- 1 x power-supply terminal
- 2 x drive signal inputs
- 1 x status output (fault return)
- 1 x input to set the blocking time
- 1 x ground terminal GND

All inputs and outputs are ESD-protected. Moreover, all digital inputs have Schmitt-trigger characteristics.

VCC terminal

The driver has one VCC terminal on the interface connector. It supplies the primary-side electronics as well as the DC/DC converter to supply the secondary sides with 15V.

The driver limits the inrush current at startup and no external current limitation of the voltage source for VCC is needed for this purpose.

INA, INB (channel drive inputs, e.g. PWM)

INA and INB are drive inputs. They safely recognize signals in the whole logic-level range between 3.3V and 15V. Both input terminals feature Schmitt-trigger characteristics. An input transition is triggered at any edge of an incoming signal at INA or INB.

Note: Recommended is a 15V logic level with an additional resistor network to increase the threshold voltage and the signal to interference ratio. Application note AN-1101 /1/ proposes corresponding protection circuits.

SO (status output)

The output SO has an open-drain transistor. When no fault condition is detected, the output has high impedance. An internal current source of 1mA pulls the SO output to a voltage of about 4V when left open. When a fault condition (primary-side supply undervoltage, secondary-side supply undervoltage, IGBT short circuit) is detected, the status output SO goes to low (connected to GND).

The maximum SO current in a fault condition must not exceed the value specified in the driver data sheet /2/.

How the status information is processed

a) A fault on one of the secondary sides (detection of IGBT module short-circuit, supply undervoltage or external fault input) is immediately transmitted to the SO output. This output is automatically reset (returning to a high impedance state) after the blocking time T_b has elapsed (refer to "TB (input for adjusting the blocking time Tb)" for timing information).

b) A supply undervoltage on the primary side is indicated immediately to the SO output. This output is automatically reset (returning to a high impedance state) after the undervoltage on the primary side disappears and the blocking time T_b has elapsed. Note that the blocking time does not run fully synchronously on both channels. It is therefore possible that the blocking time of one channel has already elapsed (the channel is free) while the other channel has not yet been released (the channel is blocked) and SO is still in a fault condition. This time mismatch is typically in the range of 5% of the programmed blocking time (e.g. 6ms for a blocking time of 120ms). It is therefore recommended to wait long enough after a fault reset before applying switching impulses to ensure that both channels have been effectively released.

TB (input for adjusting the blocking time T_b)

The terminal TB allows the blocking time T_b to be set by connecting a resistor R_b to GND (Fig. 5). The following equation calculates the value of R_b connected between pins TB and GND in order to program the desired blocking time T_b (typical value):

$R_b[k\Omega] = T_b[ms] + 51$ with $20ms < T_b < 130ms$ and $71k\Omega < R_b < 181k\Omega$

The blocking time can also be set to a minimum of 9µs (typical) by selecting $R_b = 0\Omega$. Terminal TB must not be left floating.

Recommended Interface Circuitry for the Secondary-Side Connectors

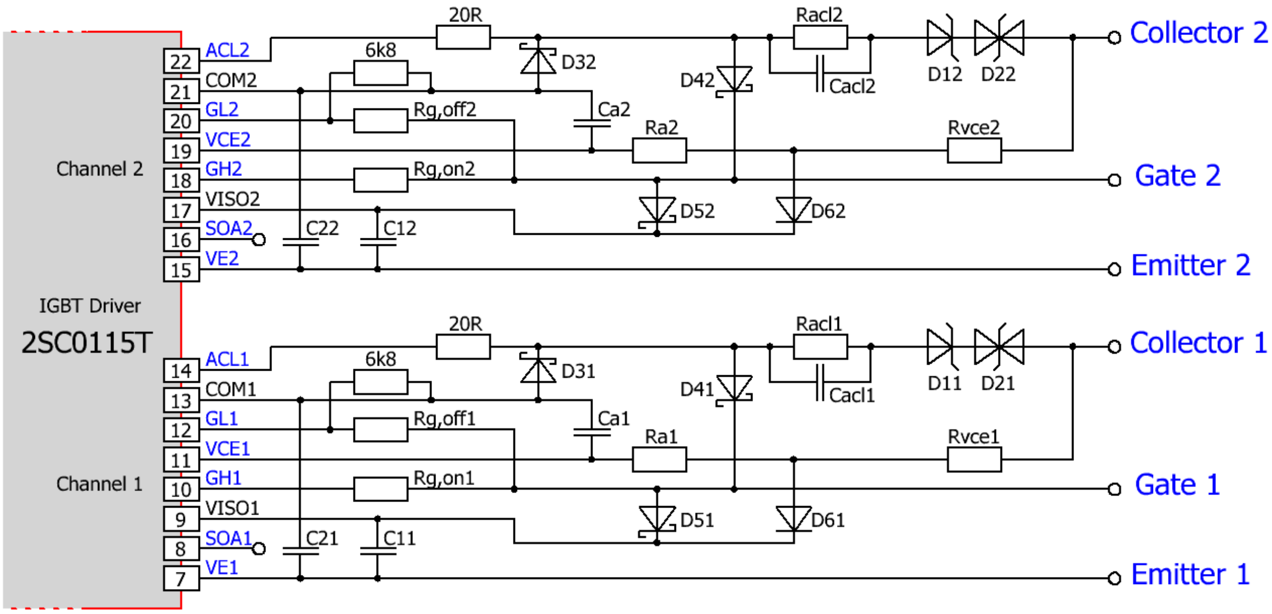

Fig. 6 Recommended user interface of 2SC0115T with Advanced Active Clamping (secondary sides)

Description of Secondary-Side Interfaces

General

Each driver's secondary side (driver channel) is equipped with an 8-pin interface connector with the following terminals (x stands for the number of the drive channel 1 or 2):

- 1 x DC/DC output terminal VISOx
- 1 x emitter terminal VEx
- 1 x secondary-side ground terminal COMx
- 1 x collector sense terminal VCEx
- 1 x active clamping terminal ACLx
- 1 x status in/out terminal SOAx
- 1 x turn-on gate terminal GHx
- 1 x turn-off gate terminal GLx

All inputs and outputs are ESD-protected.

DC/DC output (VISOx), emitter (VEx) and (COMx) terminals

The driver is equipped with blocking capacitors on the secondary side of the DC/DC converter (for values, refer to the data sheet /2/).

Power semiconductors with a gate charge of up to 3µC can be driven without additional capacitors on the secondary side. For IGBTs or MOSFETs with a higher gate charge, a minimum value of 3µF external blocking capacitance is recommended for every 1µC gate charge beyond 3µC. The blocking capacitors must be placed between VISOx and VEx (C_{1x} in Fig. 6) as well as between VEx and COMx (C_{2x} in Fig. 6). They must be connected as close as possible to the driver's terminal pins with minimum inductance. It is recommended to use the same capacitance value for both C_{1x} and C_{2x}. Ceramic capacitors with a dielectric strength ≥25V are recommended.

If the capacitances C_{1x} or C_{2x} exceed 100µF, please contact Power Integrations' support service.

No static load must be applied between VISOx and VEx, or between VEx and COMx. A static load can be applied between VISOx and COMx if necessary.

Collector sense (VCEx) with resistors

The collector sense of each channel of the 2SC0115T must be connected to the IGBT collector or MOSFET drain with the circuit shown in Fig. 6 in order to detect an IGBT or MOSFET short circuit.

- It is recommended to dimension the resistor value of R_{vcex} in order to get a current of about 0.6-1mA flowing through R_{vcex} (e.g. 800kΩ-1MΩ for $V_{DC\text{-}LINK}$=800V). The current through R_{vcex} must not exceed 1mA. It is possible to use a high-voltage resistor as well as series connected resistor. In any case, the minimum creepage distance related to the application must be considered.
- The diode D_{6x} must have a very low leakage current and a blocking voltage of >40V (e.g. BAS416). Schottky diodes must be explicitly avoided.

The reference voltage is set by an internal resistor R_{thx}=62kΩ to 9.3V. The driver will therefore safely protect the IGBT against short-circuit, but not against overcurrent. Overcurrent protection has a lower timing priority and is recommended to be realized within the host controller.

When a short-circuit fault is detected, the driver switches off the corresponding power semiconductor. The fault status is immediately transferred to the SO output. The power semiconductor is kept in the off state (non-conducting) and the fault is shown at pin SO as long as the blocking time T_b is active.

The blocking time T_b is applied independently to each channel. T_b starts as soon as a fault has been detected. As 2SC0115T drivers feature only one SO fault signal, the user cannot know from which channel a fault condition has been generated. It is therefore recommended to switch off both driver channels as soon as a fault condition is detected and to keep both driver channels in the off-state as long as a fault condition is present.

For more details about the functionality of the $V_{CE,sat}$ monitoring function and the dimensioning of the response time, refer to "V_{CE} monitoring / short-circuit protection" on page 14 and AN-1101 /1/.

Active clamping (ACLx)

Active clamping is a technique designed to partially turn on the power semiconductor as soon as the collector-emitter (drain-source) voltage exceeds a predefined threshold. The power semiconductor is then kept in linear operation.

Basic active clamping topologies implement a single feedback path from the IGBT's collector through transient voltage suppressor devices (TVS) to the IGBT gate. The 2SC0115T supports Power Integrations' Advanced Active Clamping, where the feedback is also provided to the driver's secondary side at pin ACLx: as soon as the voltage on the right side of the 20Ω resistor (Fig. 6) exceeds about 1.3V, the turn-off MOSFET is progressively switched off in order to improve the effectiveness of the active clamping and to reduce the losses in the TVS. The turn-off MOSFET is completely off when the voltage on the right side of the 20Ω resistors (Fig. 6) approaches 20V (measured to COMx).

It is recommended to use the circuit shown in Fig. 6. The following parameters must be adapted to the application:

- TVS D_{1x}, D_{2x}. It is recommended to use:

  - Six 80V TVS with 600V IGBTs with DC-link voltages up to 430V. Good clamping results can be obtained with five unidirectional TVS SMBJ70A-E3 and one bidirectional TVS SMBJ70CA-E3 from Vishay.

  - Six 150V TVS with 1200V IGBTs with DC-link voltages up to 800V. Good clamping results can be obtained with five unidirectional TVS SMBJ130A-E3 and one bidirectional TVS SMBJ130CA-E3 from Vishay or five unidirectional TVS SMBJ130A-TR from ST and one bidirectional TVS P6SMBJ130CA from Diotec.

  At least one bidirectional TVS (D_{2x}) per channel must be used in order to avoid negative current flowing through the TVS chain during turn-on of the antiparallel diode of the IGBT module due to its forward recovery behavior. Such a current could, depending on the application, lead to undervoltage of the driver secondary voltage VISOx to VEx (15V).

  Note that it is possible to modify the number of TVS in a chain. The active clamping efficiency can be improved by increasing the number of TVS used in a chain if the total threshold voltage remains at the same value. Note also that the active clamping efficiency is highly dependent on the type of TVS used (e.g. manufacturer).

- R_{aclx} and C_{aclx}: These parameters allow the effectiveness of the active clamping as well as the losses in the TVS and the IGBT to be optimized. It is recommended to determine the value with measurements in the application. Typical values are: R_{aclx}=0…150Ω and R_{aclx}*C_{aclx}=100ns…500ns. R_{aclx}=0Ω is recommended to improve the effectiveness of active clamping.

- D_{3x}, D_{4x} and D_{5x}: It is recommended to use Schottky diodes with blocking voltages >35V (>1A depending on the application).

Please note that the 20Ω resistor as well as diodes D_{3x}, D_{4x} and D_{5x} must not be omitted if AAC is used. If AAC is not used, the 20Ω resistor as well as diodes D_{3x} and D_{4x} can be omitted.

Application note AN-1302 /3/ gives information about Dynamic Advanced Active Clamping (DA^2C) which allows increasing the DC-link voltage to higher values in non-switching off-state condition.

Gate turn-on (GHx) and turn-off (GLx) terminals

These terminals allow the turn-on (GHx) and turn-off (GLx) gate resistors to be connected to the gate of the power semiconductor. The GHx and GLx pins are available as separated terminals in order to set the turn-on and turn-off resistors independently without the use of an additional diode. Please refer to the driver data sheet /2/ for the limit values of the gate resistors used.

A resistor between GLx and COMx of 6.8kΩ (other values are also possible) may be used in order to provide a low-impedance path from the IGBT/MOSFET gate to the emitter/source even if the driver is not supplied with power. No static load (e.g. resistors) must be placed between GLx and the emitter terminal VEx.

Gate clamping and STO (Safe Torque Off)

Gate driver core 2SC0115T provides a regulated 15V supply voltage on the VISOx terminal. Schottky diode D_{5x} according to Fig. 6 clamps the gate voltage to the regulated 15V.

This has the following advantages:

- The use of an additional transient voltage suppressor (TVS) between gate and emitter is not required.
- Reduction of the dissipated energy in the power semiconductor in case of short circuit due to better clamping performance of the gate-emitter voltage. The short circuit energy is a function of the gate-emitter voltage: a lower gate-emitter voltage results in a lower short-circuit current.
- STO function by unpowered driver core. In case of any dv/dt coming from the DC-bus system, which causes a current flow through the Miller capacitance of the IGBT, the diode D_{5x} provides a conducting path for this current to the buffer capacitors. This prevents an unintended turn-on of the IGBT even if the gate-driver is unpowered.

Recommended Schottky diodes for D_{5x} include PMEG4010CEJ or STPS340U.

SOAx (Status feedback output and external fault input channel)

The SOAx terminal can be used as a status feedback output and/or as an external fault input. When SOAx is externally shorted to COMx for a minimum period of time (timing and threshold values according to the driver data sheet /2/), the driver detects an external fault. The IGBT is then turned off immediately. Note that failure to respect the minimum hold time may lead to incorrect driver behavior.

The recommended circuitry for using the SOAx terminal as a status feedback output and as an external fault input is shown in Fig. 7.

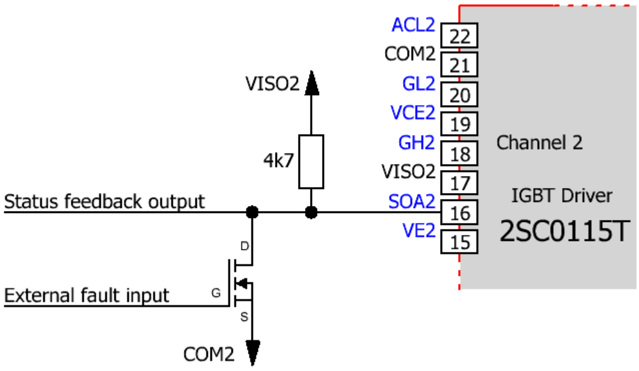

Fig. 7 Recommended secondary-side circuit for SOAx terminal (example with channel 2)

In normal operation, each edge of the control signal INx is acknowledged by the driver with a short pulse as shown in Fig. 8 (SOAx is switched to low for a short period of time; refer to driver data sheet /2/ for details).

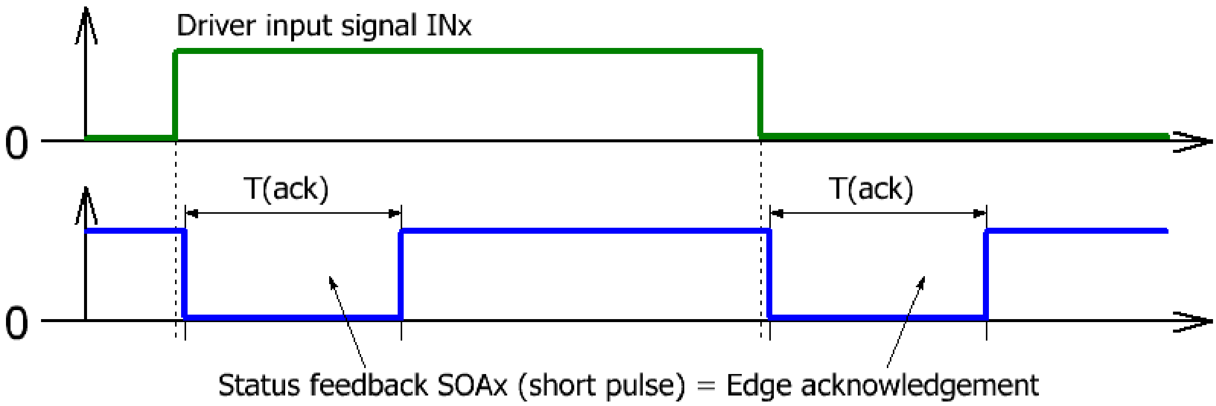

Fig. 8 Edge acknowledge on SOAx signal

The following driver channel fault conditions are also shown on the SOAx signal:

- V_{CE} desaturation detection in case of a short circuit: the SOAx signal is pulled to COMx for a period of ~9µs after the response time.
- Secondary-side supply undervoltage: the SOAx signal is pulled to COMx as long as the undervoltage fault remains. Note that during power-up, the status feedback SOAx will also show a fault condition until the supply undervoltage disappears.
- External fault (as described above)

Note that the SOAx terminal basically has the secondary-side potential of the corresponding channel. It must be isolated from the primary-side potential and from the secondary-side potential of the other channel.

If the SOAx terminal is not used, it can be left open or can be connected to VISOx via a pull-up resistor in the range from 1.5kΩ to 10kΩ.

How Do 2SC0115T SCALE-2+ Drivers Work in Detail?

Power supply and electrical isolation

The driver is equipped with a DC/DC converter to provide an electrically insulated power supply to the gate driver circuitry. All transformers (DC/DC and signal transformers) feature reinforced isolation to IEC 60664-1 between the primary side and either secondary side.

Note that the driver requires a stabilized supply voltage.

Power-supply monitoring

The driver's primary-side as well as both secondary-side driver channels are equipped with a local undervoltage monitoring circuit.

In the event of a primary-side supply undervoltage, the power semiconductors are driven with a negative gate voltage to keep them in the off-state (the driver is blocked) and the fault is transmitted to output SO until the fault disappears (refer also to "SO (status output)" for more details).

In case of a secondary-side supply undervoltage, the corresponding power semiconductor is driven with a negative gate voltage to keep it in the off-state (the channel is blocked) and a fault condition is transmitted to the SO output. The SO output is automatically reset (returning to a high impedance state) after the blocking time.

V_{CE} monitoring / short-circuit protection

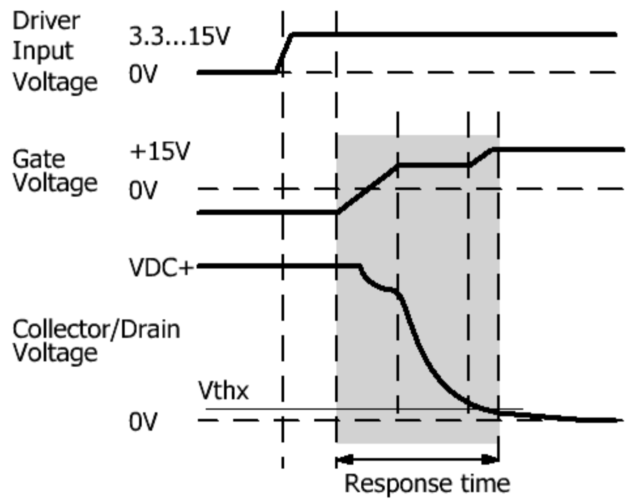

Fig. 9 Turn-on characteristic of an IGBT or MOSFET

Each channel of the 2SC0115T driver is equipped with a V_{CE} monitoring circuit. The recommended external circuitry is shown in Fig. 6. The turn-off threshold is internally set to V_{thx}=9.3V. In this case the driver will safely protect the IGBT against short-circuit, but not necessarily against overcurrent. Overcurrent protection has a lower timing priority and is recommended to be realized within the host controller.

In order to ensure that the 2SC0115T can be applied as universally as possible, the response time capacitor C_{ax} is not integrated in the driver, but must be connected externally.

During the response time, the V_{CE} monitoring circuit is inactive. The response time is the time that elapses after turn-on of the power semiconductor until the collector/drain voltage is measured (Fig. 9).

Both IGBT collector-emitter voltages are measured individually. V_{CE} is checked after the response time at turn-on to detect a short circuit. If the measured V_{CE} at the end of the response time is higher than the threshold V_{thx}, the driver detects a short circuit. The driver then switches off the corresponding power semiconductor. The fault status is immediately transferred to the SO output. The power semiconductor is kept in off-state (non-conducting) and the fault is shown at pin SO as long as the blocking time T_b is active.

The blocking time T_b is applied independently to each channel. T_b starts as soon as V_{CE} exceeds the threshold of the V_{CE} monitoring circuit outside the response time span.

The value of the response time capacitors C_{ax} can be determined with the following table in order to set the desired response time (R_{vcex}=1MΩ, R_{ax}=120kΩ, DC-link voltage $V_{DC-LINK}$>550V):

C_{ax} [pF]	Response time [µs]
15	4.5
22	5.9
27	6.9
33	8.2
47	11.2

Table 1 Typical response time as a function of the capacitance C_{ax}

As the parasitic capacitances on the host PCB may influence the response time, it is recommended to measure this in the final design. It is important to define a response time which is shorter than the maximum permitted short-circuit duration of the power semiconductor.

Note that the response time increases at DC-link voltage values lower than 500V (R_{ax}=120kΩ).

Desaturation protection with sense diodes

If desaturation protection with sense diodes is required with 2SC0115T, please refer to the application note AN-1101 /1/.

Note that the reference voltage is set by an internal resistor R_{thx}=62kΩ to 9.3V.

Additional application support for 2SC0115T

For additional application support using 2SC0115T drivers, please refer to Application Note AN-1101 /1/.

Bibliography

/1/ Application Note AN-1101: Applications with SCALE™-2 and SCALE™-2+ Gate Driver Cores, Power Integrations

/2/ Data sheets SCALE™-2+ driver core 2SC0115T, Power Integrations

/3/ Application Note AN-1302: Dynamic Advanced Active Clamping (DA2C), Power Integrations

Note: These documents are available at www.power.com/igbt-driver.

The Information Source: SCALE-2+ Driver Data Sheets

Power Integrations offers the widest selection of gate drivers for power MOSFETs and IGBTs for almost any application requirements. The largest website on gate-drive circuitry anywhere contains all data sheets, application notes and manuals, technical information and support sections: www.power.com/igbt-driver.

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Type Designation	Description
2SC0115T2A0-12	SCALE-2+ driver core

Product home page: www.power.com/igbt-driver/go/2SC0115T
Refer to www.power.com/igbt-driver/go/nomenclature for information on driver nomenclature.

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