

Design Example Report

Title	<i>12 W Power Factor Corrected (Valley Fill) Non-Dimmable Isolated Flyback; Constant Voltage (24 V) LED Driver Using TinySwitch™-4 TNY286PG</i>
Specification	Input: 190 VAC – 265 VAC (47 – 63 Hz); Output: 24 V, 500 mA _{CONT}
Application	Ballast LED Driver
Author	Applications Engineering Department
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Revision	1.0

Summary and Features

- EcoSmart™ – Meets all existing and proposed harmonized energy efficiency standards
 - CECP (China), CEC, EPA, AGO, European Commission
- No-load consumption <100 mW at 230 VAC
- >80% active-mode efficiency
- Tightly toleranced I²f parameter (-10%, +12%) reduces system cost
 - Increases MOSFET and transformer power delivery
 - Reduces overload power, lowering output diode and capacitor costs
- Integrated TinySwitch-4 safety/reliability features
 - Accurate (±5%), auto-recovering, hysteretic thermal shutdown function maintains safe PCB temperatures under all conditions
 - Auto-restart protects against output short circuit and open loop fault conditions
 - >3.2 mm creepage on package enables reliable operation in high humidity and high pollution environments
- Meets EN550022 ,EN55015 and CISPR-22 Class B conducted EMI

Power Integrations

5245 Hellyer Avenue, San Jose, CA 95138 USA.

Tel: +1 408 414 9200 Fax: +1 408 414 9201

www.powerint.com

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Important Note:

Although this board is designed to satisfy safety isolation requirements, the engineering prototype has not been agency approved. Therefore, all testing should be performed using an isolation transformer to provide the AC input to the prototype board.



1 Introduction

This document is an engineering report describing a 12 W power supply utilizing a TNY286PG from the TinySwitch-4 product Family. This power supply was specifically targeted to meet a LED ballast application however it may also be used as a general evaluation platform.

The document contains the power supply specification, schematic, bill of materials, transformer documentation, printed circuit layout, and performance data.

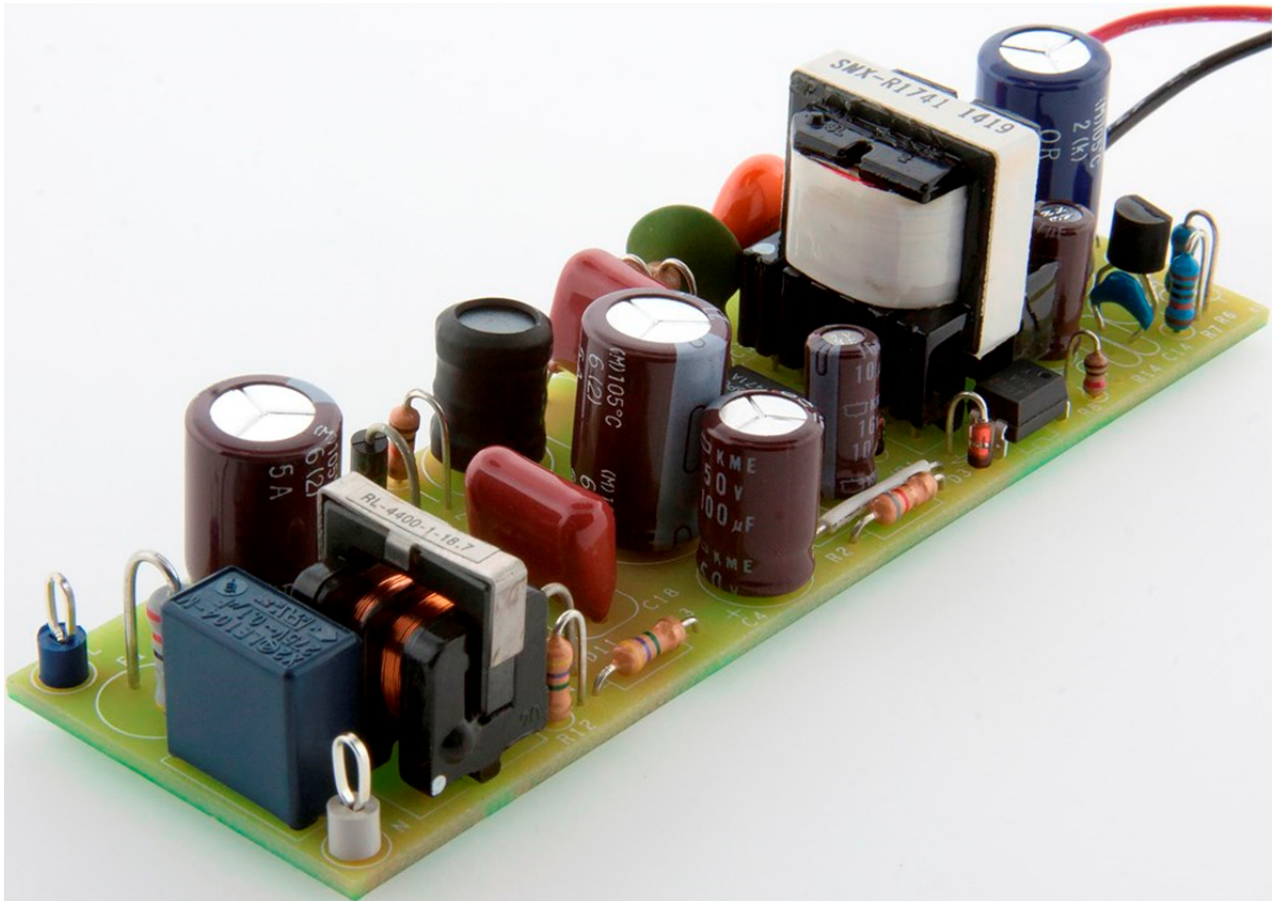


Figure 1 – Populated Circuit Board Photograph.

2 Power Supply Specification

The table below represents the minimum acceptable performance of the design. Actual performance is listed in the results section.

Description	Symbol	Min	Typ	Max	Units	Comment
Input						
Voltage	V_{IN}	190		265	VAC	2 Wire – no P.E. 269 V; 50 Hz – No damage will occur to the PSU nor should the fuse open
Frequency	f_{LINE}	47	50/60	63	Hz	
No-load Input Power (230 VAC)				0.1	W	
In-rush Current (Cold start)	I_{RUSH}					
Output						
Output Voltage	V_{OUT}	22	24	26	V	± 5%
Output Ripple Voltage	V_{RIPPLE}			1	V	Peak to peak, 20 MHz bandwidth-measured with 180 μ F, 0.1 μ F and 1 μ F ceramic capacitor
Total Output Power						
Continuous Output Power	P_{OUT}			12	W	
Efficiency						
Required Average Efficiency at 25, 50, 75 and 100 % of P_{OUT}	η_{AVE}	80			%	Per Energy Star test method
Environmental						
Conducted EMI		Meets CISPR22B / EN55022B/FCC Part 15				6 dBuV margin with grounded and ungrounded chassis
Safety		Designed to meet IEC950 / UL1950 Class II				
Leakage Current	I_{LEAK}	0.25 mA				Measured at 265 V_{RMS} , 50/60 Hz
Line Surge						IEC 61000-4-5/EN5504, 500 A short-circuit Series Impedance: Differential Mode: 2 Ω Common Mode: 12 Ω
Differential Mode (L1-L2)				1	kV	
Common mode (L1/L2-PE)				2.5	kV	
Ring Wave (100 kHz)						
Differential Mode (L1-L2)				2.5	kV	
Common Mode (L1/L2-PE)					kV	
Ambient Temperature	T_{AMB}	0		40	°C	Free convection, sea level



3 Schematic

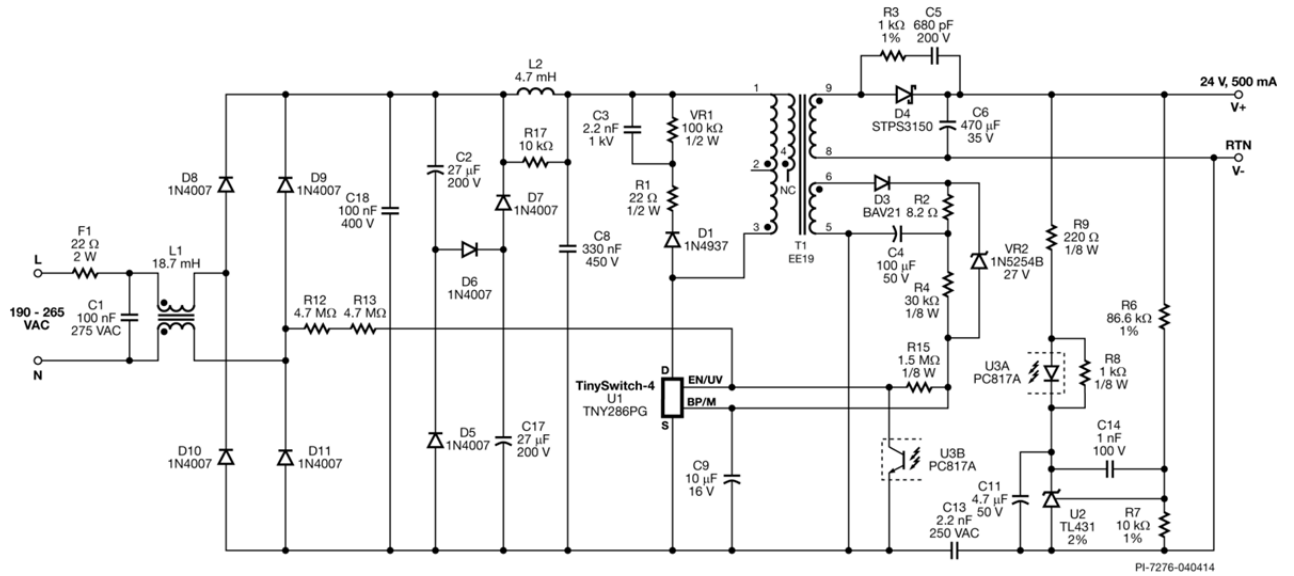


Figure 2 – Schematic.



4 Circuit Description

This circuit is designed for an LED ballast driver application configured as an isolated flyback that provides 500 mA at 24 V with an input voltage range of 190 VAC to 265 VAC.

4.1 Input Stage

Fusible resistor F1 provides protection against component failure causing short or overload in the primary circuit. The fusible resistor also aids in damping of the input current ringing during dimming. Its resistance is useful in suppressing differential line surges.

Diodes D8 to D11 were configured as a full bridge rectifier.

Common mode choke L1, capacitors C1, C18, C8 and differential choke L2 form the EMI filter. The frequency jitter feature of TinySwitch-4 ensures compliance with Class B emission limits. Resistor R17 damps the resonance of L2, which helps lower EMI high frequency noise. Inductor L2 was positioned after the bridge to balance the EMI profile between line and neutral. This also allows the use of small high-voltage ceramic capacitors in the input filter.

A valley fill circuit comprising of C2, C17 and D6, D7 and D5 provides greater than 0.7 power factor. The same circuit absorbs energy from line surge disturbances.

4.2 TinySwitch-4 Primary

The TNY286PG device (U1) is an integrated circuit, which includes a power MOSFET, an oscillator, control, start-up and protection functions.

A clamp circuit (D1, VR1, R1 and C3) limits the voltage that appears on the drain of U1 each time the power MOSFET turns off. The clamp design maximizes efficiency at light load conditions.

The output of the bias/auxiliary supply winding is rectified by diode D3 and filtered by capacitor C4. The bias winding is used to supply current to the TNY286PG BYPASS/MULTIFUNCTION (BP/M) pin during steady-state operation. The value of resistor R4 is selected to deliver the IC supply current to the BP/M pin, thereby inhibiting the internal high-voltage current source that normally charges the BP/M pin capacitor (C9). This results in reduced IC heat dissipation thus lower input power consumption under all load conditions. This also lowers no-load consumption. Three different capacitor values could be used for C9, which selects one of three internal current limits (i.e. RED, STD, INC). A 10 μ F capacitor was used in this design, which selects the increased current limit (INC) set for the TNY286PG.



The transistor of optocoupler U3 pulls current from the ENABLE/UNDER-VOLTAGE (EN/UV) pin of U1. The IC keeps switching as long as the current drawn from the EN/UV pin is less than 90 μA . Switching stops whenever the current drawn from the EN/UV pin exceeds that threshold, which ranges from 90 μA to 150 μA (typical value $\approx 115 \mu\text{A}$). By enabling and disabling switching pulses, the feedback loop regulates the output voltage.

An internal state machine sets the power MOSFET current limit to one of four levels, depending on the main output load current. This ensures that the effective switching frequency remains above the audible frequency range. The lowest current limit (used at no-load) makes the transformer flux density so low that it produces no perceptible audible noise, especially with dip-varnished transformers.

4.3 Output Rectification

Schottky diode D4 provides output rectification, while capacitor C6 is the main output filter capacitor. Secondary RC (R3, C5) snubber is used across D4 to reduce EMI.

4.4 Output Feedback

Resistors R6 and R7 form a voltage divider network, which provides a proportional voltage signal of the output voltage into the input terminal of the TL431 (U2). The TL431 varies its cathode voltage to keep its input voltage constant (equal to 2.5 V, $\pm 2\%$). As the cathode voltage changes, the current through the LED and transistor within U3 changes. Every time the EN/UV pin current exceeds the threshold the next switching cycle is disabled and when the EN/UV pin current falls below the threshold, the next switching cycle is enabled. As the load is reduced, the number of enabled switching cycles decreases by skipping a cycle, which lowers the effective switching frequency and the switching losses. This results in a constant efficiency down to very light load, meeting energy efficiency requirements. Capacitor C14 rolls off the gain of U2 with frequency, to ensure stable operation. Capacitor C11 provides soft start-up which prevents the output voltage from overshooting.

4.5 Line Sense

Resistors R12 and R13 senses the input voltage directly at the input of the bridge rectifier. This reduces no-load power consumption. Resistor R15 ensures that sufficient current is injected into the EN/UV pin even when no current flows through resistors R12 and R13, which is approximately 50% of each line cycle. This ensures that the UV detection feature is enabled at all times thereby preventing any hiccup during a slow brown-in or during a line dropout.

4.6 Overvoltage Protection (OVP)

The IC has internal OVP latching protection via the BP/M pin. It is triggered when current exceeds the OV shutdown threshold ($\approx 5.5 \text{ mA}$) due to an open feedback condition and when the bias voltage rises above the VR2 threshold. The latch condition is reset through R12 and R13, once the AC line is recycled.

4.7 PCB Layout

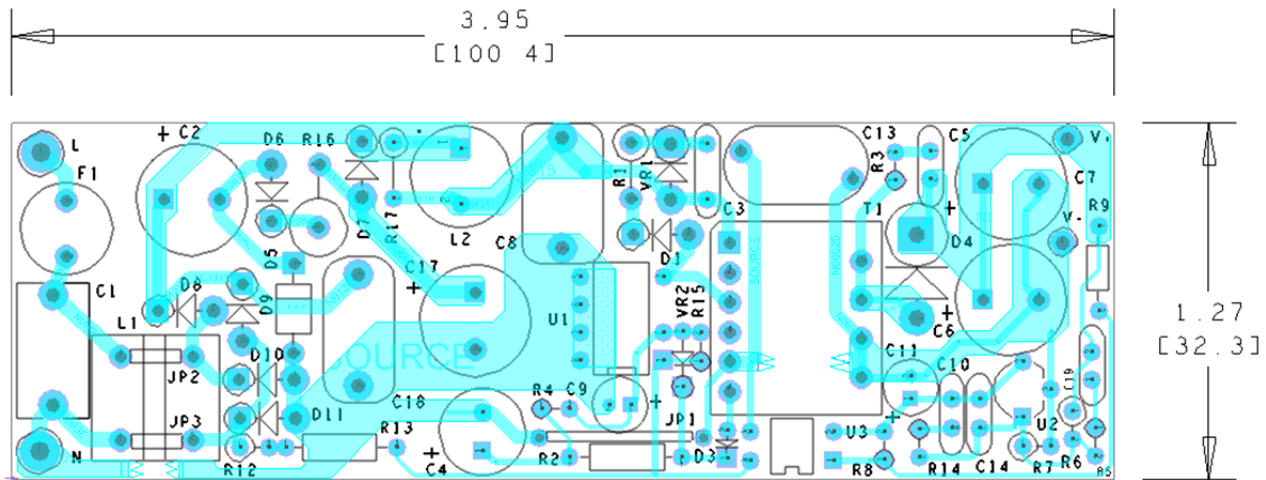


Figure 3 – Printed Circuit Layout.

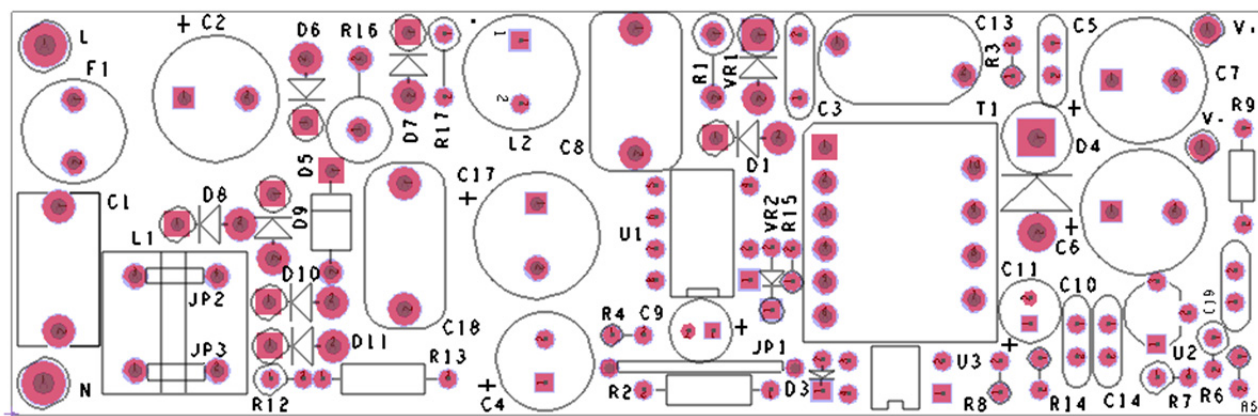


Figure 4 – Component legend.

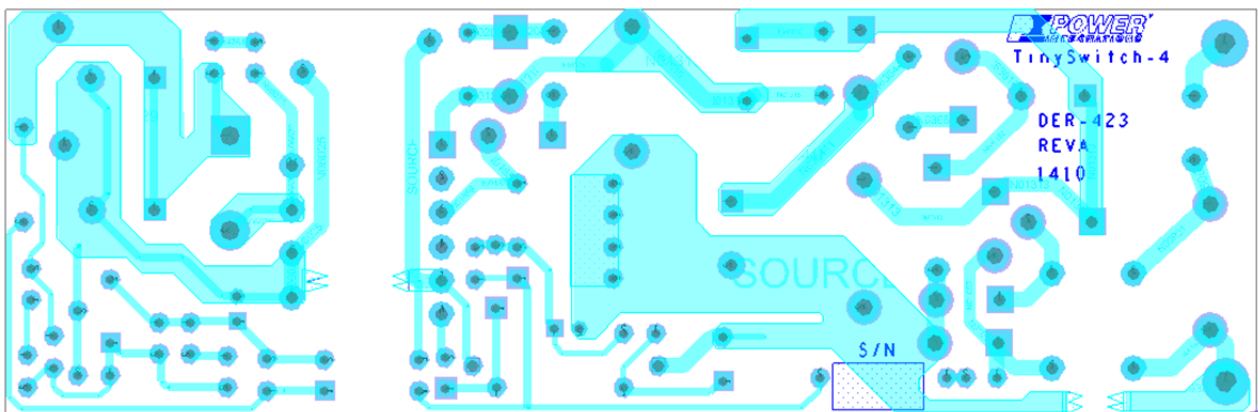


Figure 5 – Bottom Layout.

5 PCB Assembly

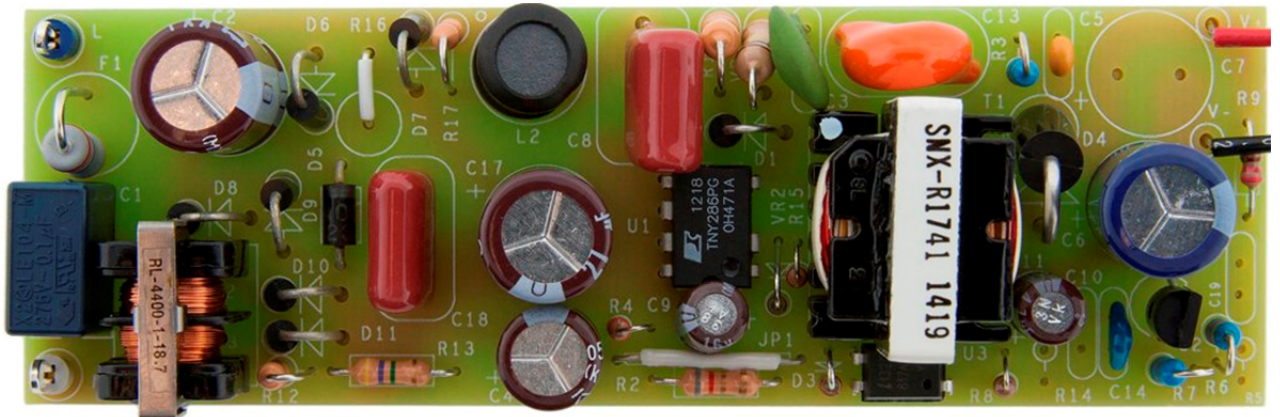


Figure 6 – Top Assembly, No Components on the Bottom Side. Some Parts can be Converted to SMD for More Compact Applications.

6 Bill of Materials

Item	Qty	Ref Des	Description	Mfg P/N	Manufacturer
1	1	C1	100 nF, 275VAC, Film, X2	LE104-M	OKAYA
2	2	C2 C17	27 μ F, 200 V, Electrolytic, (10 x 16),	EKXJ201ELL270MJ16S	Nippon Chemi-Con
3	1	C3	2.2 nF, 1 kV, Disc Ceramic	NCD222K1KVY5FF	NIC
4	1	C4	100 μ F, 50 V, Electrolytic, Gen. Purpose, (8 x 11.5)	KME50VB101M6X11LL	Nippon Chemi-Con
5	1	C5	680 pF, 200 V, Ceramic, X7R	C315C681K2R5TA	Kemet
6	1	C6	470 μ F, 35 V, Electrolytic, Low ESR, 52 m Ω , (10 x 20)	ELXZ350ELL471MJ20S	Nippon Chemi-Con
7	1	C8	330 nF, 450 V, METALPOLYPRO	ECW-F2W334JAQ	Panasonic
8	1	C9	10 μ F, 16 V, Electrolytic, Gen. Purpose, (5 x 11)	EKMG160ELL100ME11D	United Chemi-Con
9	1	C11	4.7 μ F, 50 V, Electrolytic, Gen. Purpose, (5 x 11)	EKMG500ELL4R7ME11D	Nippon Chemi-Con
10	1	C13	2.2 nF, Ceramic, Y1	440LD22-R	Vishay
11	1	C14	1 nF, 100 V, Ceramic, X7R	FK18X7R2A102K	TDK
12	1	C18	100 nF, 400 V, Film	ECQ-E4104KF	Panasonic
13	1	D1	600 V, 1 A, Fast Recovery Diode, 200 ns, DO-41	1N4937RLG	On Semi
14	1	D3	250 V, 250 mA, Fast Switching, DO-35	BAV21	Vishay
15	1	D4	150 V, 3 A, Schottky, DO-201AD	STPS3150RL	ST
16	7	D5 D6 D7 D8 D9 D10 D11	1000 V, 1 A, Rectifier, DO-41	1N4007-E3/54	Vishay
17	1	F1	22 Ω , 10%, 2 W, 10 % Axial Flame Proof, Fusible, Pulse Withstanding	EMC2-22RKI	TT Electronics
18	1	L1	18.7 mH, 0.22 A, Common Mode Choke	RL-4400-1-18.7	Renco
19	1	L2	4.7 mH, 0.150 A, 20%	RL-5480-3-4700	Renco
20	1	R1	22 Ω , 5%, 1/2 W, Carbon Film	CFR-50JB-22R	Yageo
21	1	R2	8.2 Ω , 5%, 1/4 W, Carbon Film	CFR-25JB-8R2	Yageo
22	1	R3	1 k Ω , 1%, 1/4 W, Metal Film	MFR-25FBF-1K00	Yageo
23	1	R4	30 k Ω , 5%, 1/8 W, Carbon Film	CF18JT30K0	Stackpole
24	1	R6	86.6 k Ω , 1%, 1/4 W, Metal Film	MFR-25FBF-86K6	Yageo
25	1	R7	10 k Ω , 1%, 1/4 W, Metal Film	MFR-25FBF-10K0	Yageo
26	1	R8	1 k Ω , 5%, 1/8 W, Carbon Film	CF18JT1K00	Stackpole
27	1	R9	220 Ω , 5%, 1/8 W, Carbon Film	CF18JT220R	Stackpole
28	2	R12 R13	4.7 M Ω , 5%, 1/4 W, Carbon Film	CFR-25JB-4M7	Yageo
29	1	R15	1.5 M Ω , 5%, 1/8 W, Carbon Film	CF18JT1M50	Stackpole
30	1	R17	10 k Ω , 5%, 1/4 W, Carbon Film	CFR-25JB-10K	Yageo
31	1	T1	Bobbin, EE19, Vertical, 10 pins, 6pri, 4sec Transformer	TF-1939 SNX-R1741-X1 PNU-28624	Taiwan Shulin Santronics Premier Magnetics
32	1	U1	TinySwitch-4, DIP-8C	TNY286PG	Power Integrations
33	1	U2	2.495 V Shunt Regulator IC, 2%, 0 to 70C, TO-92	TL431CLPG	On Semi
34	1	U3	Optocoupler, 35 V, CTR 80-160%, 4-DIP	LTV817A	Liteon
35	2	V+ V-	PCB Terminal Hole, #22 AWG	N/A	N/A
36	1	VR1	100 k Ω , 5%, 1/2 W, Carbon Film	CFR-50JB-100K	Yageo
37	1	VR2	27 V, 5%, 500 mW, DO-35	1N5254B	Microsemi
Mechanical BOM					
1	1	JP1	Wire Jumper, Insulated, #24 AWG, 0.6 in	C2003A-12-02	Gen Cable
2	1	N	Test Point, WHT, THRU-HOLE MOUNT	5012	Keystone
3	1	L	Test Point, BLU, THRU-HOLE MOUNT	5127	Keystone



4	1	R16	Wire Jumper, Insulated, TFE, #22 AWG, 0.2 in	C2004-12-02	Alpha
5	1	WIRE #24 AWG INS (V+)	Wire, UL1007, #24 AWG, Red, PVC, 4 "	1007-24/7-2	Anixter
6	1	WIRE #24 AWG INS (V-)	Wire, UL1007, #24 AWG, Blk, PVC, 4"	1007-24/7-0	Anixter
7	1	PCB	PCB, 0.062 X 1.25 X 4 in; 2 oz Cu	-	-



7 Transformer Specification

7.1 Electrical Diagram

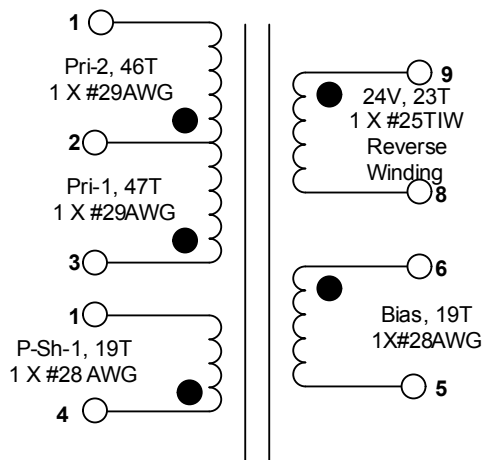


Figure 7 – Transformer Electrical Diagram.

7.2 Electrical Specifications

Electrical Strength	1 second, 60 Hz, from pins 1-3 to pins 8-9.	3000 VAC
Primary Inductance	Pins 1-3, all other windings open, measured at 100 kHz, 0.4 V _{RMS} .	1200 μ H \pm 10%
Resonant Frequency	Pins 1-3 all other windings open.	700 kHz (Min.)
Primary Leakage Inductance	Pins 1-3, with pins 5-9 shorted, measured at 100 kHz, 0.4 V _{RMS} .	25 μ H (Max.)

7.3 Materials

Item	Description
[1]	Core: EE19, P4 (Acme) or Equivalent, gapped for A _G of 136 nH/T ² .
[2]	Bobbin: EE19 (6-4 pins) Vertical, High Creepage.
[3]	Tape Polyester film [2 mil (25 μ m) base thickness], 9.00 mm wide.
[4]	Varnish; BC346 or BC359 (Dolphs).
[5]	Magnet Wire: AWG #29.
[6]	Triple Insulated Wire: AWG #25.
[7]	Magnet Wire: AWG #28.
[8]	Tape Polyester film [2 mil (25 μ m) base thickness], 5.00 mm wide.

7.4 Transformer Build Diagram

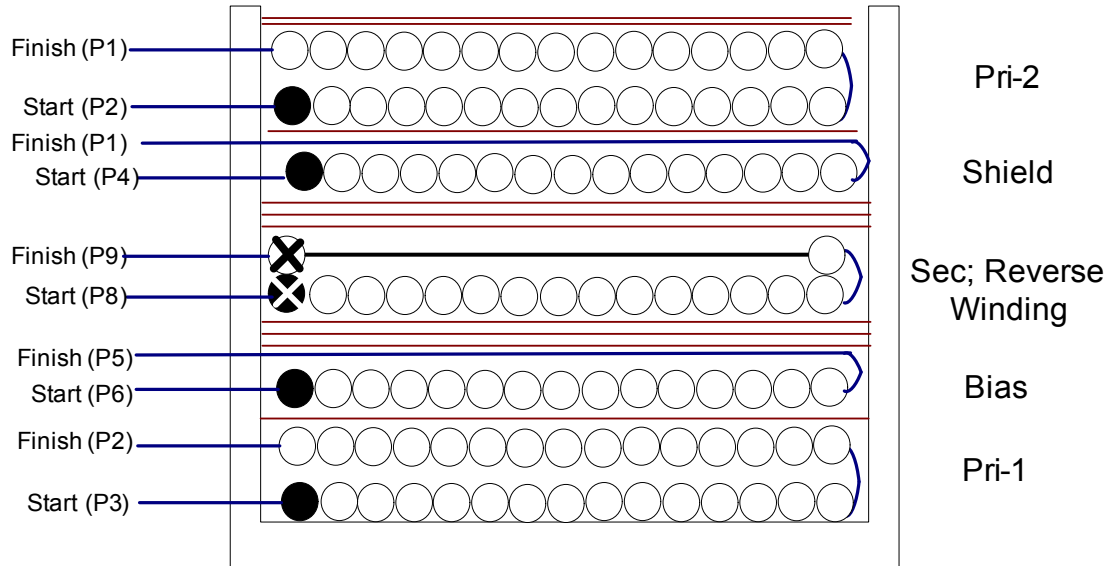


Figure 8 – Transformer Build Diagram.

7.5 Transformer Construction

Bobbin Preparation	For the purpose of these instructions, bobbin is oriented on winder such that pin 1 side is on the left. Winding direction is counter-clockwise. Follow the pin number assignment in the specification.
WDG1; Pri-1	Start on pin(s) 3 and wind 47 turns (x 1 filar) of item [5]. in 2 layer(s) from left to right. At the end of 1st layer, continue to wind the next layer from right to left. On the final layer, spread the winding evenly across entire bobbin. Finish this winding on pin(s) 2. Wind 12 bifilar turns of #27 AWG. Finish on pin 10.
Insulation	Add 1 layer of tape, item [3], for insulation.
WDG2; Bias	Start on pin(s) 6 and wind 19 turns (x 1 filar) of item [7]. Wind in same rotational direction as primary winding. Spread the winding evenly across entire bobbin. Finish this winding on pin(s) 5.
Insulation	Add 3 layers of tape, item [3], for insulation.
WDG3; Sec Reverse Winding	Start on pin(s) 8 and reverse wind 23 turns (x 1 filar) of item [6]. Spread the winding evenly across entire bobbin. Wind in opposite rotational direction as primary winding. Finish this winding on pin(s) 9.
Insulation	Add 3 layers of tape, item [3], for insulation.
WDG4; Pri-Shield	Start at pin 4 on the secondary side and wind 19 turns (x 1 filar) of item [7]. Wind in same rotational direction as primary winding. Spread the winding evenly across entire bobbin. Finish this winding on pin(s) 1. Cut out wire connected to temp pin on secondary side. Leave this end of primary shield winding not connected. Bend the end 90 degree and cut the wire in the middle of the bobbin.
Insulation	Add 1 layer of tape, item [3], for insulation.
WDG5; Pri-2	Start on pin(s) 2 and wind 46 turns (x 1 filar) of item [5] in 2 layer(s) from left to right. At the end of 1st layer, continue to wind the next layer from right to left. On the final layer, spread the winding evenly across entire bobbin. Finish this winding on pin(s) 1.
Core Preparation	Grind E core to get the desired inductance. Wrap bottom of one E core with 2 layers of tape to secure the core
Varnish	Dip the transformer to the varnish [4] then dry.



8 Transformer Design Spreadsheet

ACDC_TinySwitch-4_121812; Rev.1.1; Copyright Power Integrations 2012	INPUT	INFO	OUTPUT	UNIT	ACDC_TinySwitch-4_121812_Rev1-1.xls; TinySwitch-4 Continuous/Discontinuous Flyback Transformer Design Spreadsheet
ENTER APPLICATION VARIABLES					
VACMIN	150		150	Volts	Minimum AC Input Voltage
VACMAX	265		265	Volts	Maximum AC Input Voltage
fL			50	Hertz	AC Mains Frequency
VO	24.00		24.00	Volts	Output Voltage (at continuous power)
IO	0.50		0.50	Amps	Power Supply Output Current (corresponding to peak power)
Power			12	Watts	Continuous Output Power
n	0.85		0.85		Efficiency Estimate at output terminals. Under 0.7 if no better data available
Z			0.50		Z Factor. Ratio of secondary side losses to the total losses in the power supply. Use 0.5 if no better data available
tC			3.00	mSeconds	Bridge Rectifier Conduction Time Estimate
CIN	30.00		30	uFarads	Input Capacitance
ENTER TinySwitch-4 VARIABLES					
TinySwitch-4	TNY286P		TNY286P		User-defined TinySwitch-4
Chose Configuration	INC		Increased Current Limit		Enter "RED" for reduced current limit (sealed adapters), "STD" for standard current limit or "INC" for increased current limit (peak or higher power applications)
ILIMITMIN			0.419	Amps	Minimum Current Limit
ILIMITTYP			0.450	Amps	Typical Current Limit
ILIMITMAX			0.499	Amps	Maximum Current Limit
fSmin			124000	Hertz	Minimum Device Switching Frequency
I ² fmin			24.057	A ² kHz	I ² f (product of current limit squared and frequency is trimmed for tighter tolerance)
VOR	100.00		100	Volts	Reflected Output Voltage (VOR < 135 V Recommended)
VDS			10	Volts	TinySwitch-4 on-state Drain to Source Voltage
VD			0.7	Volts	Output Winding Diode Forward Voltage Drop
KP			0.97		Ripple to Peak Current Ratio (KP < 6)
KP_TRANSIENT			0.73		Transient Ripple to Peak Current Ratio. Ensure KP_TRANSIENT > 0.25
ENTER BIAS WINDING VARIABLES					
VB	20.00		20.00	Volts	Bias Winding Voltage
VDB			0.70	Volts	Bias Winding Diode Forward Voltage Drop
NB			18.62		Bias Winding Number of Turns
VZOV			26.00	Volts	Over Voltage Protection zener diode voltage.
UVLO VARIABLES					
V_UV_TARGET			215.59	Volts	Target DC under-voltage threshold, above which the power supply will start
V_UV_ACTUAL			207.20	Volts	Typical DC start-up voltage based on standard value of RUV_ACTUAL
RUV_IDEAL			8.54	Mohms	Calculated value for UV Lockout resistor
RUV_ACTUAL			8.20	Mohms	Closest standard value of resistor to RUV_IDEAL
ENTER TRANSFORMER CORE/CONSTRUCTION VARIABLES					
Core Type	EE19		EE19		Enter Transformer Core
Core		EE19		P/N:	PC40EE19-Z
Custom core				P/N:	EE19_BOBBIN
AE			0.23	cm ²	Core Effective Cross Sectional Area



LE			3.94	cm	Core Effective Path Length
AL			1250	nH/T ²	Ungapped Core Effective Inductance
BW			9	mm	Bobbin Physical Winding Width
M			0	mm	Safety Margin Width (Half the Primary to Secondary Creepage Distance)
L			3		Number of Primary Layers
NS	23		23		Number of Secondary Turns
DC INPUT VOLTAGE PARAMETERS					
VMIN			196	Volts	Minimum DC Input Voltage
VMAX			375	Volts	Maximum DC Input Voltage
CURRENT WAVEFORM SHAPE PARAMETERS					
DMAX			0.34		Duty Ratio at full load, minimum primary inductance and minimum input voltage
IAVG			0.08	Amps	Average Primary Current
IP			0.42	Amps	Minimum Peak Primary Current
IR			0.42	Amps	Primary Ripple Current
IRMS			0.17	Amps	Primary RMS Current
TRANSFORMER PRIMARY DESIGN PARAMETERS					
LP			1184	uHenries	Typical Primary Inductance. +/- 10% to ensure a minimum primary inductance of 1065 uH
LP_TOLERANCE			10	%	Primary inductance tolerance
NP			93		Primary Winding Number of Turns
ALG			136	nH/T ²	Gapped Core Effective Inductance
BM			2758	Gauss	Maximum Operating Flux Density, BM<3100 is recommended
BAC			1379	Gauss	AC Flux Density for Core Loss Curves (0.5 X Peak to Peak)
ur			1704		Relative Permeability of Ungapped Core
LG			0.19	mm	Gap Length (Lg > 0.1 mm)
BWE			27	mm	Effective Bobbin Width
OD			0.29	mm	Maximum Primary Wire Diameter including insulation
INS			0.05	mm	Estimated Total Insulation Thickness (= 2 * film thickness)
DIA			0.24	mm	Bare conductor diameter
AWG			31	AWG	Primary Wire Gauge (Rounded to next smaller standard AWG value)
CM			81	Cmils	Bare conductor effective area in circular mils
CMA			477	Cmils/Amp	Primary Winding Current Capacity (200 < CMA < 500)
TRANSFORMER SECONDARY DESIGN PARAMETERS					
Lumped parameters					
ISP			1.70	Amps	Peak Secondary Current
ISRMS			0.96	Amps	Secondary RMS Current
IRIPPLE			0.82	Amps	Output Capacitor RMS Ripple Current
CMS			191	Cmils	Secondary Bare Conductor minimum circular mils
AWGS			27	AWG	Secondary Wire Gauge (Rounded up to next larger standard AWG value)
VOLTAGE STRESS PARAMETERS					
VDRAIN			605	Volts	Maximum Drain Voltage Estimate (Assumes 20% zener clamp tolerance and an additional 10% temperature tolerance)
PIVS			117	Volts	Output Rectifier Maximum Peak Inverse Voltage
TRANSFORMER SECONDARY DESIGN PARAMETERS (MULTIPLE OUTPUTS)					
1st output					
VO1			24	Volts	Main Output Voltage (if unused, defaults to single output design)



IO1			0.500	Amps	Output DC Current
PO1			12.00	Watts	Output Power
VD1			0.7	Volts	Output Diode Forward Voltage Drop
NS1			23.00		Output Winding Number of Turns
ISRMS1			0.957	Amps	Output Winding RMS Current
IRIPPLE1			0.82	Amps	Output Capacitor RMS Ripple Current
PIVS1			117	Volts	Output Rectifier Maximum Peak Inverse Voltage
Recommended Diodes			1N5817, SB120		Recommended Diodes for this output
CMS1			191	Cmils	Output Winding Bare Conductor minimum circular mils
AWGS1			27	AWG	Wire Gauge (Rounded up to next larger standard AWG value)
DIAS1			0.36	mm	Minimum Bare Conductor Diameter
ODS1			0.39	mm	Maximum Outside Diameter for Triple Insulated Wire
2nd output					
VO2				Volts	Output Voltage
IO2				Amps	Output DC Current
PO2			0.00	Watts	Output Power
VD2			0.7	Volts	Output Diode Forward Voltage Drop
NS2			0.65		Output Winding Number of Turns
ISRMS2			0.000	Amps	Output Winding RMS Current
IRIPPLE2			0.00	Amps	Output Capacitor RMS Ripple Current
PIVS2			3	Volts	Output Rectifier Maximum Peak Inverse Voltage
Recommended Diode					Recommended Diodes for this output
CMS2			0	Cmils	Output Winding Bare Conductor minimum circular mils
AWGS2			N/A	AWG	Wire Gauge (Rounded up to next larger standard AWG value)
DIAS2			N/A	mm	Minimum Bare Conductor Diameter
ODS2			N/A	mm	Maximum Outside Diameter for Triple Insulated Wire
3rd output					
VO3				Volts	Output Voltage
IO3				Amps	Output DC Current
PO3			0.00	Watts	Output Power
VD3			0.7	Volts	Output Diode Forward Voltage Drop
NS3			0.65		Output Winding Number of Turns
ISRMS3			0.000	Amps	Output Winding RMS Current
IRIPPLE3			0.00	Amps	Output Capacitor RMS Ripple Current
PIVS3			3	Volts	Output Rectifier Maximum Peak Inverse Voltage
Recommended Diode					Recommended Diodes for this output
CMS3			0	Cmils	Output Winding Bare Conductor minimum circular mils
AWGS3			N/A	AWG	Wire Gauge (Rounded up to next larger standard AWG value)
DIAS3			N/A	mm	Minimum Bare Conductor Diameter
ODS3			N/A	mm	Maximum Outside Diameter for Triple Insulated Wire
Total power			12	Watts	Total Output Power
Negative Output	N/A		N/A		If negative output exists enter Output number; eg: If VO2 is negative output, enter 2

9 Performance Data

All measurements performed at room temperature unless specified.

9.1 Efficiency

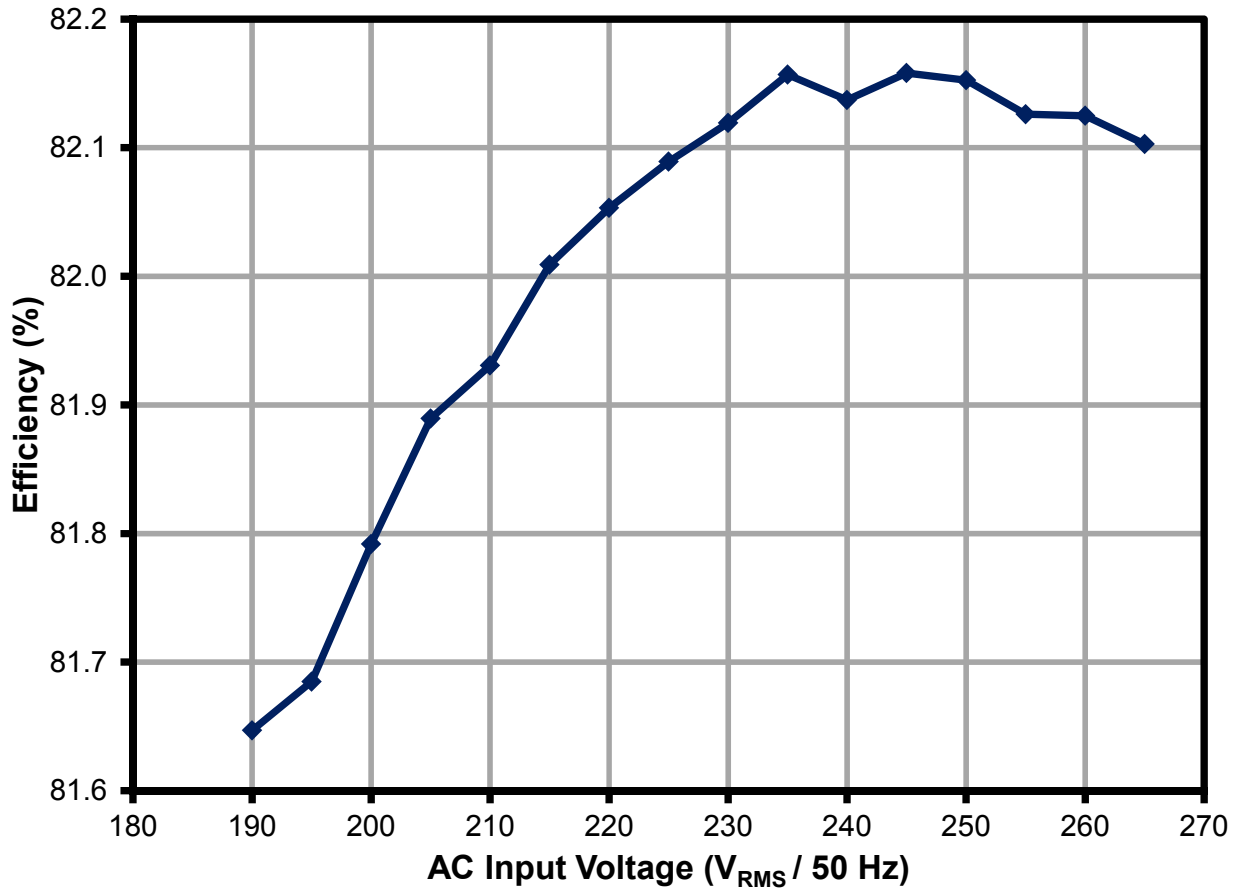


Figure 9 – Efficiency vs. Input Voltage, Room Temperature, 60 Hz.

Input		Input Measurement				Load Measurement			
VAC (V _{RMS})	Freq (Hz)	V _{IN} (V _{RMS})	I _{IN} (A _{RMS})	P _{IN} (W)	PF	V _{OUT} (V _{DC})	I _{OUT} (A _{DC})	P _{OUT} (W)	Efficiency (%)
180	50	179.94	0.10	14.98	0.83	24.48	0.50	12.21	81.52
185	50	184.91	0.10	14.97	0.83	24.48	0.50	12.21	81.57
190	50	189.97	0.10	14.95	0.82	24.48	0.50	12.21	81.65
195	50	194.95	0.09	14.94	0.82	24.47	0.50	12.2	81.68
200	50	199.91	0.09	14.93	0.81	24.48	0.50	12.21	81.79
205	50	204.97	0.09	14.91	0.81	24.48	0.50	12.21	81.89
210	50	209.94	0.09	14.90	0.80	24.47	0.50	12.21	81.93
215	50	214.92	0.09	14.89	0.80	24.48	0.50	12.21	82.01
220	50	219.97	0.09	14.88	0.79	24.48	0.50	12.21	82.05
225	50	224.94	0.08	14.87	0.79	24.47	0.50	12.21	82.09
230	50	229.92	0.08	14.87	0.78	24.48	0.50	12.21	82.12
235	50	234.97	0.08	14.86	0.78	24.48	0.50	12.21	82.16
240	50	239.95	0.08	14.86	0.77	24.48	0.50	12.21	82.14
245	50	244.92	0.08	14.86	0.77	24.48	0.50	12.21	82.16
250	50	249.98	0.08	14.86	0.76	24.48	0.50	12.21	82.15
255	50	254.95	0.08	14.86	0.76	24.48	0.50	12.21	82.13
260	50	259.93	0.08	14.87	0.75	24.48	0.50	12.21	82.12
265	50	265.00	0.08	14.87	0.75	24.48	0.50	12.21	82.10
270	50	269.97	0.07	14.88	0.74	24.48	0.50	12.21	82.07
275	50	274.94	0.07	14.88	0.74	24.47	0.50	12.21	82.02

Table 1 – Data for Figure 9.



9.2 Active Mode Efficiency

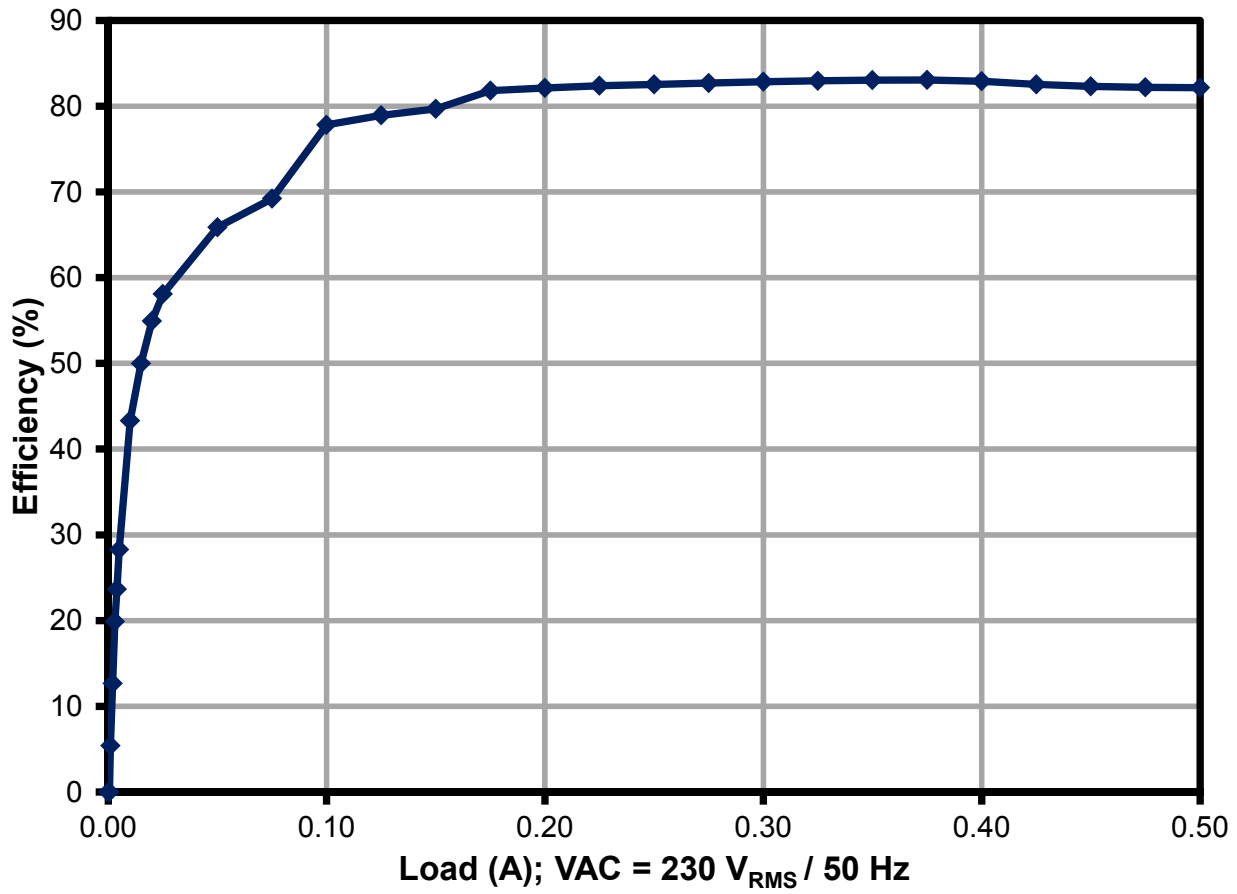


Figure 10 – Load efficiency at 230 V_{RMS} / 60 Hz line, Room Temperature, 60 Hz.

Load Setting		Input Measurement				Load Measurement			
Load (%)	Load (A)	V _{IN} (V _{RMS})	I _{IN} (A _{RMS})	P _{IN} (W)	PF	V _{OUT} (V _{DC})	I _{OUT} (A _{DC})	P _{OUT} (W)	Efficiency (%)
100	0.50	229.93	0.08	14.87	0.78	24.48	0.50	12.21	82.14
95	0.48	229.93	0.08	14.11	0.78	24.48	0.47	11.60	82.21
90	0.45	229.93	0.08	13.35	0.77	24.48	0.45	10.99	82.31
85	0.43	229.93	0.07	12.57	0.76	24.48	0.42	10.37	82.55
80	0.40	229.94	0.07	11.77	0.75	24.48	0.40	9.76	82.91
75	0.38	229.94	0.06	11.02	0.74	24.48	0.37	9.15	83.06
70	0.35	229.94	0.06	10.29	0.73	24.48	0.35	8.54	83.02
65	0.33	229.94	0.06	9.56	0.72	24.48	0.32	7.93	82.95
60	0.30	229.94	0.05	8.83	0.71	24.48	0.30	7.32	82.86
55	0.28	229.94	0.05	8.10	0.69	24.48	0.27	6.70	82.70
50	0.25	229.94	0.05	7.38	0.67	24.48	0.25	6.09	82.54
45	0.23	229.94	0.04	6.65	0.65	24.48	0.22	5.48	82.37
40	0.20	229.94	0.04	5.93	0.64	24.48	0.20	4.87	82.12
35	0.18	229.94	0.04	5.20	0.62	24.48	0.17	4.25	81.81
30	0.15	229.94	0.03	4.57	0.61	24.48	0.15	3.64	79.70
25	0.13	229.94	0.03	3.84	0.58	24.48	0.12	3.03	78.94
20	0.10	229.94	0.03	3.11	0.53	24.48	0.10	2.42	77.81
15	0.08	229.95	0.02	2.61	0.48	24.48	0.07	1.80	69.21
10	0.05	229.95	0.02	1.81	0.44	24.48	0.05	1.19	65.86
5	0.03	229.95	0.01	1.00	0.34	24.48	0.02	0.58	58.09
4	0.02	229.95	0.01	0.83	0.31	24.48	0.02	0.46	54.93
3	0.02	229.95	0.01	0.66	0.26	24.48	0.01	0.33	49.99
2	0.01	229.95	0.01	0.49	0.21	24.48	0.01	0.211	43.32
1	0.01	229.95	0.01	0.30	0.14	24.48	0.00	0.09	28.28
0.80	0.004	229.95	0.01	0.26	0.13	24.48	0.00	0.06	23.66
0.60	0.003	229.95	0.01	0.23	0.11	24.48	0.00	0.05	19.88
0.40	0.002	229.95	0.01	0.20	0.10	24.48	0.00	0.03	12.67
0.20	0.001	229.95	0.01	0.17	0.08	24.48	0.00	0.01	5.41
0.10	0.0005	229.95	0.01	0.15	0.08	24.48	0.00	0.00	0.00
0.00	0	229.95	0.01	0.08	0.04	24.48	0.00	0.00	0.00
							Average Efficiency		81.67

Table 2 – Data for Figure 10.

The external power supply requirements below all require meeting active mode efficiency and no-load input power limits. Minimum active mode efficiency is defined as the average efficiency of 25, 50, 75 and 100% of output current (based on the nameplate output current rating).

For adapters that are single input voltage only then the measurement is made at the rated single nominal input voltage (115 VAC or 230 VAC), for universal input adapters the measurement is made at both nominal input voltages (115 VAC and 230 VAC).

To meet the standard the measured average efficiency (or efficiencies for universal input supplies) must be greater than or equal to the efficiency specified by the standard.



The test method can be found here:

http://www.energystar.gov/ia/partners/prod_development/downloads/power_supplies/EP_SupplyEffic_TestMethod_0804.pdf

For the latest up to date information please visit the PI Green Room:

<http://www.powerint.com/greenroom/regulations.htm>

9.2.1 USA Energy Independence and Security Act 2007

This legislation mandates all single output single output adapters, including those provided with products, manufactured on or after July 1st, 2008 must meet minimum active mode efficiency and no load input power limits.

Active Mode Efficiency Standard Models

Nameplate Output (P _o)	Minimum Efficiency in Active Mode of Operation
< 1 W	$0.5 \times P_o$
≥ 1 W to ≤ 51 W	$0.09 \times \ln(P_o) + 0.5$
> 51 W	0.85

ln = natural logarithm

No-load Energy Consumption

Nameplate Output (P _o)	Maximum Power for No-load AC-DC EPS
All	≤ 0.5 W

This requirement supersedes the legislation from individual US States (for example CEC in California).

9.2.2 ENERGY STAR EPS Version 2.0

This specification takes effect on November 1st, 2008.

Active Mode Efficiency Standard Models

Nameplate Output (P _o)	Minimum Efficiency in Active Mode of Operation
≤ 1 W	$0.48 \times P_o + 0.14$
> 1 W to ≤ 49 W	$0.0626 \times \ln(P_o) + 0.622$
> 49 W	0.87

ln = natural logarithm

Active Mode Efficiency Low Voltage Models (V_o<6 V and I_o ≥ 550 mA)

Nameplate Output (P _o)	Minimum Efficiency in Active Mode of Operation
≤ 1 W	$0.497 \times P_o + 0.067$
> 1 W to ≤ 49 W	$0.075 \times \ln(P_o) + 0.561$
> 49 W	0.86

ln = natural logarithm

No-load Energy Consumption (both models)

Nameplate Output (P_o)	Maximum Power for No-load AC-DC EPS
0 to < 50 W	≤ 0.3 W
≥ 50 W to ≤ 250 W	≤ 0.5 W



9.3 No-load Input Power

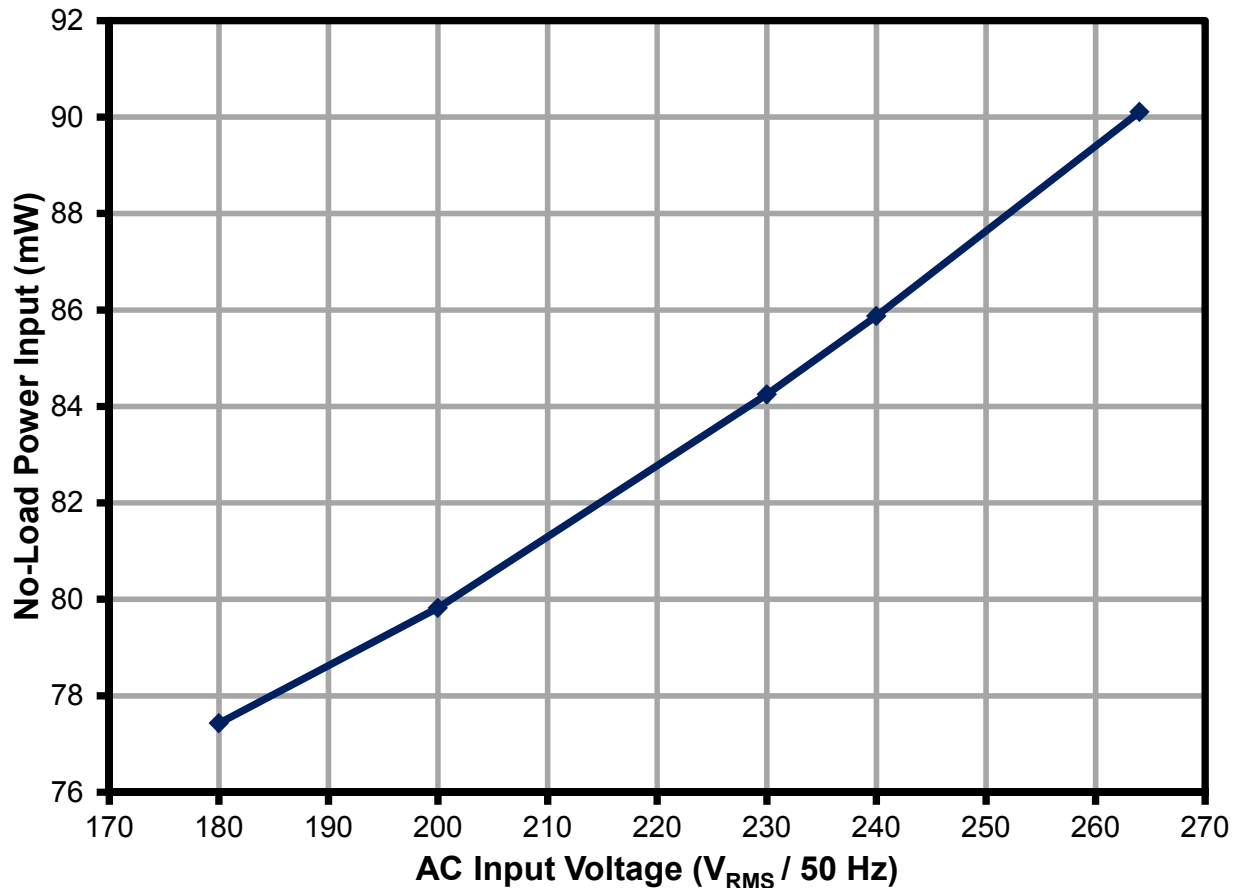


Figure 11- Zero Load Input Power vs. Input Line Voltage, Room Temperature, 50 Hz.

Input		Input Measurement (Integration)				
VAC (V _{RMS})	Freq (Hz)	P _{IN} (mW)	I _{IN} (mA _{RMS})	V _{OUT} (V _{DC})	Limit (mW)	Remarks
180	50	77.43	7.44	24.48	100	Pass
200	50	79.82	7.85	24.48	100	Pass
230	50	84.25	8.53	24.48	100	Pass
240	50	85.87	8.77	24.48	100	Pass
265	50	90.11	9.35	24.48	100	Pass

Table 3 – Data for Figure 10.

9.4 Available Standby Output Power

The chart below shows the available output power vs line voltage for an input power of 1 W, 2 W and 3 W.

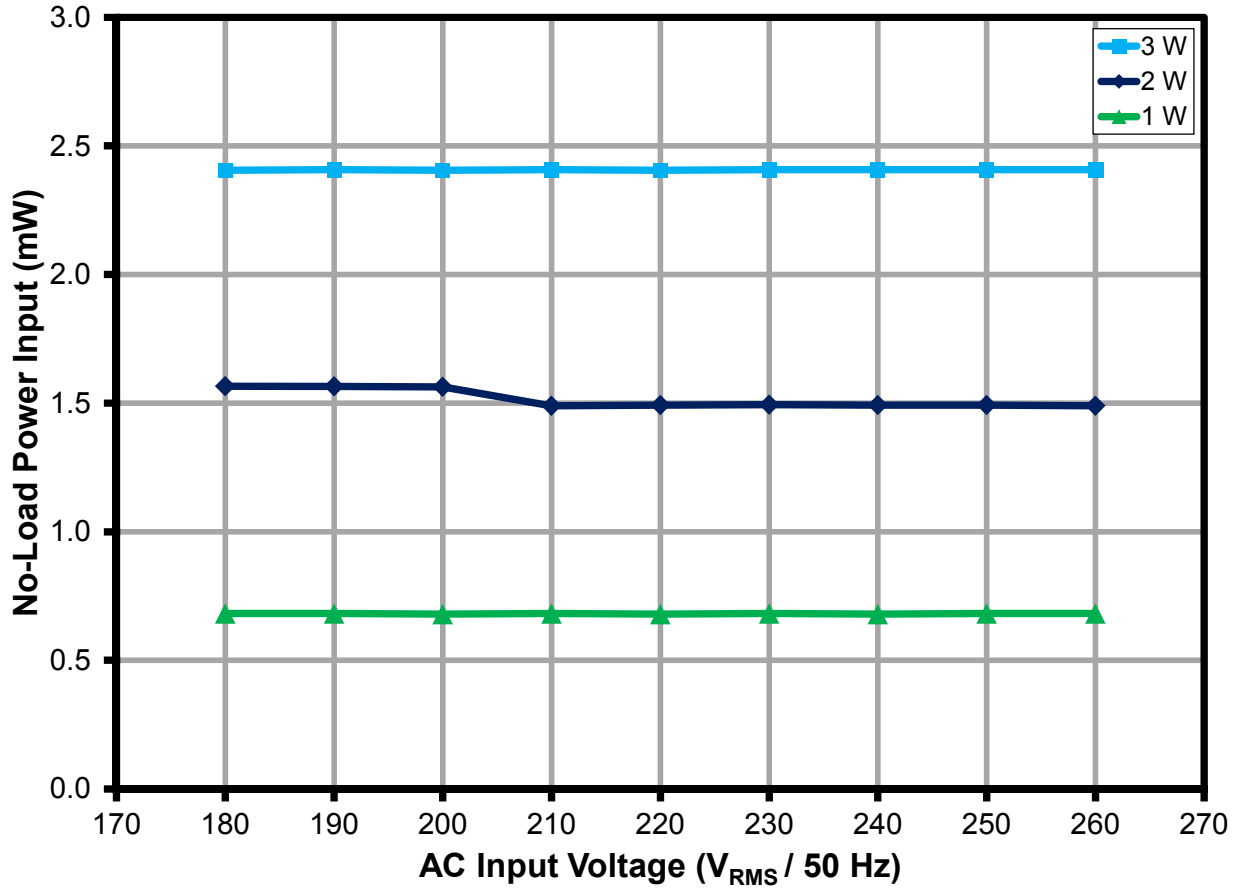


Figure 12 – Available Standby Power vs. Line.

9.5 Regulation

9.5.1 Load

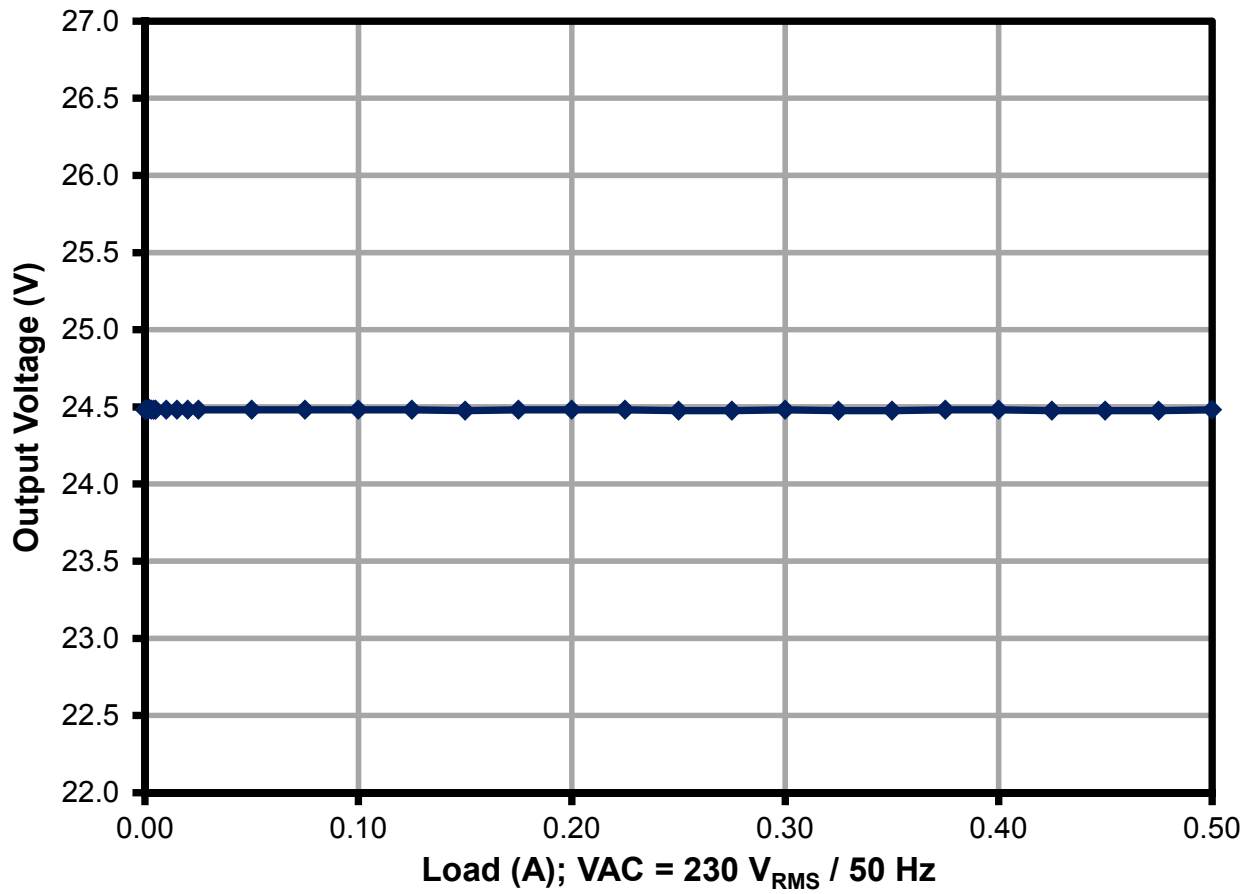


Figure 13 – Load Regulation, Room Temperature.



9.5.2 Line

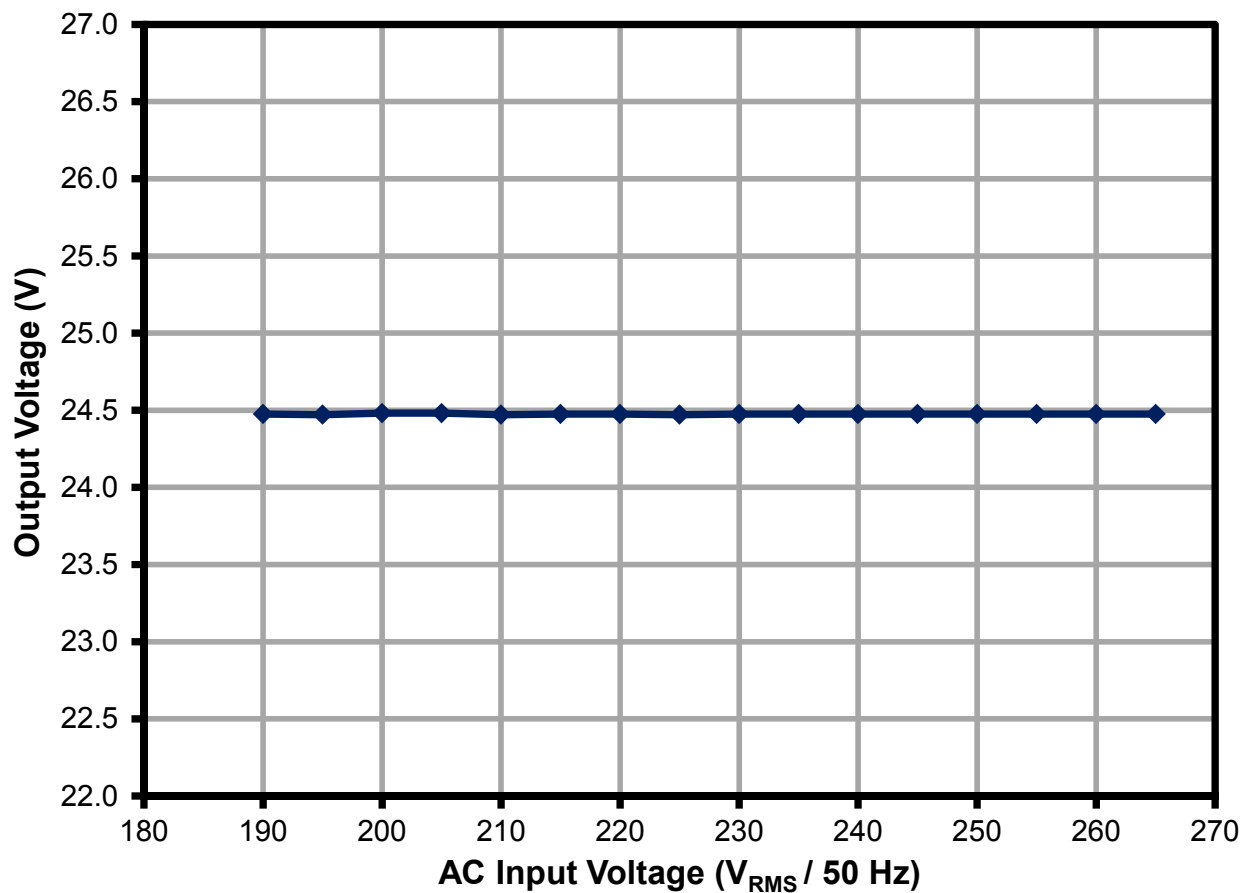


Figure 14 – Line Regulation, Room Temperature, Full Load.

9.5.3 Power Factor (PF)

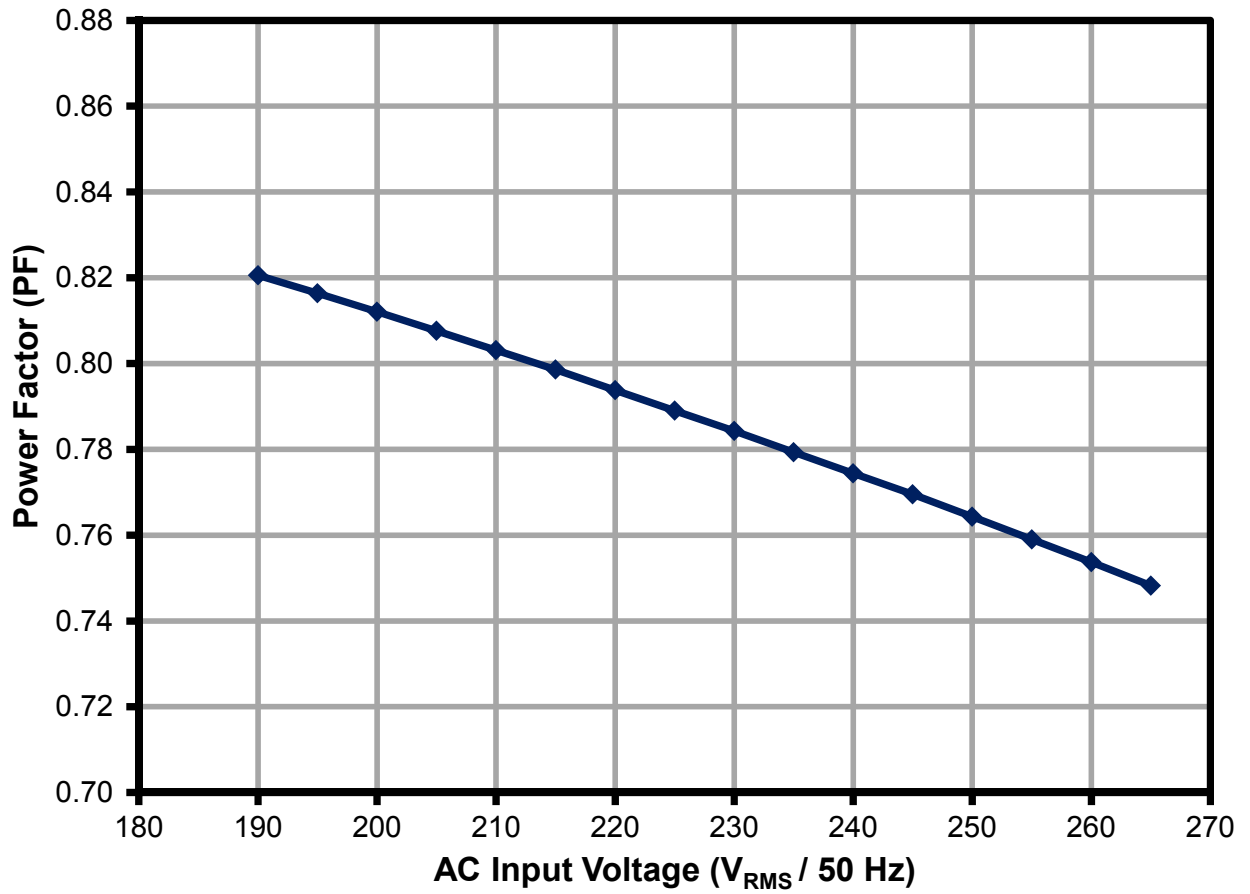


Figure 15 – Power Factor vs. AC Input at full load.



10 Thermal Performance

10.1 Thermal Images

Unit was measured open frame (no enclosure). Temperatures were allowed to stabilize prior to making measurements (>30 mins)

10.1.1 Component Temperatures (190 VAC, 50 Hz, 25 °C)

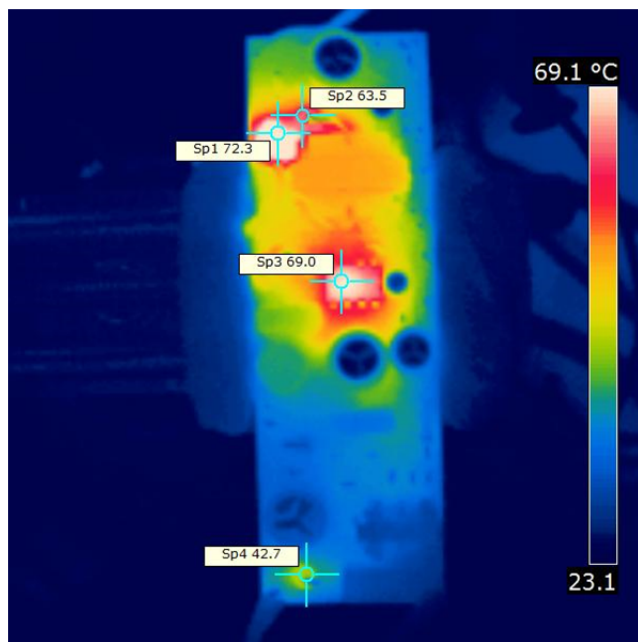


Figure 16 – SP1 – Snubber Output Resistor (R3).
 SP2 – Output Diode (D4).
 SP3 – TNY286PG (U1).
 SP4 – Fusible Resistor (F1).

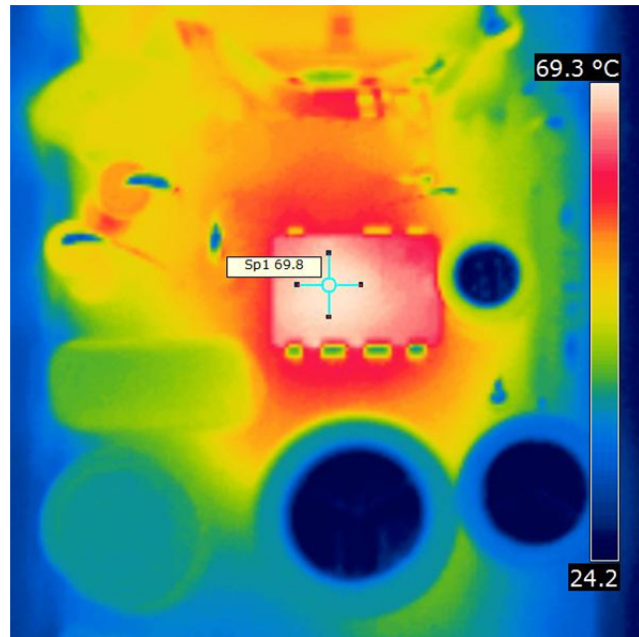


Figure 17 – SP1 – TNY286PG (U1).

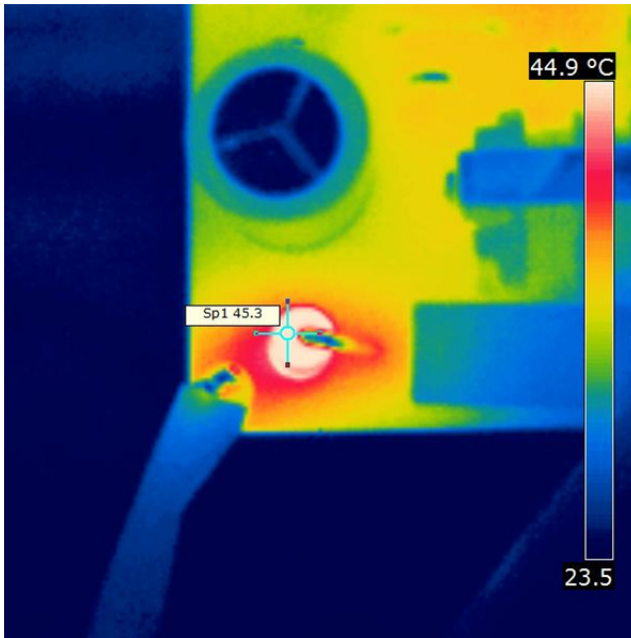


Figure 18 – SP1 – Fusible Resistor (F1).

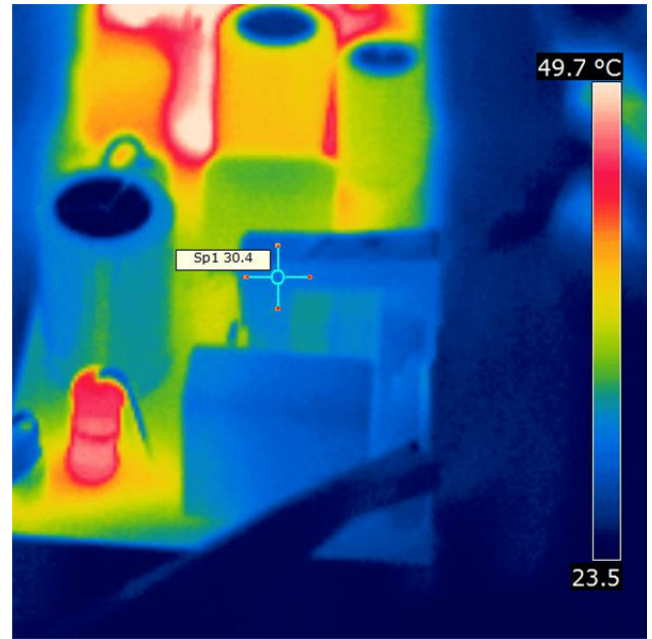


Figure 19 – SP1 – Common Mode Choke (L1).

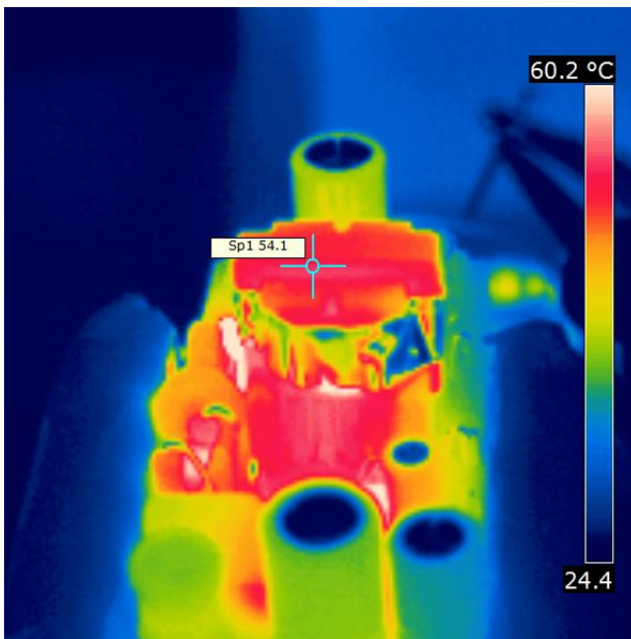


Figure 20 – SP1 – Transformer (T1).

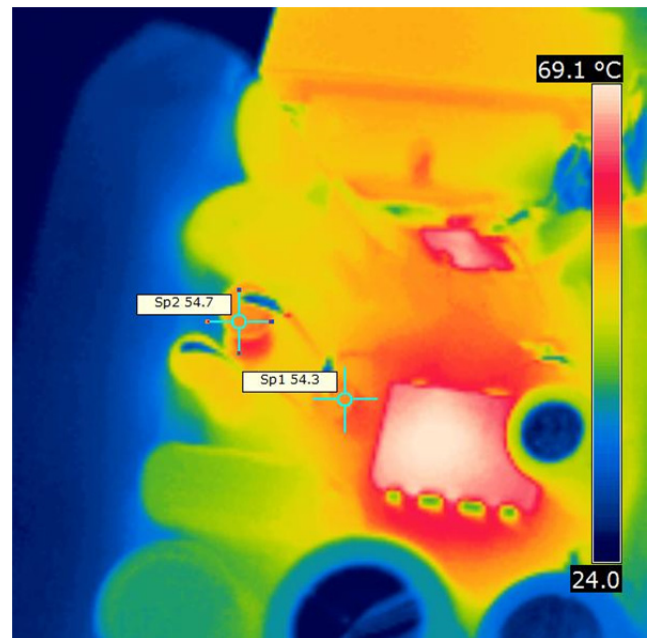


Figure 21 – SP1 – Snubber Diode (D1).
SP2 – Snubber Resistor (VR1).

10.1.2 Component Temperatures (265 VAC, 50 Hz, 25°C)

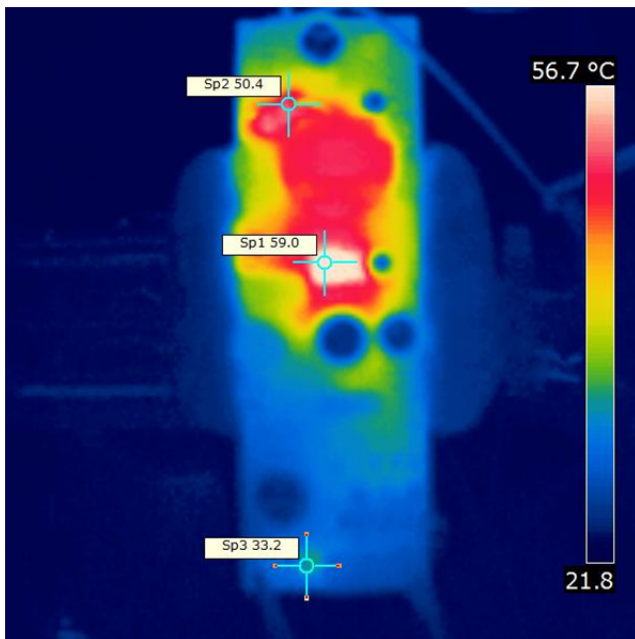


Figure 22 – SP1 – TNY286PG (U1).
SP2 – Output Diode (D4).
SP3 – Fusible Resistor (FR1).

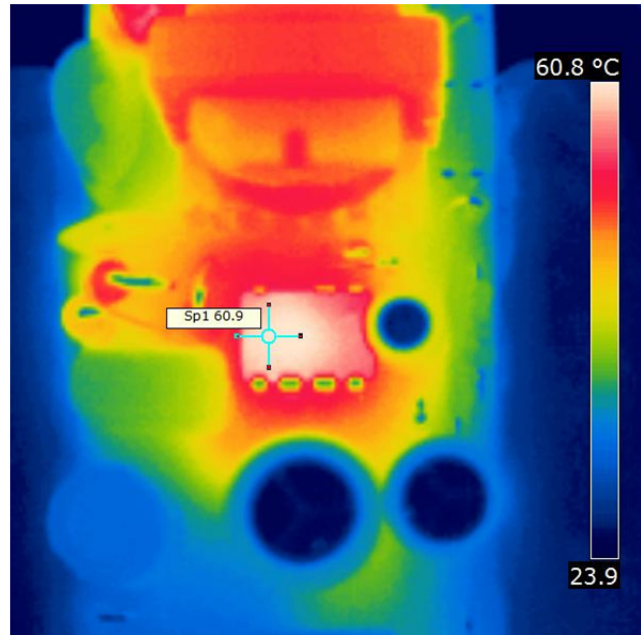


Figure 23 – SP1 – TNY286PG (U1).

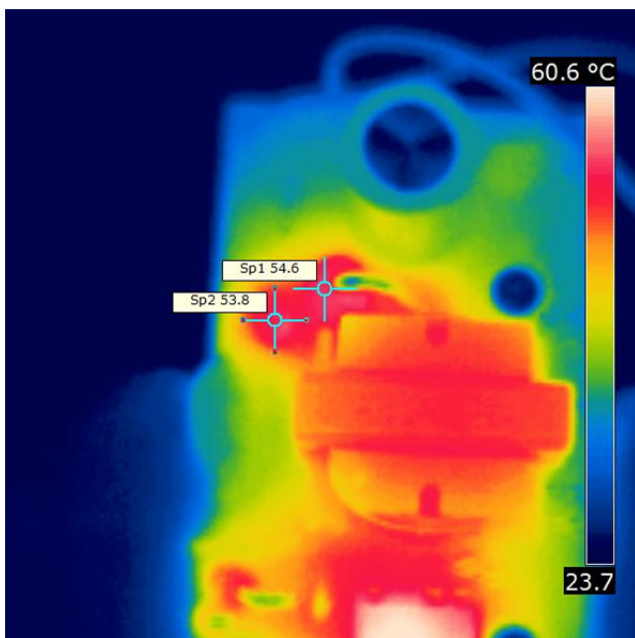


Figure 24 – SP1 – Output Diode (D4).
SP2 – Output Snubber Resistor (R4).

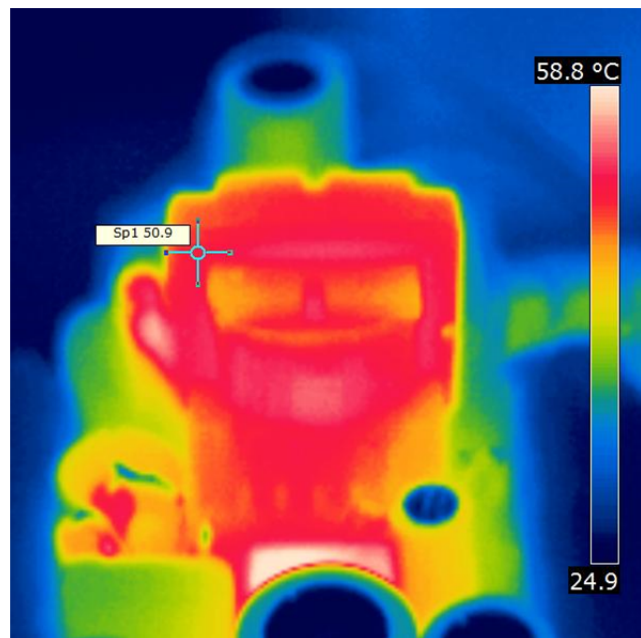


Figure 25 – SP1 – Transformer (T1).

11 Waveforms

11.1 Input Voltage and Current, Normal Operation

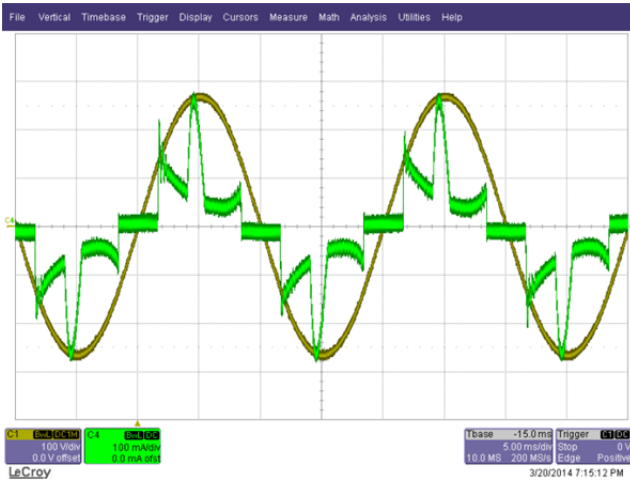


Figure 26 – 190 VAC, Full Load.
 Green: I_{IN} , 0.1 A / div.
 Yellow: V_{DIN} , 100 V, 5 ms / div.

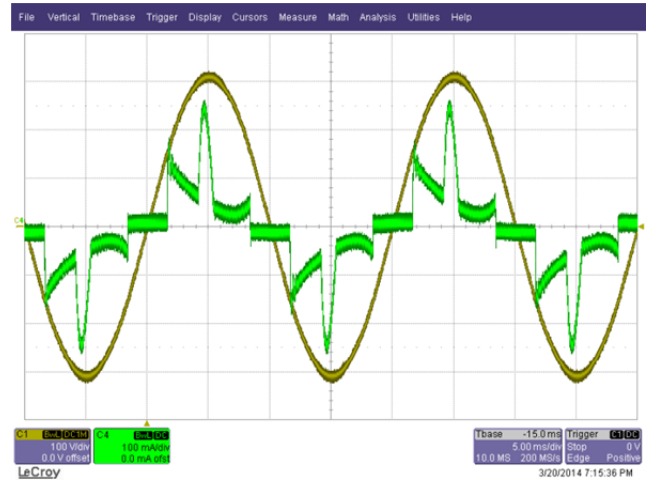


Figure 27 – 220 VAC, Full Load.
 Green: I_{IN} , 0.1 A / div.
 Yellow: V_{DIN} , 100 V, 5 ms / div.

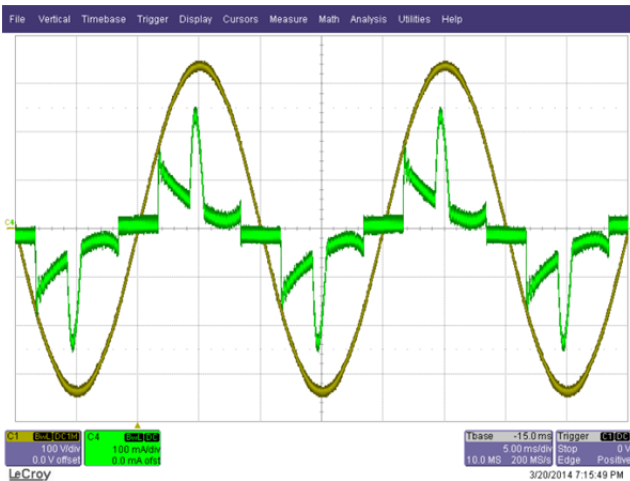


Figure 28 – 240 VAC, Full Load.
 Green: I_{IN} , 0.1 A / div.
 Yellow: V_{DIN} , 100 V, 5 ms / div.

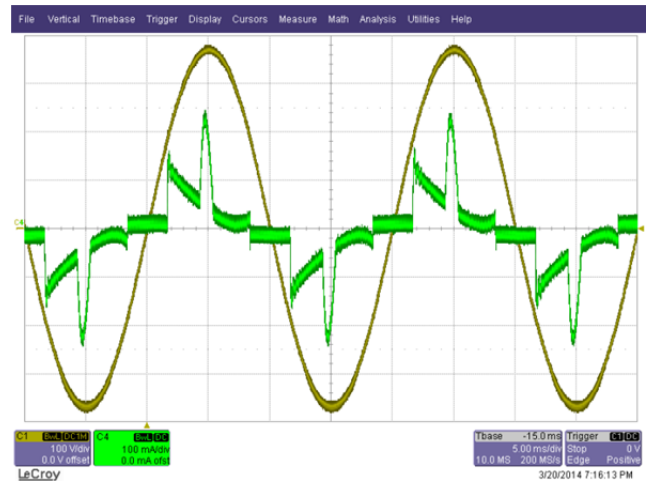


Figure 29 – 265 VAC, Full Load.
 Green: I_{IN} , 0.1 A / div.
 Yellow: V_{DIN} , 100 V, 5 ms / div.



11.2 Drain Voltage and Current, Normal Operation

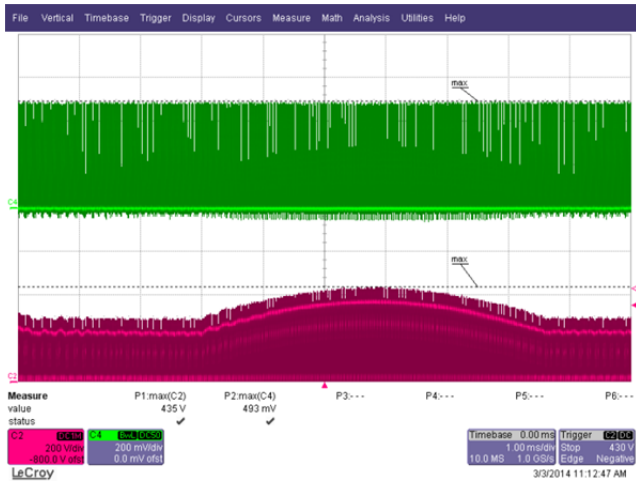


Figure 30 – 190 VAC, Full Load.
 Upper: I_{DRAIN} , 0.2 A / div.
 Lower: V_{DRAIN} , 200 V, 1 ms / div.



Figure 31 – 190 VAC, Full Load.
 Upper: I_{DRAIN} , 0.2 A / div.
 Lower: V_{DRAIN} , 200 V / div.
 Time Scale: 1 ms / div.
 Zoom Time Scale: 100 μ s / div.

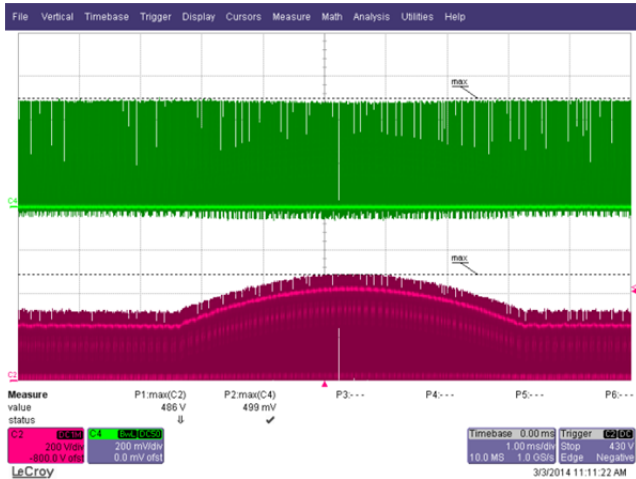


Figure 32 – 230 VAC, Full Load.
 Upper: I_{DRAIN} , 0.2 A / div.
 Lower: V_{DRAIN} , 200 V, 1ms / div.

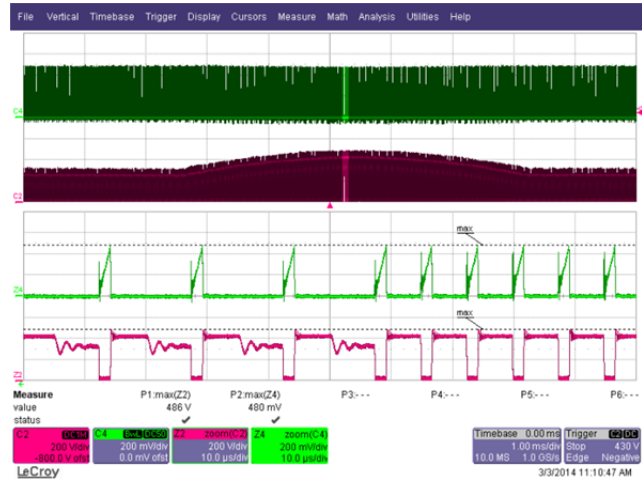


Figure 33 – 230 VAC, Full Load.
 Upper: I_{DRAIN} , 0.2 A / div.
 Lower: V_{DRAIN} , 200 V/div.
 Time Scale: 1 ms / div.
 Zoom Time Scale: 10 μ s / div.

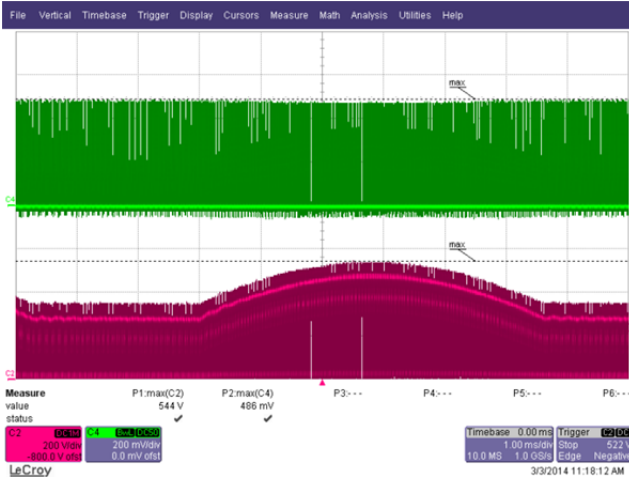


Figure 34 – 265 VAC, Full Load.
 Upper: I_{DRAIN} , 0.2 A / div.
 Lower: V_{DRAIN} , 200 V.
 Time Scale: 1 ms / div.



Figure 35 – 265 VAC, Full Load.
 Upper: I_{DRAIN} , 0.2 A / div.
 Lower: V_{DRAIN} , 200 V / div.
 Time Scale: 1 ms / div.
 Zoom Time Scale: 10 μ s / div.

11.3 Drain Voltage and Current Start-up Profile

No saturation or any possible cause of failure.

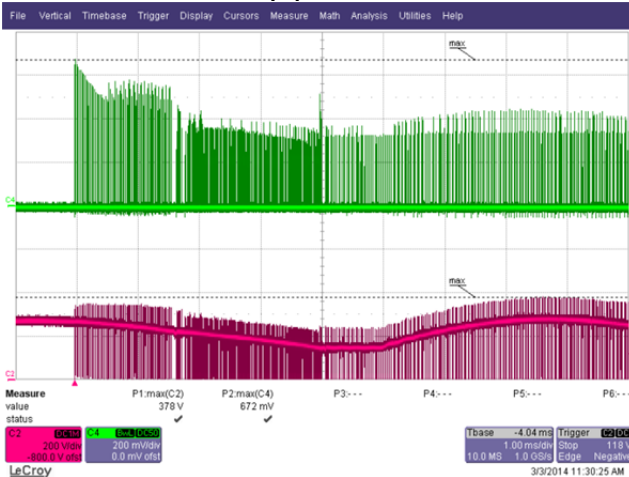


Figure 36 – 190 VAC Input and Maximum Load.
 Upper: I_{DRAIN} , 0.2 A / div.
 Lower: V_{DRAIN} , 200 V / div.
 Time Scale: 1 ms / div.



Figure 37 – 190 VAC Input and Maximum Load.
 Upper: I_{DRAIN} , 0.2 A / div.
 Lower: V_{DRAIN} , 200 V / div.
 Time Scale: 1 ms / div.
 Zoom Time Scale: 2 μ s / div.

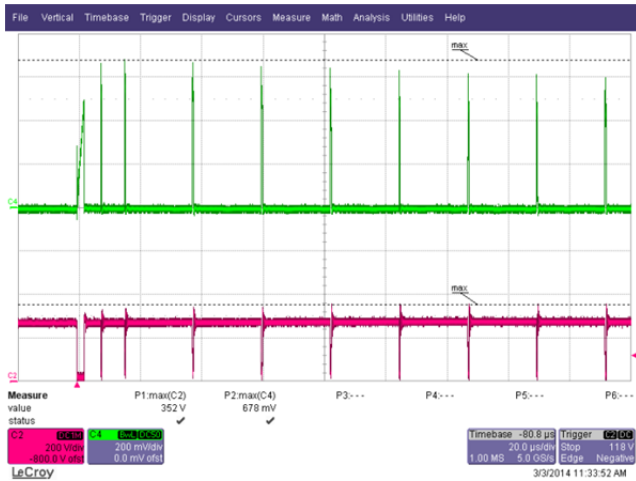


Figure 38 – 190 VAC Input and Maximum Load.
 Upper: I_{DRAIN} , 0.2 A / div.
 Lower: V_{DRAIN} , 200 V / div.
 Time Scale: 1 μ s / div.

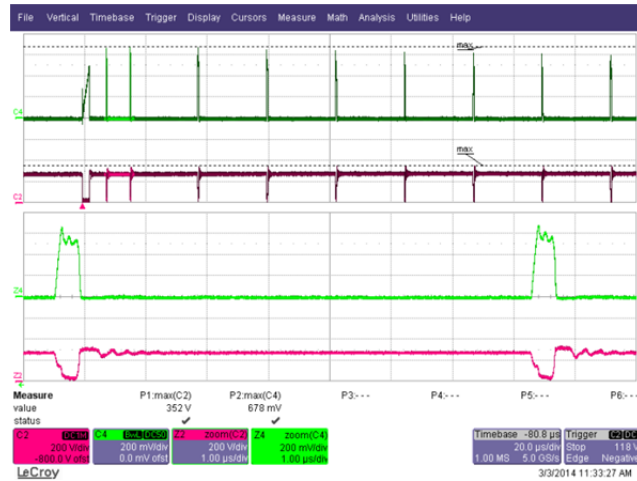


Figure 39 – 190 VAC Input and Maximum Load.
 Upper: I_{DRAIN} , 0.2 A / div.
 Lower: V_{DRAIN} , 200 V / div.
 Time Scale: 20 μ s / div.
 Zoom Time Scale: 1 μ s / div.

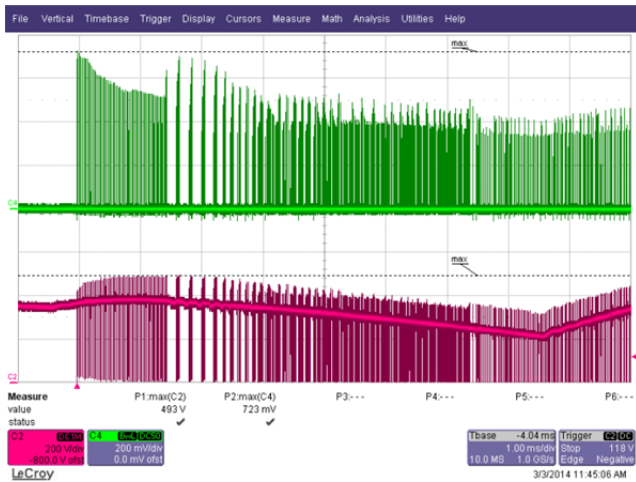


Figure 40 – 265 VAC Input and Maximum Load.
 Upper: I_{DRAIN} , 0.2 A / div.
 Lower: V_{DRAIN} , 200 V / div.
 Time Scale: 1 ms / div.



Figure 41 – 265 VAC Input and Maximum Load.
 Upper: I_{DRAIN} , 0.2 A / div.
 Lower: V_{DRAIN} , 200 V / div.
 Time Scale: 1 ms / div.
 Zoom Time Scale: 5 μ s / div.

11.4 Drain Voltage and Current Start-up Short Waveform

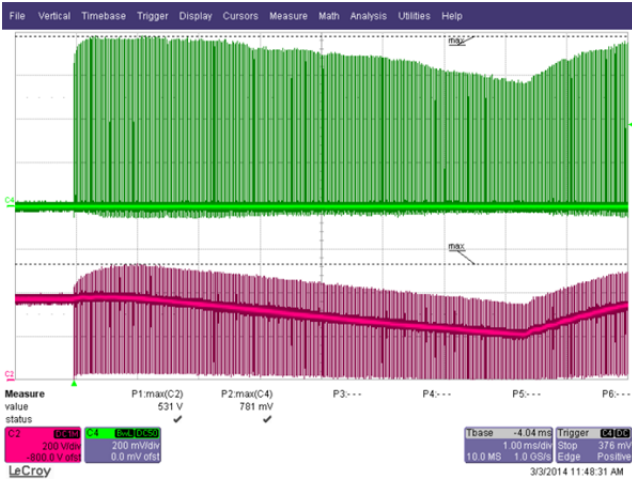


Figure 42 – 265 VAC Input and Shorted Load.
 Upper: I_{DRAIN} , 0.2 A / div.
 Lower: V_{DRAIN} , 200 V / div.
 Time Scale: 1 ms / div.



Figure 43 – 265 VAC Input and Shorted Load.
 Upper: I_{DRAIN} , 0.2 A / div.
 Lower: V_{DRAIN} , 200 V / div.
 Time Scale: 1 ms / div.
 Zoom Time Scale: 5 μ s / div.

11.5 Drain Voltage and Current Normal Running Short Waveform



Figure 44 – 265 VAC Input, Full Load then Short.
 180 ms Continuous Switching.
 Upper: I_{DRAIN} , 0.2 A / div.
 Lower: V_{DRAIN} , 200 V / div.
 Time Scale: 500 ms / div.



Figure 45 – 265 VAC Input, Full Load then Short.
 2.5 s Off Time before Auto-restart.
 Upper: I_{DRAIN} , 0.2 A / div.
 Lower: V_{DRAIN} , 200 V / div.
 Time Scale: 500 ms / div.



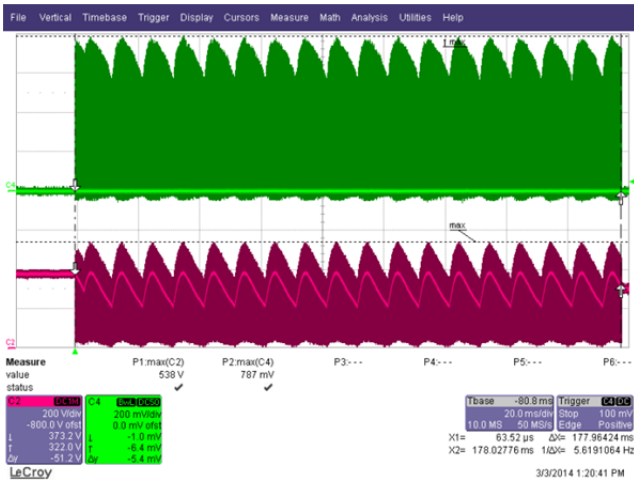


Figure 46 – 265 VAC Input and Full Load then Short.
 Upper: I_{DRAIN} , 0.2 A / div.
 Lower: V_{DRAIN} , 200 V / div.
 Time Scale: 20 ms / div.

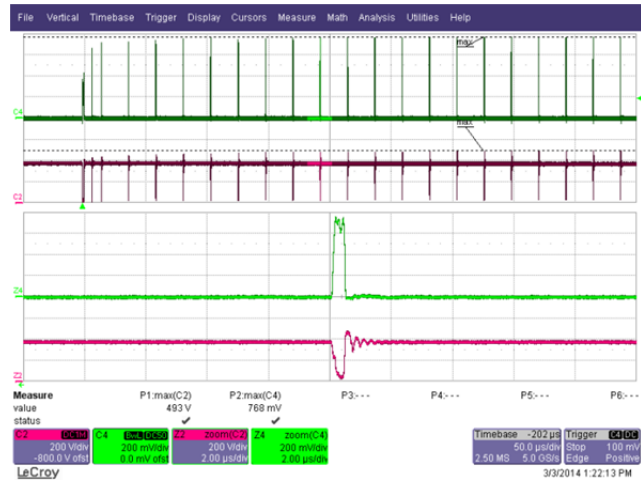


Figure 47 – 265 VAC Input and Full Load then Short.
 Upper: I_{DRAIN} , 0.2 A / div.
 Lower: V_{DRAIN} , 200 V / div.
 Time Scale: 50 μ s / div.
 Zoom Time Scale: 2 μ s / div.

11.6 Output Diode Waveform at Normal Operation



Figure 48 – 190 VAC Input and Full Load then Short.
 Upper: I_{DRAIN} , 0.2 A / div.
 Lower: V_{OUT} , 20 V / div.
 Time Scale: 100 μ s / div.



Figure 49 – 265 VAC Input and Full Load then Short.
 Upper: I_{DRAIN} , 0.2 A / div.
 Lower: V_{DRAIN} , 200 V / div.
 Time Scale: 50 μ s / div.
 Zoom Time Scale: 2 μ s / div.

11.7 Output Voltage Start-up Profile

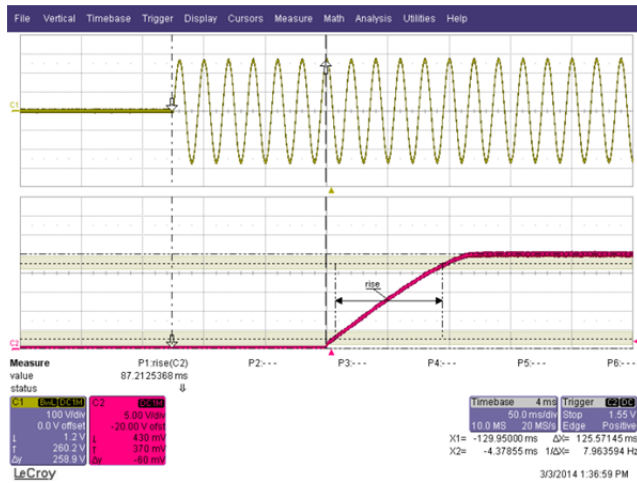


Figure 50 – Start-up Profile, 190 VAC
 Upper: V_{IN} , 100 V / div.
 Lower: V_{OUT} , 5 V / div.
 Time Scale: 50 ms / div.

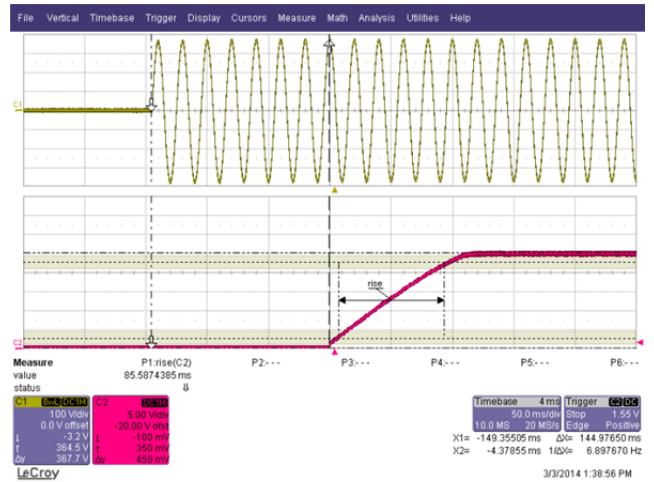


Figure 51 – Start-up Profile, 265 VAC.
 Upper: V_{IN} , 100 V / div.
 Lower: V_{OUT} , 5 V / div.
 Time Scale: 50 ms / div.



11.8 Load Transient Response (0% to 100% Load Step)

In the figures shown below, signal averaging was used to better enable viewing the load transient response. The oscilloscope was triggered using the load current step as a trigger source. Since the output switching and line frequency occur essentially at random with respect to the load transient, contributions to the output ripple from these sources will average out, leaving the contribution only from the load step response.

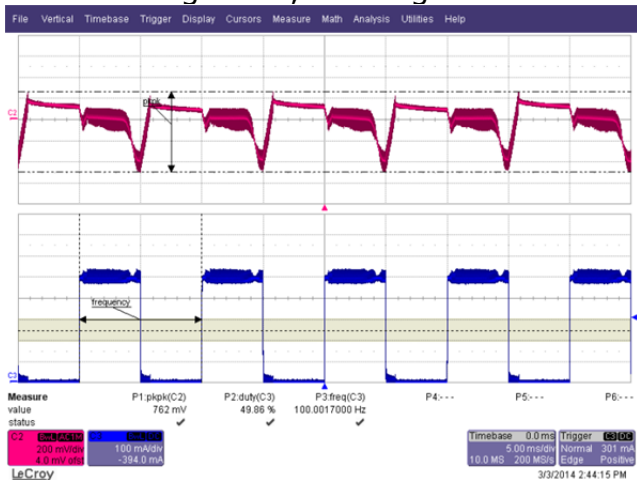


Figure 52 – Transient Response, 230 VAC, 0-100-0% Load Step for Worst Case Condition at 100 Hz.
Upper: V_{OUT} , 200 mV / div.
Lower: I_{OUT} , 100 mA / div.
Time Scale: 5 ms / div.

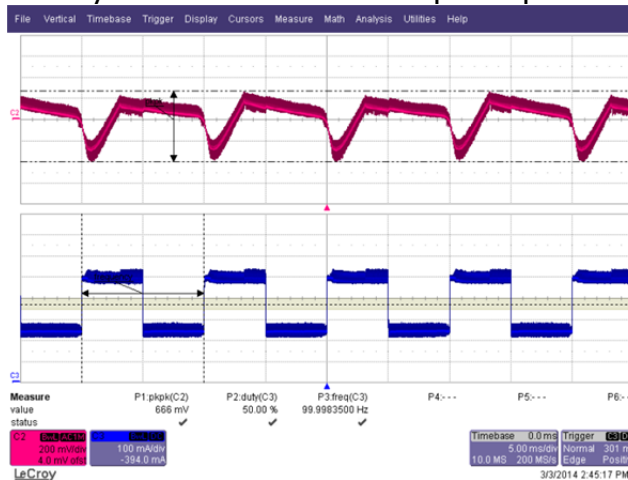


Figure 53 – Transient Response, 230 VAC, 50-100-50% Load Step for Worst Case Condition at 100 Hz.
Upper: V_{OUT} , 200 mV / div.
Lower: I_{OUT} , 100 mA / div.
Time Scale: 5 ms / div.

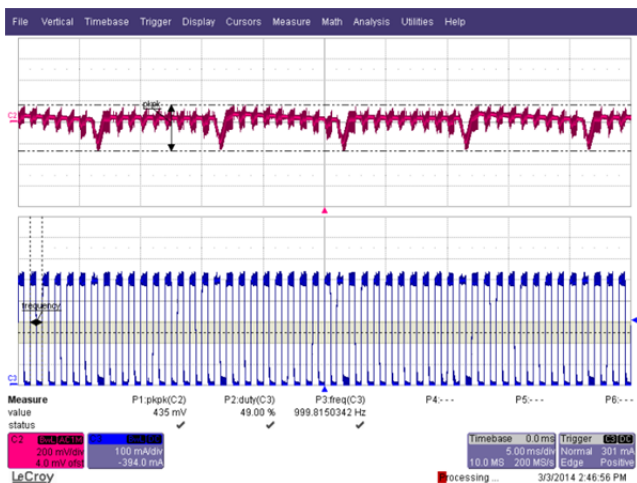


Figure 54 – Transient Response, 230 VAC, 0-100-0% Load Step for Worst Case Condition at 1 kHz.
Upper: V_{OUT} , 200 mV / div.
Lower: I_{OUT} , 100 mA / div.
Time Scale: 5 ms / div.

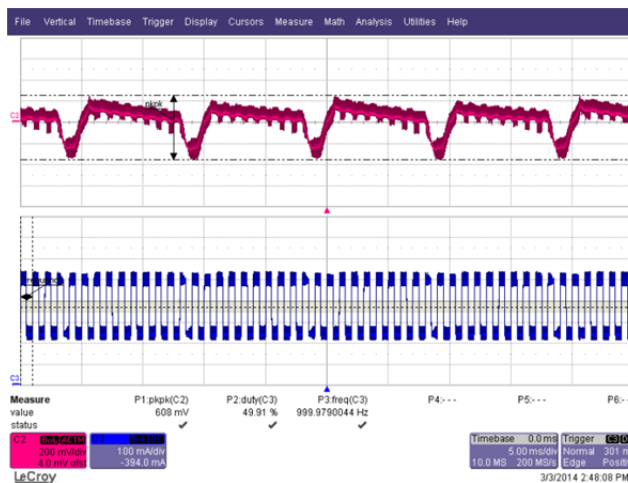


Figure 55 – Transient Response, 230 VAC, 50-100-50% Load Step for Worst Case Condition at 1 kHz.
Upper: V_{OUT} , 200 mV / div.
Lower: I_{OUT} , 100 mA / div.
Time Scale: 5 ms / div.



11.9 Brown-out Test

No component failure was observed.

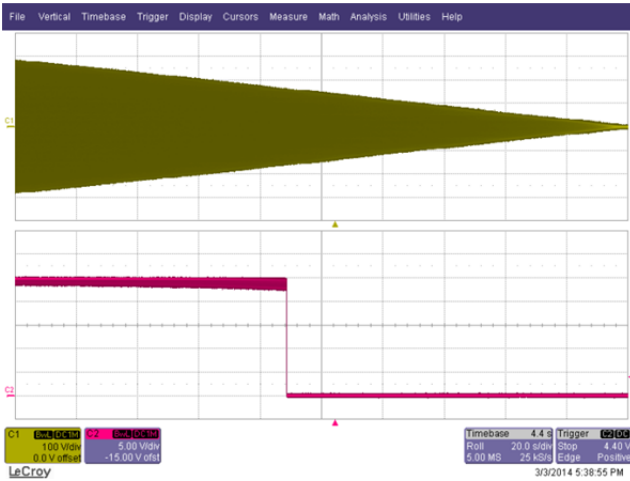


Figure 56 – Brown-out at 0.5 V / div.
 Upper: V_{IN} , 100 V / div.
 Lower: V_{OUT} , 5 V / div.
 Time Scale: 20 s / div.

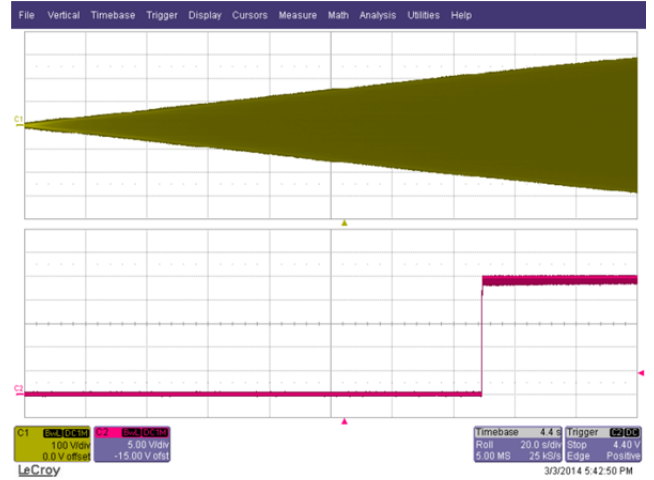


Figure 57 – Brown-in at 0.5 V / div.
 Upper: V_{IN} , 100 V / div.
 Lower: V_{OUT} , 5 V / div.
 Time Scale: 20 s / div.

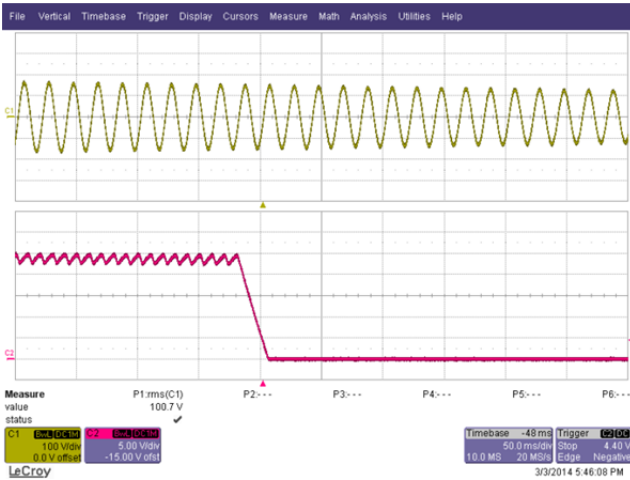


Figure 58 – Brown-out at 0.5 V / div.
 Upper: V_{IN} , 100 V / div.
 Lower: V_{OUT} , 5 V / div.
 Time Scale: 50 ms / div.

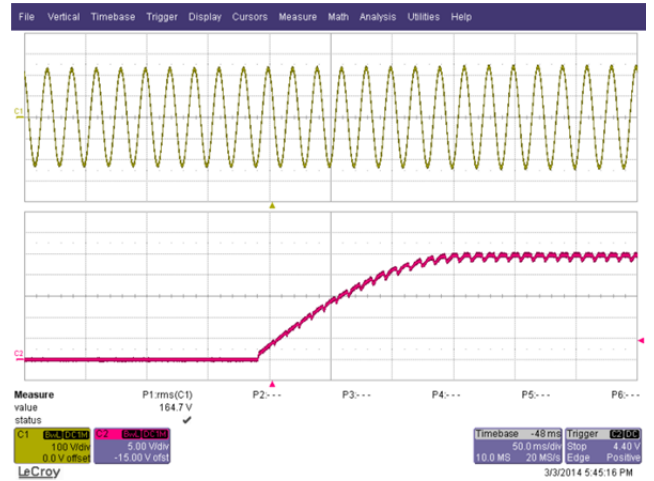


Figure 59 – Brown-in at 0.5 V / div.
 Upper: V_{IN} , 100 V / div.
 Lower: V_{OUT} , 5 V / div.
 Time Scale: 50 ms / div.



11.10 Open Loop Test

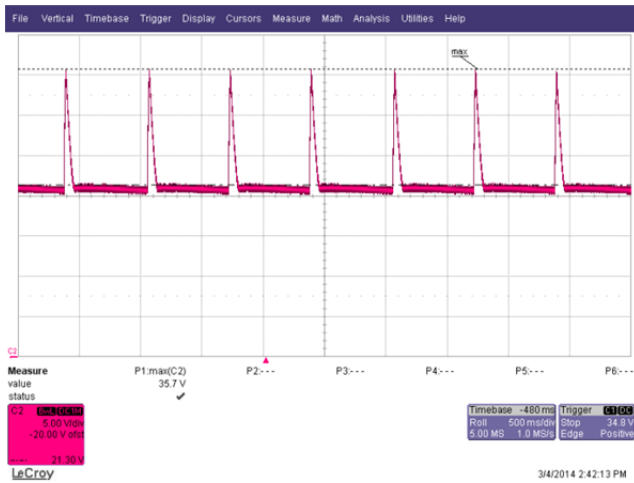


Figure 60 – 190 VAC Open Loop at No-Load.
 V_{OUT} , 5 V / div.
 Time Scale: 500 ms / div.

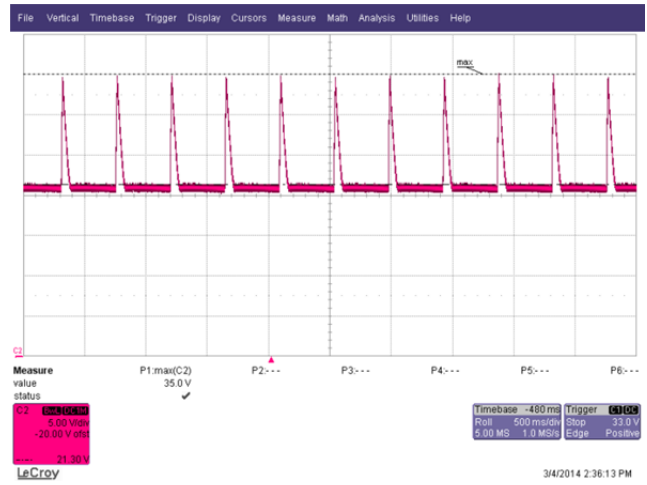


Figure 61 – 265 VAC Open Loop at No-Load.
 V_{OUT} , 5 V / div.
 Time Scale: 500 ms / div.

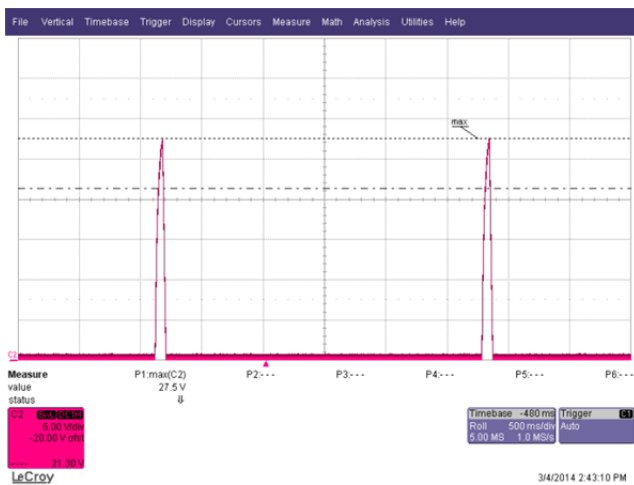


Figure 62 – 190 VAC Open Loop at Full-Load.
 V_{OUT} , 5 V / div.
 Time Scale: 500 ms / div.

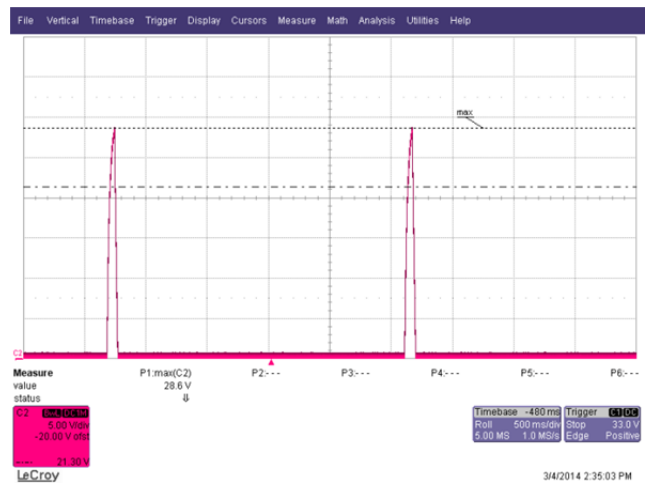


Figure 63 – 265 VAC Open Loop at Full-Load.
 V_{OUT} , 5 V / div.
 Time Scale: 500 ms / div.

11.11 Output Ripple Measurements

11.11.1 Ripple Measurement Technique

For DC output ripple measurements, a modified oscilloscope test probe must be utilized in order to reduce spurious signals due to pick-up. Details of the probe modification are provided in the Figures below.

The 4987BA probe adapter is affixed with two capacitors tied in parallel across the probe tip. The capacitors include one (1) 0.1 $\mu\text{F}/50\text{ V}$ ceramic type and one (1) 1.0 $\mu\text{F}/50\text{ V}$ aluminum electrolytic. The aluminum electrolytic type capacitor is polarized, so proper polarity across DC outputs must be maintained (see below).

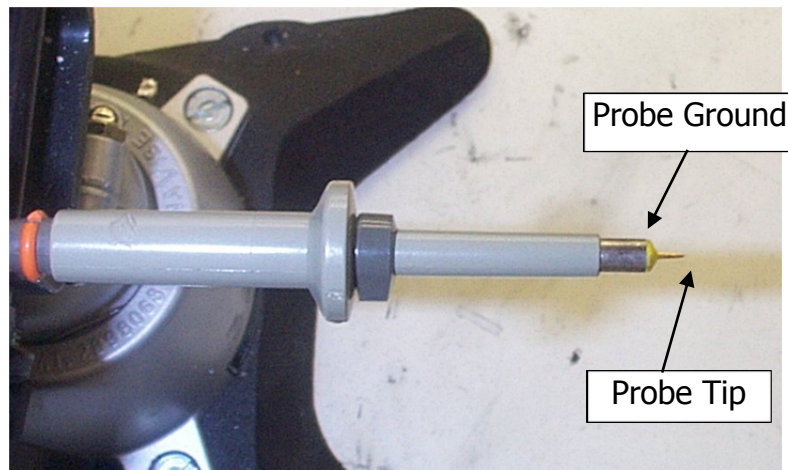


Figure 64 – Oscilloscope Probe Prepared for Ripple Measurement. (End Cap and Ground Lead Removed)

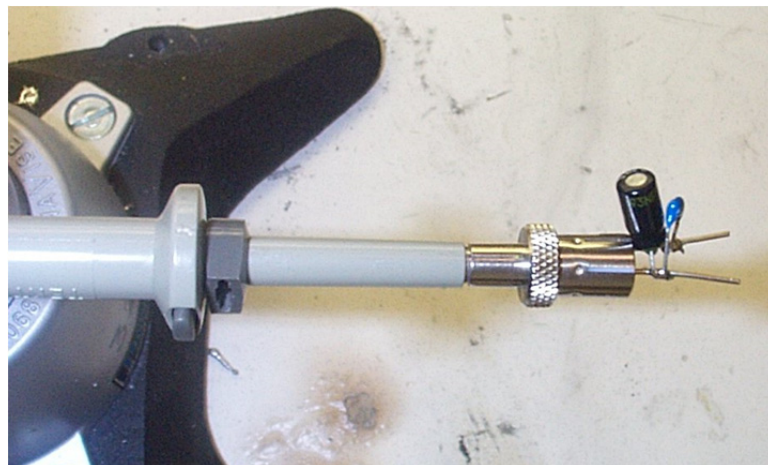


Figure 65 – Oscilloscope Probe with Probe Master (www.probemaster.com) 4987A BNC Adapter. (Modified with wires for ripple measurement, and two parallel decoupling capacitors added)

11.11.2 Measurement Results

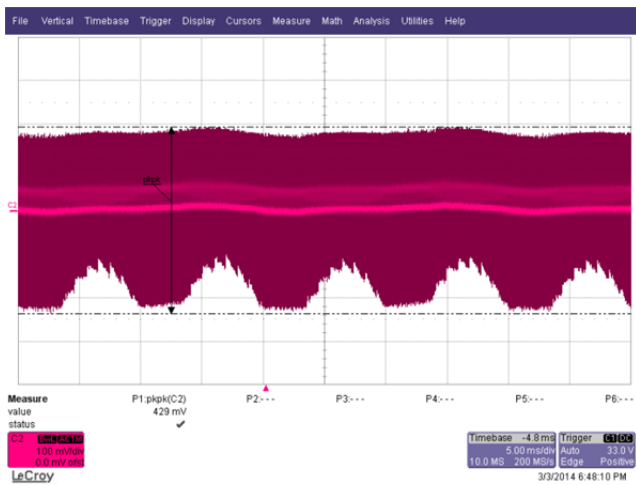


Figure 66 – Ripple, 190 VAC, Full Load.
5 ms, 100 mV / div.

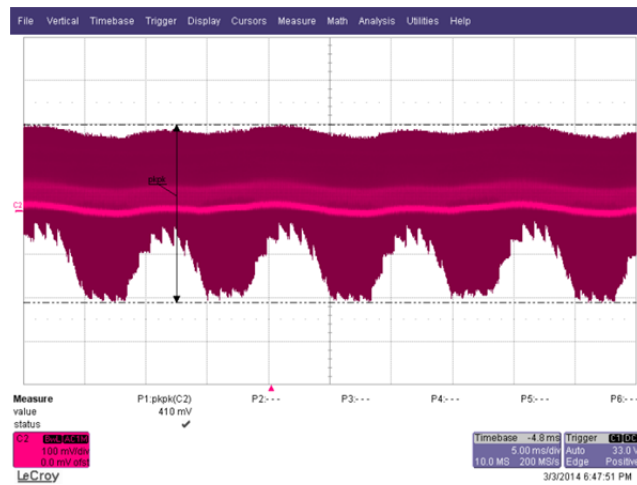


Figure 67 – Ripple, 265 VAC, Full Load.
5 ms, 100 mV / div.

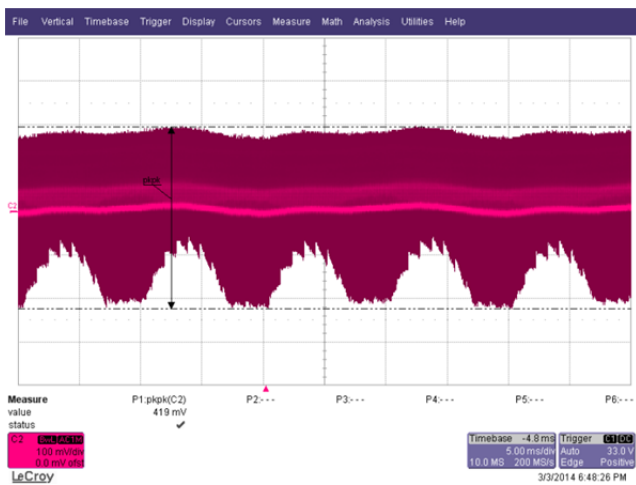


Figure 68 – Ripple, 230 VAC, Full Load.
5 ms, 100 mV / div.

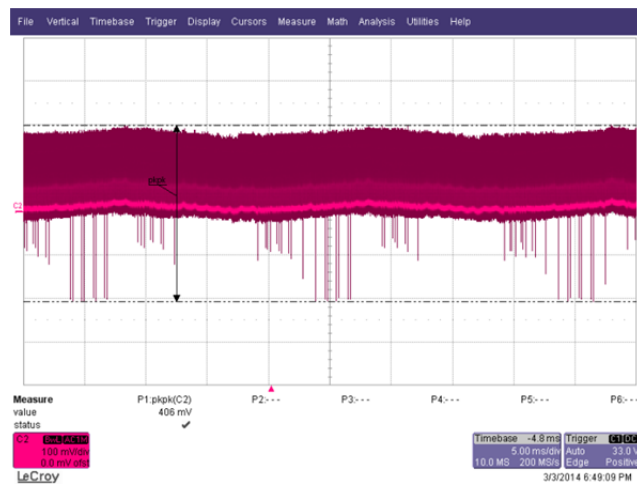


Figure 69 – Ripple, 230 VAC, 3/4 Full Load.
5 ms, 100 mV / div.

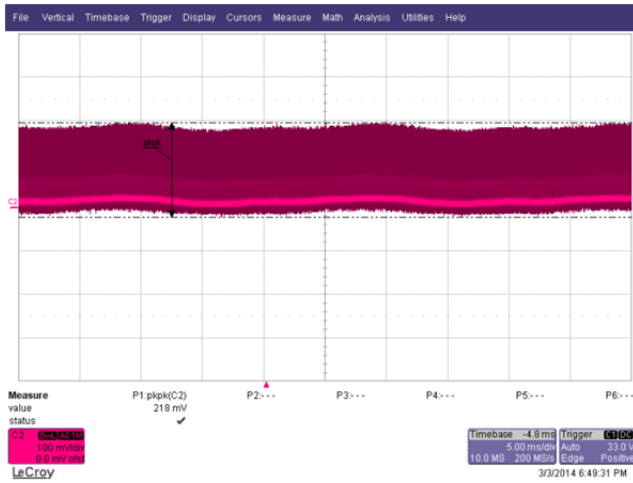


Figure 70 – Ripple, 230 VAC, 1/2 Full Load.
5 ms, 100 mV / div.

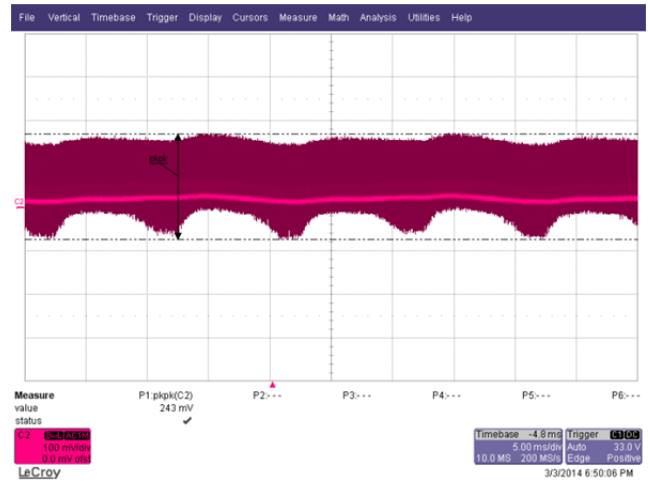


Figure 71 – Ripple, 230 VAC, 1/4 Full Load.
5 ms, 100 mV / div.

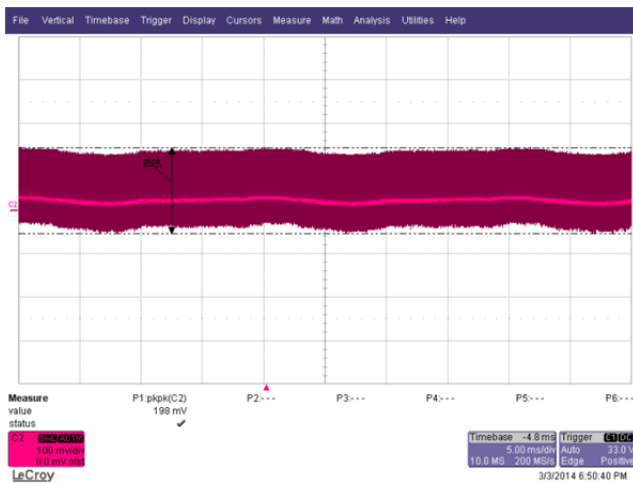


Figure 72 – Ripple, 230 VAC, 1/8 Full Load.
5 ms, 100 mV / div.

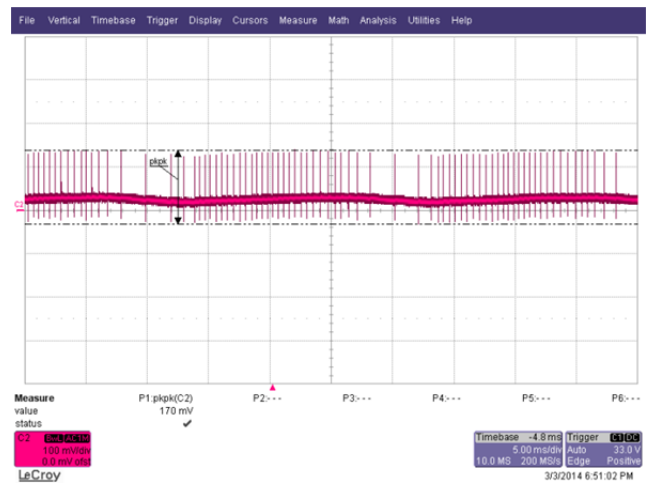


Figure 73 – Ripple, 230 VAC, No-Load.
5 ms, 100 mV / div.



13 Line Surge

Differential input line 1.2/50 μ s surge testing was completed on a single test unit to IEC61000-4-5. Input voltage was set at 230 VAC / 60 Hz. Output was loaded at full load and operation was verified following each surge event.

Surge Level (V)	Input Voltage (VAC)	Injection Location	Injection Phase (°)	Test Result (Pass/Fail)
+250	230	L to N	90	Pass
-250	230	L to N	90	Pass
+500	230	L to N	90	Pass
-500	230	L to N	90	Pass
+750	230	L to N	90	Pass
-750	230	L to N	90	Pass
+1000	230	L to N	90	Pass
-1000	230	L to N	90	Pass

Unit passes under all test conditions.

Differential Ring input line surge testing was completed on a single test unit to IEC61000-4-5. Input voltage was set at 230 VAC / 60 Hz. Output was loaded at full load and operation was verified following each surge event.

Surge Level (V)	Input Voltage (VAC)	Injection Location	Injection Phase (°)	Test Result (Pass/Fail)
+2500	230	L to N	90	Pass
-25000	230	L to N	90	Pass
+2500	230	L to N	0	Pass
-25000	230	L to N	0	Pass

Unit passes under all test conditions.



14 Conducted EMI



Power Integrations
20.Mar 14 13:19

RBW 9 kHz
MT 500 ms

Att 10 dB AUTO

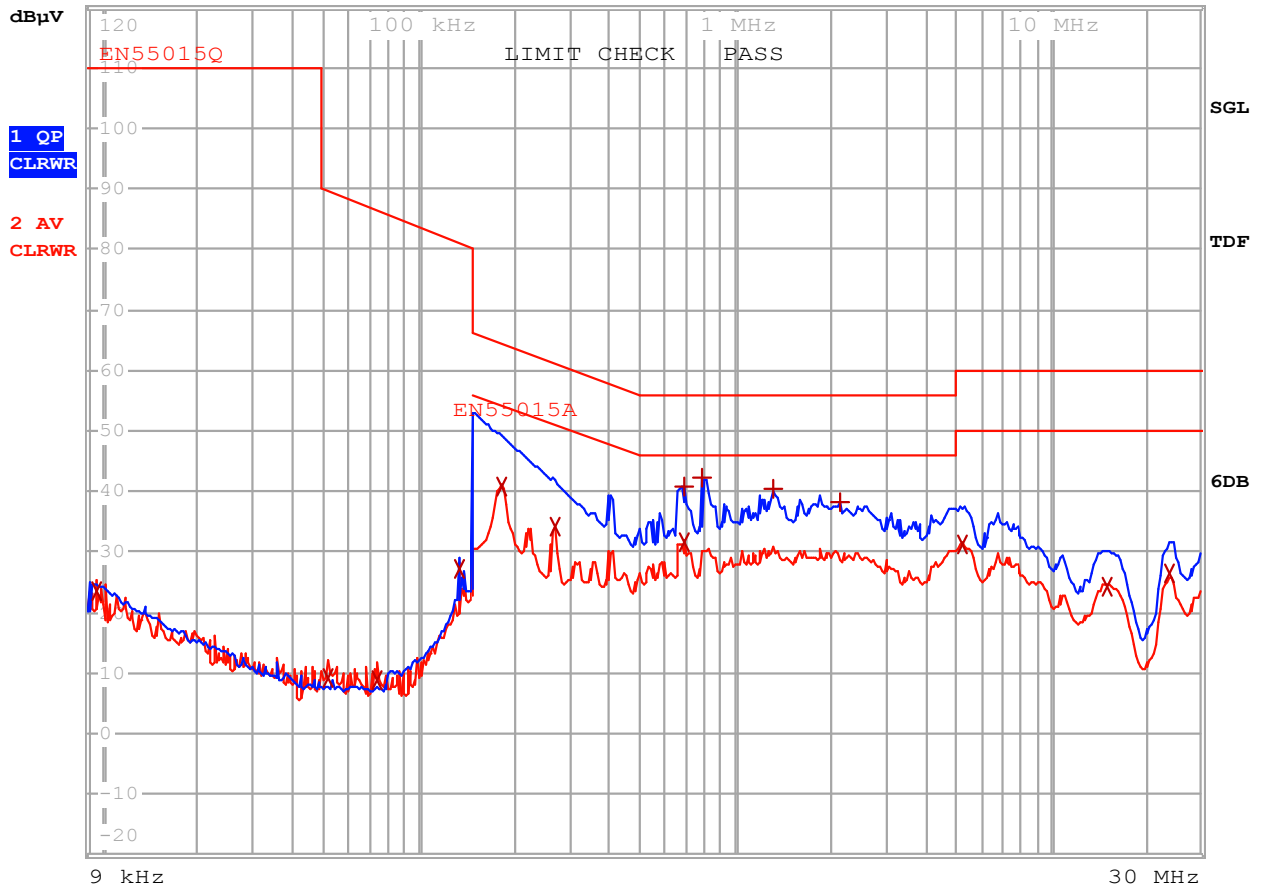


Figure 74 – Conducted EMI, Maximum Steady-State Load, 230 VAC, 60 Hz, and EN55015 B Limits. Unit on Top of Copper Plane.



EDIT PEAK LIST (Final Measurement Results)						
Trace1:	EN55015Q					
Trace2:	EN55015A					
Trace3:	---					
TRACE	FREQUENCY	LEVEL	dB μ V	DELTA	LIMIT	dB
2 Average	9.4590904509 kHz	23.72	L1 gnd			
2 Average	51.3431986431 kHz	9.32	L1 gnd			
2 Average	73.4602458683 kHz	8.87	L1 gnd			
2 Average	134.789536006 kHz	27.12	N gnd			
2 Average	183.028505992 kHz	40.98	N gnd	-13.36		
2 Average	269.806440381 kHz	34.16	N gnd	-16.96		
1 Quasi Peak	687.48218373 kHz	40.89	N gnd	-15.10		
2 Average	687.48218373 kHz	31.76	N gnd	-14.23		
1 Quasi Peak	790.243042258 kHz	42.18	N gnd	-13.81		
1 Quasi Peak	1.32578199726 MHz	40.35	N gnd	-15.64		
1 Quasi Peak	2.1374603093 MHz	38.12	N gnd	-17.87		
2 Average	5.23385515413 MHz	31.40	N gnd	-18.59		
2 Average	15.0275202 MHz	24.45	N gnd	-25.55		
2 Average	23.7503773643 MHz	26.52	L1 gnd	-23.47		

Table 4 – Conducted EMI, Maximum Steady-State Load, 230 VAC, 60 Hz, and EN55015 B Limits. Unit on Top of Copper Plane.



Power Integrations
20.Mar 14 12:35

RBW 9 kHz
MT 500 ms

Att 10 dB AUTO

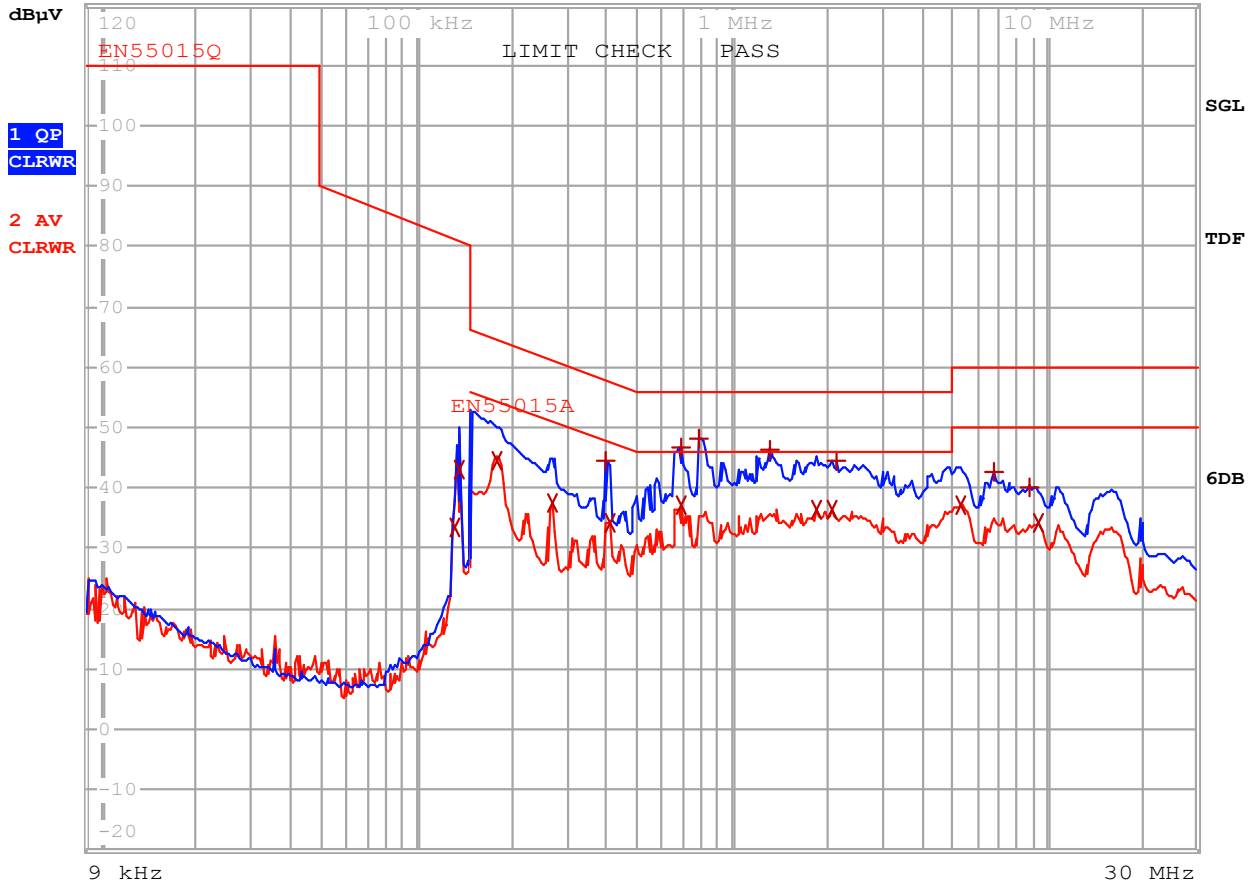


Figure 75 – Conducted EMI, Maximum Steady-State Load, 230 VAC, 60 Hz, and EN55015 B Limits. Unit on Top of Copper Plane that is Connected to Earth.



EDIT PEAK LIST (Final Measurement Results)

Trace1: EN55015Q
 Trace2: EN55015A
 Trace3: ---

	TRACE	FREQUENCY	LEVEL dBµV	DELTA LIMIT dB
2	Average	130.825395691 kHz	33.39 N gnd	
2	Average	136.137431366 kHz	43.13 N gnd	
2	Average	179.422121353 kHz	44.63 N gnd	-9.88
2	Average	269.806440381 kHz	37.40 N gnd	-13.72
1	Quasi Peak	397.727746704 kHz	44.42 N gnd	-13.47
2	Average	409.779295157 kHz	34.21 N gnd	-13.43
1	Quasi Peak	687.48218373 kHz	46.75 N gnd	-9.24
2	Average	687.48218373 kHz	37.01 N gnd	-8.98
1	Quasi Peak	790.243042258 kHz	48.05 N gnd	-7.94
1	Quasi Peak	1.32578199726 MHz	46.42 N gnd	-9.57
2	Average	1.84110031489 MHz	36.42 N gnd	-9.57
2	Average	2.0745979178 MHz	36.39 N gnd	-9.60
1	Quasi Peak	2.1588349124 MHz	44.56 N gnd	-11.43
2	Average	5.28619370567 MHz	36.97 N gnd	-13.02
1	Quasi Peak	6.77918394001 MHz	42.52 N gnd	-17.47
1	Quasi Peak	8.86858861671 MHz	40.08 N gnd	-19.91
2	Average	9.32097576636 MHz	34.03 N gnd	-15.96

Table 5 – Conducted EMI, Maximum Steady-State Load, 230 VAC, 60 Hz, and EN55015 B Limits. Unit on Top of Copper Plane that is Connected to Earth.



15 Revision History

Date	Author	Revision	Description & changes	Reviewed
07-Nov-14	JdC	1.0	Initial Release	Apps & Mktg



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Power Integrations Worldwide Sales Support Locations

WORLD HEADQUARTERS

5245 Hellyer Avenue
San Jose, CA 95138, USA.
Main: +1-408-414-9200
Customer Service:
Phone: +1-408-414-9665
Fax: +1-408-414-9765
e-mail: usasales@powerint.com

CHINA (SHANGHAI)

Rm 2410, Charity Plaza, No. 88,
North Caoxi Road,
Shanghai, PRC 200030
Phone: +86-21-6354-6323
Fax: +86-21-6354-6325
e-mail: chinasales@powerint.com

CHINA (SHENZHEN)

17/F, Hivac Building, No. 2, Keji
Nan 8th Road, Nanshan District,
Shenzhen, China, 518057
Phone: +86-755-8672-8689
Fax: +86-755-8672-8690
e-mail: chinasales@powerint.com

GERMANY

Lindwurmstrasse 114
80337, Munich
Germany
Phone: +49-895-527-39110
Fax: +49-895-527-39200
e-mail: eurosales@powerint.com

INDIA

#1, 14th Main Road
Vasanthanagar
Bangalore-560052
India
Phone: +91-80-4113-8020
Fax: +91-80-4113-8023
e-mail: indiasales@powerint.com

ITALY

Via Milanese 20, 3rd. Fl.
20099 Sesto San Giovanni
(MI) Italy
Phone: +39-024-550-8701
Fax: +39-028-928-6009
e-mail: eurosales@powerint.com

JAPAN

Kosei Dai-3 Building
2-12-11, Shin-Yokohama,
Kohoku-ku, Yokohama-shi,
Kanagawa 222-0033
Japan
Phone: +81-45-471-1021
Fax: +81-45-471-3717
e-mail: japansales@powerint.com

KOREA

RM 602, 6FL
Korea City Air Terminal B/D,
159-6
Samsung-Dong, Kangnam-Gu,
Seoul, 135-728 Korea
Phone: +82-2-2016-6610
Fax: +82-2-2016-6630
e-mail: koreasales@powerint.com

SINGAPORE

51 Newton Road,
#19-01/05 Goldhill Plaza
Singapore, 308900
Phone: +65-6358-2160
Fax: +65-6358-2015
e-mail: singaporesales@powerint.com

TAIWAN

5F, No. 318, Nei Hu Rd.,
Sec. 1
Nei Hu District
Taipei 11493, Taiwan R.O.C.
Phone: +886-2-2659-4570
Fax: +886-2-2659-4550
e-mail: taiwansales@powerint.com

UK

First Floor, Unit 15, Meadway
Court, Rutherford Close,
Stevenage, Herts. SG1 2EF
United Kingdom
Phone: +44 (0) 1252-730-141
Fax: +44 (0) 1252-727-689
e-mail: eurosales@powerint.com

APPLICATIONS HOTLINE

World Wide +1-408-414-9660

APPLICATIONS FAX

World Wide +1-408-414-9760

