

Design Example Report

Title	<i>30 W Power Supply Using InnoSwitch3™-CP INN3268C-H202</i>
Specification	90 VAC – 132 VAC Input; 5.1 V / 6 A, 9.2 V / 3.3 A, 15.3 V / 2 A Output
Application	AC Outlet with USB Ports
Author	Applications Engineering Department
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Summary and Features

- 30 W compact power supply for high power USB Type-A/C port charging
- >90% average efficiency at nominal AC input
- <30 mW no-load input power
- All the benefits of secondary side control with the simplicity of primary side regulation
 - Insensitive to transformer variation
 - Extremely fast transient response independent of load timing
- Synchronous rectification for higher efficiency
- Accurate thermal protection with hysteretic shutdown
- Input voltage monitor with accurate brown-in/brown-out and overvoltage protection
- Meets IEC 2.0 kV common mode surge, 1.0 kV differential surge and EN55022 conducted EMI

PATENT INFORMATION

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Power Integrations

5245 Hellyer Avenue, San Jose, CA 95138 USA.
Tel: +1 408 414 9200 Fax: +1 408 414 9201
www.power.com

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Important Note: Although this board is designed to satisfy safety isolation requirements, the engineering prototype has not been agency approved. Therefore, all testing should be performed using an isolation transformer to provide the AC input to the prototype board.



1 Introduction

This engineering report describes an output power supply intended for USB wall outlet charger. The 30 W output (selectable 5.1 V / 6 A or 9.2 V / 3.3 A or 15.3 V / 2 A) rail is designed for a high power USB charging with Type-A or Type-C ports. The output utilizes INN3268C from the InnoSwitch3-CP family of ICs. This design shows high power density and efficiency that is possible due to the high level of integration of the InnoSwitch3-CP controller providing exceptional performance.

DER-631 is a low-line input flyback converter design. The key design goals were high power density, high efficiency, low no load consumption, and best in class thermal performance. This is intended for wall outlet USB chargers.

This document contains the power supply specification, schematic diagram, bill of materials, printed circuit layout, and performance data.

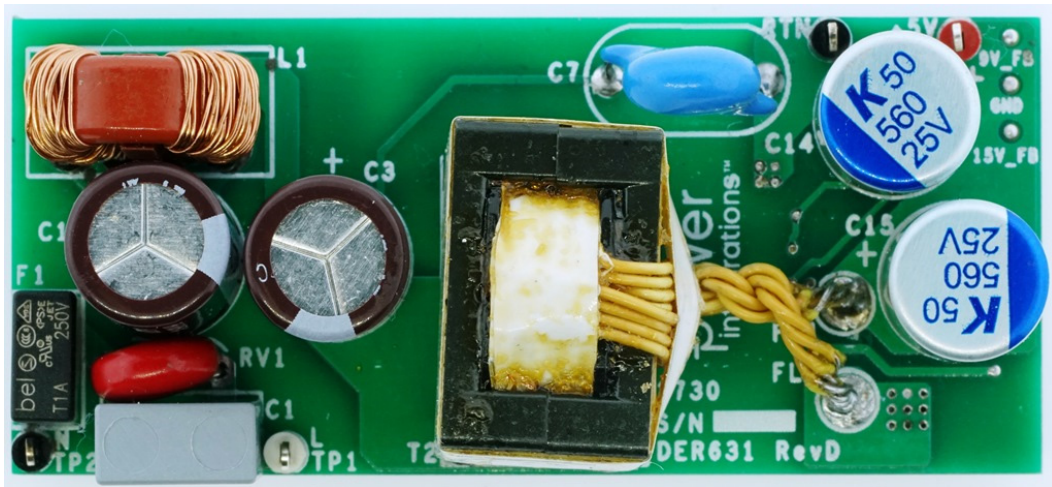


Figure 1 – Populated Circuit Board, Top View.

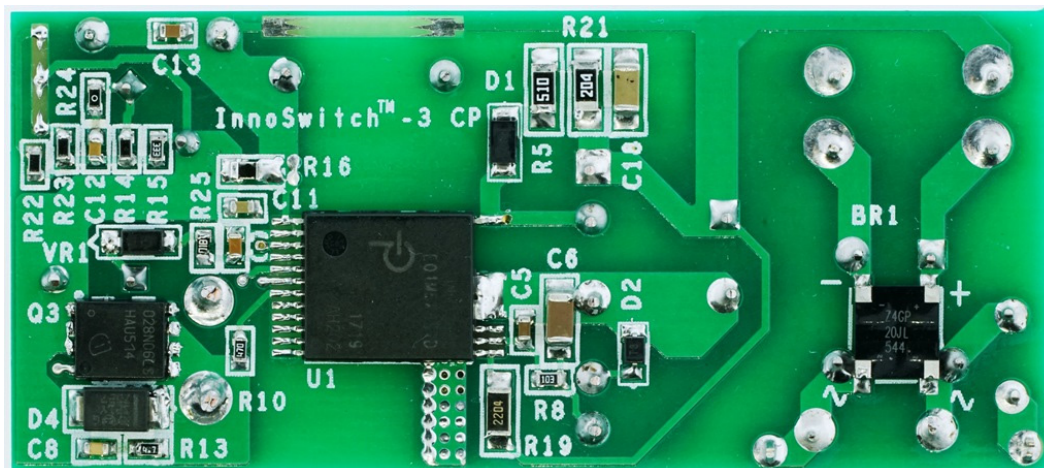


Figure 2 – Populated Circuit Board, Bottom View.

2 Power Supply Specification

The table below represents the minimum acceptable performance of the design. Actual performance is listed in the results section.

Description	Symbol	Min	Typ	Max	Units	Comment
Input						
Voltage	V_{IN}	100	115	132	VAC	2 Wire – no P.E.
Frequency	f_{LINE}	47	60	63	Hz	
No-load Input Power (115 VAC)				30	mW	Measured at 115 VAC.
5 V Output						
Output Voltage	V_{OUT}		5.1		V	±3%
Output Ripple Voltage	V_{RIPPLE}			150	mV	At End of Cable. Cable Needs a Resistance of 100 mΩ.
Output Current	I_{OUT}	6		6.3	A	20 MHz Bandwidth.
9 V Output						
Output Voltage	V_{OUT}		9.2		V	±5%
Output Ripple Voltage	V_{RIPPLE}			150	mV	At End of Cable. Cable Needs a Resistance of 100 mΩ.
Output Current	I_{OUT}			3.3	A	20 MHz Bandwidth.
15 V Output						
Output Voltage	V_{OUT}		15.3		V	±5%
Output Ripple Voltage	V_{RIPPLE}			150	mV	At End of Cable. Cable Needs a Resistance of 100 mΩ.
Output Current	I_{OUT}			2	A	20 MHz Bandwidth.
Continuous Output Power	P_{OUT}			30	W	
Conducted EMI						
Safety						Meets CISPR22B / EN55022B Designed to meet IEC60950 / UL1950 Class II
Ambient Temperature	T_{AMB}	0		50	°C	Free Convection, Sea Level.

3 Schematic

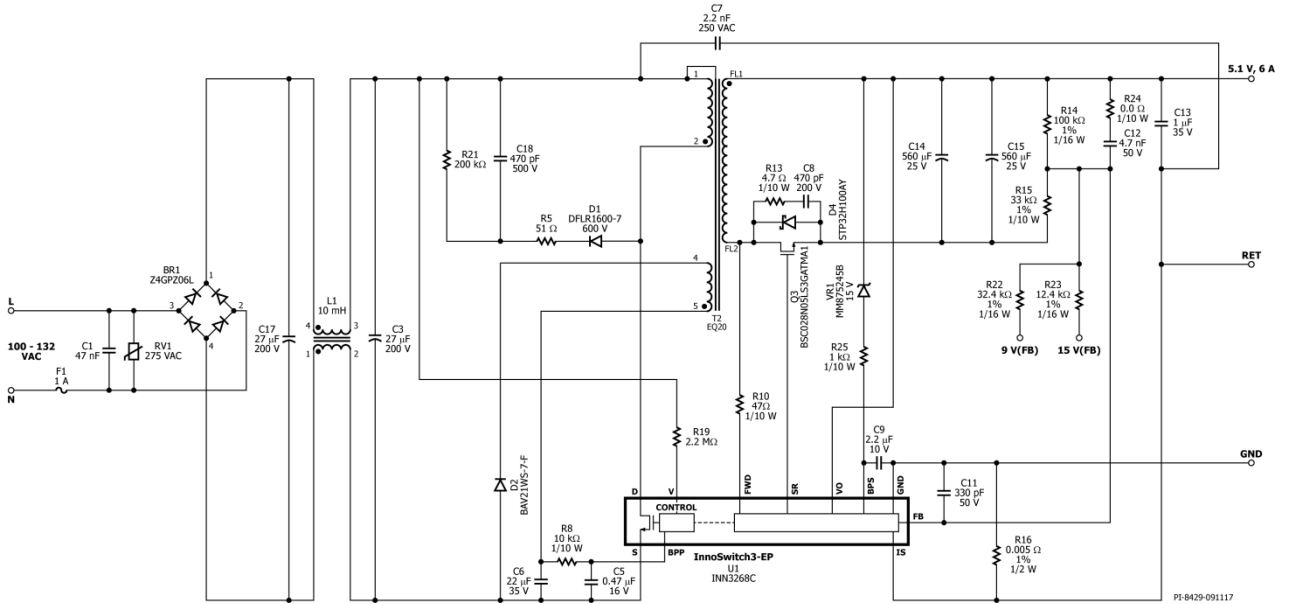


Figure 3 – Schematic.

4 Circuit Description

The InnoSwitch3-CP IC combines primary, secondary and feedback circuits in a single surface mounted off-line flyback switcher IC. The IC incorporates the primary MOSFET, the primary-side controller, the secondary-side controller for synchronous rectification and the Fluxlink™ technology that eliminates the need for an optocoupler needed on a secondary sensed feedback system.

4.1 Input Circuit Description

Fuse F1 isolates the circuit and provides protection from component failure, and the capacitor C1 provides attenuation for EMI. Common mode inductor L1 and capacitors C3 and C17 form a π -filter that provides filtering for both common mode and differential mode noise. Bridge rectifiers BR1 rectifies the AC line voltage and provides a full wave rectified DC across the input capacitors C3 and C17.

4.2 Primary Circuit

One end of the transformer T2 primary is connected to the rectified DC bus; the other is connected to the drain terminal of the MOSFET inside the INN3268C (U1).

A low cost RCD clamp formed by diode D1, resistors R5 and R21, and capacitor C18 limits the peak Drain voltage of U1 at the instant turn-off of the MOSFET. The clamp helps dissipate the energy stored in the leakage reactance of transformer T2.

The IC is kick-started by an internal high-voltage current source that charges the BPP pin capacitor C5 when AC is first applied. During normal operation the primary-side block is powered from an auxiliary winding on the transformer. The output of this is configured as a flyback winding which is rectified and filtered using diode D2 and capacitor C6. Resistor R8 limits the current being supplied to the BPP pin of the InnoSwitch3-CP (U1). An R-C network can be placed across D2 to offer damping of the high frequency ringing, which can reduce radiated EMI.

The primary-side controller has a current limit threshold ramp that is inversely proportional to time from the end of the last primary switching cycle. The nature of this characteristic introduces a primary current limit that reduces as the switching frequency reduces. It is similar to the state machine of ON/OFF control but the reduction is now linear in nature rather than the discrete jumps in current limit that the ON/OFF state machine introduces. This produces a primary MOSFET switching pulse train that looks similar to a traditional PWM waveform under steady state conditions with consistent time and peak current between cycles rather than the ON/OFF cycle skipping.

This algorithm enables the most efficient use of the primary switch with the benefit that this algorithm responds to digital feedback information where the start of the next switching cycle is immediate when a feedback switching cycle request is received.

Resistor R19 provides line voltage sensing and supplies a current to the V pin of U1, which is proportional to the DC voltage across capacitor C3. At approximately 55 V DC, the current through this resistor exceeds the line undervoltage threshold, which results in enabling of U1. At approximately 250 V DC, the current through this resistor exceeds the line overvoltage threshold, which results in disabling of U1.

4.3 *Secondary Circuit*

The secondary-side of the INN3268C IC provides output voltage, output current sensing and drive a MOSFET providing synchronous rectification. The secondary of the transformer is rectified by MOSFET Q3 and filtered by capacitors C14 and C15. High frequency ringing during switching transients that would otherwise create radiated EMI is reduced via RC snubber, R13 and C8.

The gate of Q3 is turned on by the secondary-side controller inside IC U1, based on the winding voltage sensed via resistor R10 and fed into the FWD pin of the IC.

In continuous conduction mode operation, the power MOSFET is turned off just prior to the secondary-side controller commanding a new switching cycle from the primary. In discontinuous mode the MOSFET is turned off when the voltage drop across the MOSFET falls below ground. Secondary-side control of the primary-side MOSFET ensures that it is never on at the same time with the synchronous rectification MOSFET on time. The MOSFET drive signal is the output on the SR pin.

The secondary side of the IC is self-powered from either the secondary winding forward voltage or the output voltage. The output voltage powers the device then fed into VO pin and charges the decoupling capacitor C9 via an internal regulator.

During CC operation, when the output voltage falls, the device will power itself from the secondary winding directly. During the on-time of the primary-side power MOSFET, the forward voltage that appears across the secondary winding is used to charge the decoupling capacitor C9 via resistor R10 and an internal regulator. This allows output current regulation to be maintained down to ~3.0 V. Below this level the unit enters auto-restart until the output load is reduced.

Output current is sensed by monitoring the voltage drop across resistors R16 between the IS and GND pins with a threshold of approximately 30 mV to reduce losses. Once the internal current sense threshold is exceeded the device adjusts the number of switch pulses to maintain a fixed output current. If no fixed current requirement, the IS and GND pins can be shorted.

Below the CC threshold, the device operates in constant voltage mode. Output voltage is regulated so as to achieve an internal reference voltage of 1.265 V on the FB pin. Capacitor C12 form a phase-lead network that ensures stable operation and minimizes

output voltage overshoot and undershoot during transient load conditions. Capacitor C11 provides noise filtering of the signal at the FB pin.

Resistors R14 and R15 form the feedback divider network to sense the output voltage. To change the output to 9 V, resistor R22 is added in parallel to the bottom resistor R15. And to change the output to 15 V, resistor R23 is added in parallel to the bottom resistor R15. To vary the output voltage using a USB PD interface, the ports must be connected to the terminals 9V_FB and GND to make it a 9 V output and to the terminals 15V_FB and GND to make it a 15 V output.

VR1 protects the power supply from output overvoltage. If the output voltage exceeds VR1 + BPS voltage, current will flow through the BPS pin that will result to auto-restart. A 15 V Zener regulator was used to not exceed the voltage rating of the output capacitors.

In order to improve conversion efficiency and reduce switching losses, InnoSwitch3-CP introduces a secondary-based QR functionality. The secondary controller has a means to allow switching when the voltage across the primary switch is near its minimum voltage when the converter operates in critical (CRM) or discontinuous conduction mode (DCM). Rather than detecting the magnetizing ring valley on the primary-side, the peak voltage of the FW pin voltage as it rises above the output voltage level is used to gate secondary request to initiate the switch “on” cycle in the primary controller.

4.4 *Design Key Points*

The design targets greater than 90% average efficiency for the 3 outputs. Efficiency was optimized with transformer design, chosen active devices and bias voltages. For the transformer design, it is best to keep the reflected voltage (VOR) low to decrease the RMS current on the secondary side. Lower VOR also means lower drain to source voltage on the primary side MOSFET that can reduce switching loss. In this design, the VOR was set to 50 V for the 5 V output. This will make the operation of the 5 V output in continuous mode (CCM), but this will ensure the 9 V and 15 V output operations in discontinuous mode (DCM) with valley switching. InnoSwitch3-CP switches up to the 4th valley to achieve better efficiency. Always note that further lowering the VOR can lead to a very large leading edge spike on the primary current because of deep CCM operation. This can trigger the SOA peak limit protection that will result to auto-restart.

Aside from the VOR consideration it is also important to lower the leakage inductance of the transformer. The energy being stored in the leakage inductance which is dissipated on the clamping circuit contributes to lower efficiency. Reducing the leakage is an utmost important in this design, to significantly increase the efficiency. A sandwich winding was used to lower the leakage inductance to a value less than 5 μH (< 2% of magnetizing inductance). Detailed transformer construction is described on section 7 of this report.



For higher efficiency, it is also necessary to choose the active devices that offer lower conduction losses. For the InnoSwitch3-CP family, INN3268C offers the lowest $R_{DS(ON)}$. For the secondary rectifier (SR), a MOSFET was chosen instead of a Schottky diode. A MOSFET of 2.8 m Ω $R_{DS(ON)}$ was used in the design. An added Schottky diode in parallel with the SR MOSFET gives a slight improvement on the efficiency. This diode conducts instead of the MOSFET body diode during the start of secondary MOSFET ON and before the secondary current reaches zero or secondary MOSFET OFF. These delays on transition are needed to avoid cross-conduction with the primary MOSFET.

The sweet spot (efficiency and small form factor consideration) for switching frequency operation is at the range from 70 kHz to 80 kHz. An EQ20 transformer with AE of 60 mm² is enough without saturating the core. The design chooses the minimum number of secondary turns at 390 mT flux density.

Auxiliary bias voltage was chosen at range from 8 V to 10 V at no-load condition. This helps improve no load consumption as well as light load efficiency.

5 PCB Layout

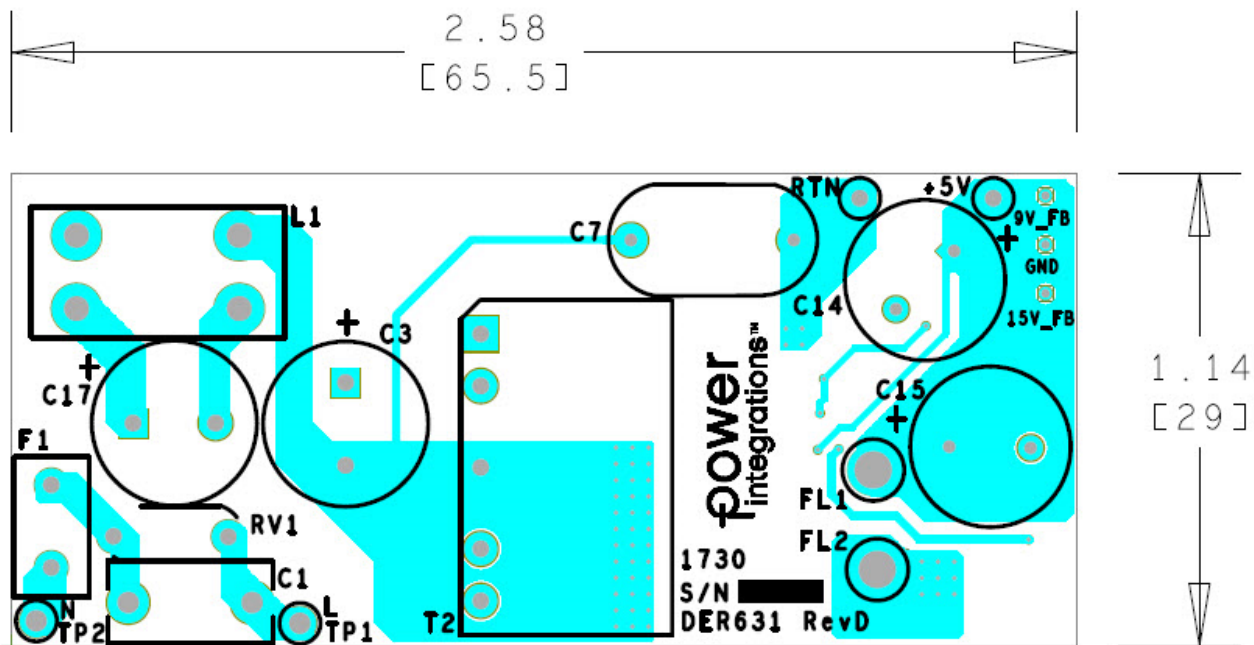


Figure 4 – Top Side.

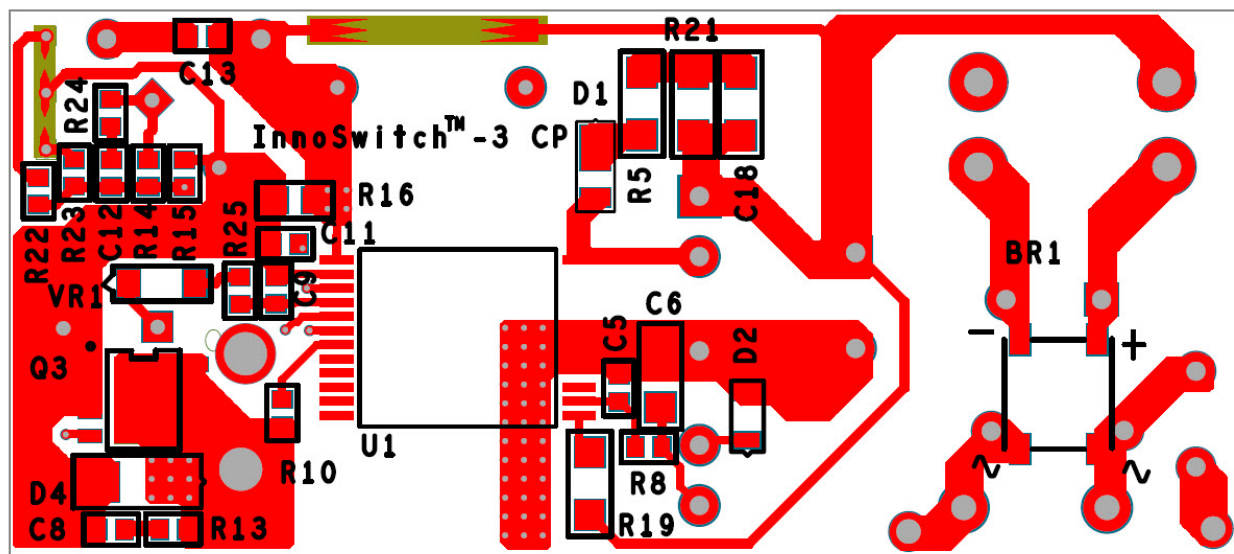


Figure 5 – Bottom Side.



6 Bill of Materials

Item	Qty	Ref Des	Description	Mfg Part Number	Mfg
1	1	BR1	RECT BRIDGE, GP, 600V, 2A, Z4-D	Z4GP206L-HF	Comchip
2	1	C1	47 nF, 310 VAC, Polyester Film, X2	BFC233920473	Vishay
3	2	C3 C17	27 μ F, 200 V, Electrolytic, (10 x 16),	EKXJ201ELL270MJ16S	Nippon Chemi-Con
4	1	C5	0.47 μ F, 10%, 16V, X7R, 0603	GRM188R71C474KA88D	Murata
5	1	C6	22 μ F, 35 V, Ceramic, X5R, 1206	C3216X5R1V226M160AC	TDK
6	1	C7	2.2 nF, Ceramic, Y1	CD90ZU2GA222MYNKA	TDK
7	1	C8	470 pF, 200 V, Ceramic, X7R, 0603	06032C471KAT2A	AVX
8	1	C9	2.2 μ F, 10 V, Ceramic, X7R, 0603	GRM188R71A225KE15D	Murata
9	1	C11	330 pF 50 V, Ceramic, X7R, 0603	CC0603KRX7R9BB331	Yageo
10	1	C12	4.7 nF 50 V, Ceramic, X7R, 0603	GRM188R71H472KA01D	Murata
11	1	C13	1 μ F 35 V, Ceramic, X7R, 0603	C1608X7R1V105M	TDK
12	2	C14 C15	560 μ F, 25 V, \pm 20%, Al Organic Polymer,	A750MS567M1EAAE015	Kemet
13	1	C18	470 pF, \pm 10%, 500 V, X7R, Ceramic Capacitor,	CC1206KKX7RBBB471	Yageo
14	1	D1	600 V, 1 A, Rectifier, Glass Passivated, POWERD1123	DFLR1600-7	Diodes, Inc.
15	1	D2	250 V, 0.2 A, Fast Switching, 50 ns, SOD-323	BAV21WS-7-F	Diode, Inc.
16	1	D4	100 V, 2 A, Schottky, SMA	STPS2H100AY	ST Micro
17	1	F1	1 A, 250 V, Slow, Long Time Lag, RST 1	RST 1	Belfuse
18	1	L1	10 mH, 0.7 A, Common Mode Choke	744821110	Würth
19	1	Q3	MOSFET, N-CH, 60 V, 100 A, SMD, PG-TDSON-8	BSC028N06LS3GATMA1	Infineon
20	1	R5	RES, 51 Ω , 5%, 1/4 W, Thick Film, 1206	ERJ-8GEYJ510V	Panasonic
21	1	R8	RES, 10 k Ω , 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ103V	Panasonic
22	1	R10	RES, 47 Ω , 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ470V	Panasonic
23	1	R13	RES, 4.7 Ω , 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ4R7V	Panasonic
24	1	R14	RES, 100 k Ω , 1%, 1/16 W, Thick Film, 0603	ERJ-3EKF1003V	Panasonic
25	1	R15	RES, SMD, 33 k Ω , 1%, 1/10 W, \pm 100ppm/ $^{\circ}$ C, 0603	RC0603FR-0733KL	Yageo
26	1	R16	RES, 0.005 Ω , 0.5 W, 1%, 0805	PMR10EZPFU5L00	Rohm
27	1	R19	RES, 2.2 M Ω , 5%, 1/4 W, Thick Film, 1206	ERJ-8GEYJ225V	Panasonic
28	1	R21	RES, 200 k Ω , 5%, 1/4 W, Thick Film, 1206	ERJ-8GEYJ204V	Panasonic
29	1	R22	RES, 32.4 k Ω , 1%, 1/16 W, Thick Film, 0603	ERJ-3EKF3242V	Panasonic
30	1	R23	RES, 12.4 k Ω , 1%, 1/16 W, Thick Film, 0603	ERJ-3EKF1242V	Panasonic
31	1	R24	RES, 0 Ω , 5%, 1/10 W, Thick Film, 0603	ERJ-3GEY0R00V	Panasonic
32	1	R25	RES, 1 k Ω , 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ102V	Panasonic
33	1	RV1	275 VAC, 23 J, 7 mm, RADIAL	V275LA4P	Littlefuse
34	1	T2	Bobbin, EQ20, 10 pins, 5pri, 5sec	P-2042	Pinshine
35	1	U1	InnoSwitch3-CP, InSOP24	INN3268C-H202	Power Integrations
36	1	VR1	15 V, 5%, 500 mW, SOD-123	MMSZ5245B-E3-08	Vishay

7 Transformer (T2) Specification

7.1 Electrical Diagram

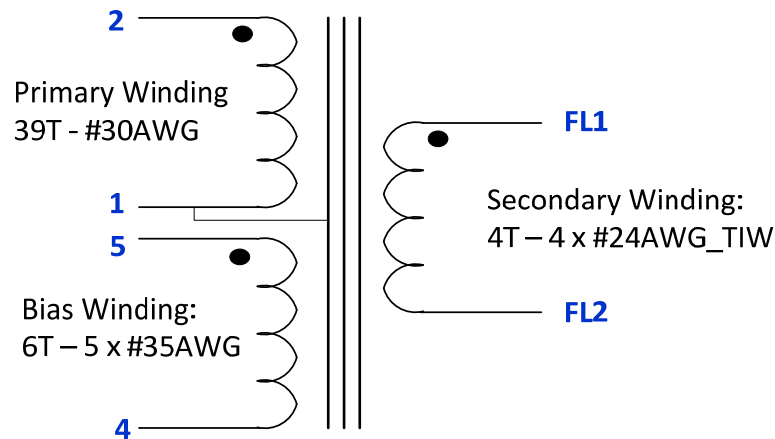


Figure 6 – Transformer Electrical Diagram.

7.2 Electrical Specifications

Electrical Strength	1 second, 60 Hz, from pins 1, 2, 4 and 5 to FL1, FL2.	3000 VAC
Primary Inductance	Pins 1-2, all other open, measured at 100 kHz, 0.4 V _{RMS} .	490 μH, ±5%
Primary Leakage	Pins 1-2, with FL1-FL2 shorted, measured at 100 kHz, 0.4 V _{RMS} .	7μH (Max.)

7.3 Material List

Item	Description
[1]	Core: EQ20.
[2]	Bobbin: EQ20, Horizontal, 10 Pins.
[3]	Magnet Wire: #30 AWG Double Coated, Solderable.
[4]	Magnet Wire: #35 AWG Double Coated, Solderable.
[5]	Magnet Wire: #24 AWG Triple Insulated Wire.
[6]	Tape: 3M 1298 Polyester Film, 1 mil Thick, 6 mm Wide.
[7]	Varnish: Dolph BC-359.

7.4 Transformer Build Diagram

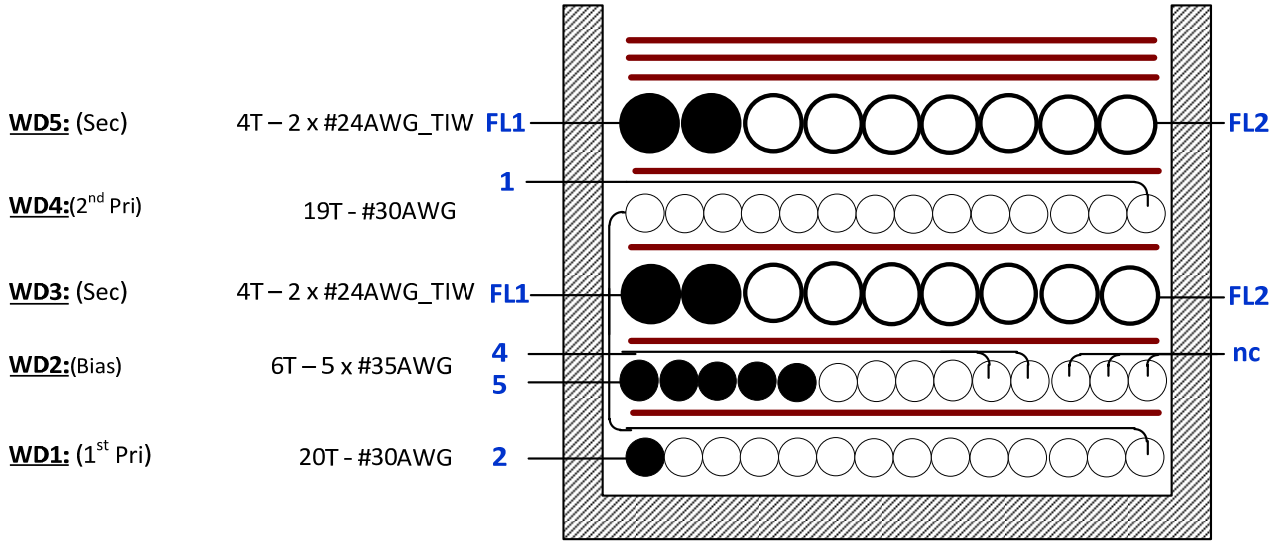


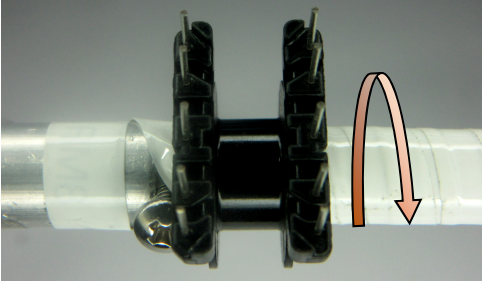
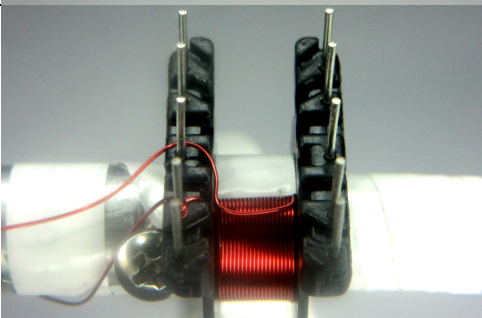
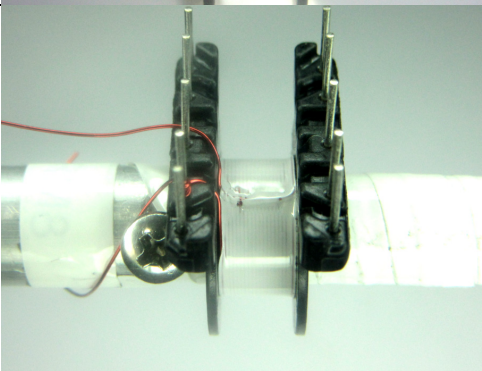
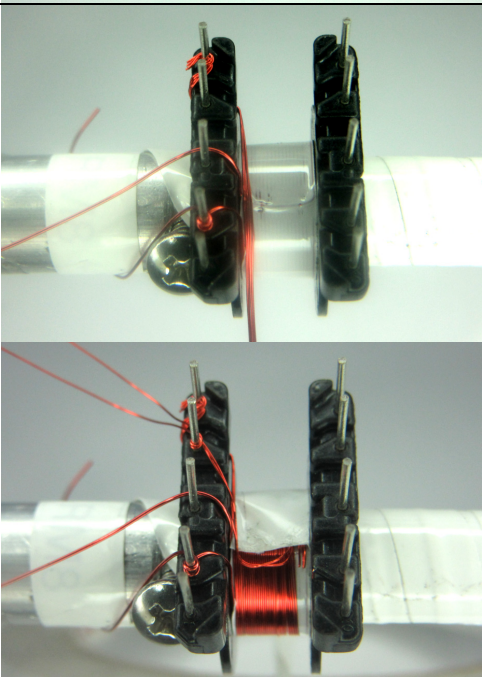
Figure 7 – Transformer Build Diagram.

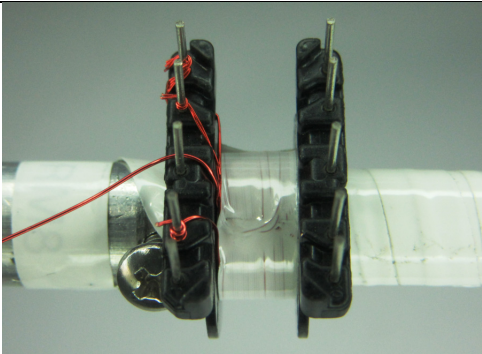
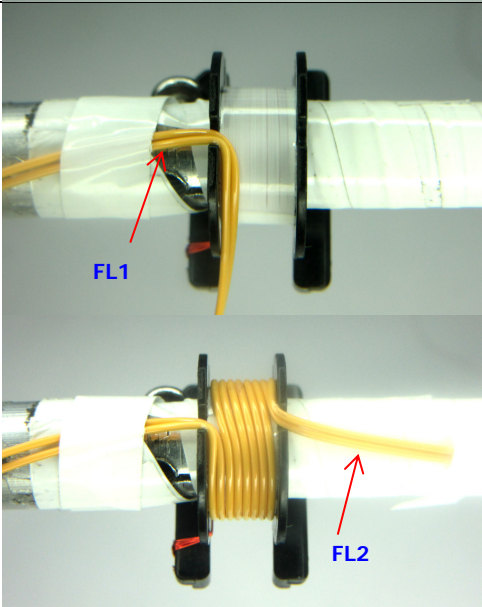
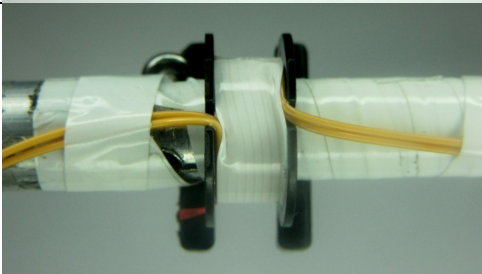
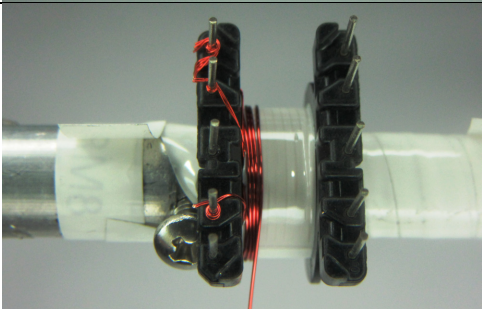
7.5 Transformer Construction

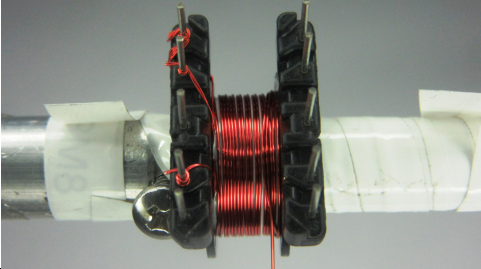
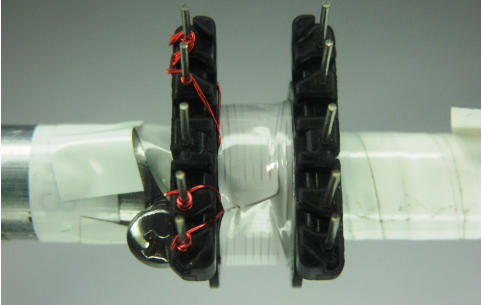
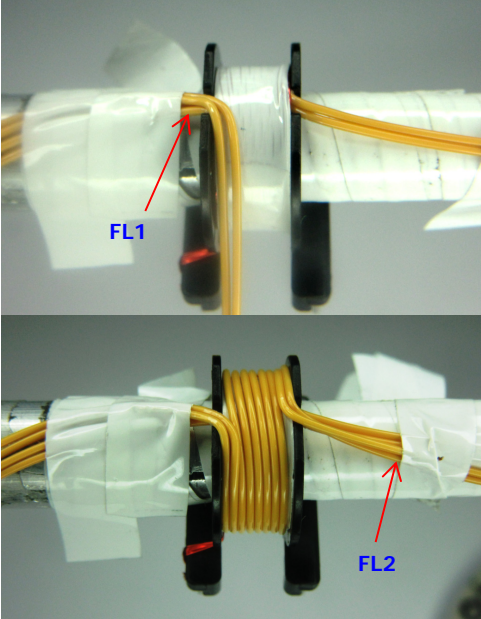
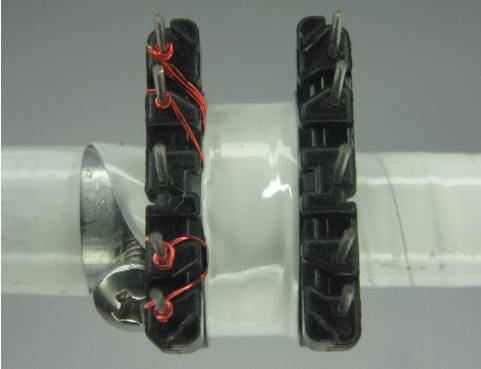
Winding preparation	Place the bobbin Item [2] on the mandrel with the pin side is on the left side. Winding direction is clockwise direction.
WD1 1st Primary	Start at pin 2, wind 20 turns of wire Item [3] in 1 layer. At the last turn, bring wire back to the left side.
Insulation	Place 1 layer of tape Item [6] for insulation.
WD2 Bias/Shield	Start at pin 5, wind 6 (5-filars) turns of wire Item [4] in 1 layer. At the last turn, bring bifilar wire back to the left finish at pin 4. Cut the remaining trifilar wire then no connect.
Insulation	Place 1 layer of tape Item [6] for insulation.
WD3 Secondary	Start at FL1 from the left side of the bobbin, wind 4 bifilar turns of wire Item [5] in 1 layer. At the last turn, finish winding at FL2.
Insulation	Place 1 layer of tape Item [6] for insulation.
WD4 2nd Primary	Continue primary winding of 19 turns from left to right. At the last turn finish at pin 1.
Insulation	Place 1 layer of tape Item [6] for insulation.
WD5 2nd Primary	Start at FL1 from the left side of the bobbin, wind 4 bifilar turns of wire Item [5] in 1 layer. At the last turn, finish winding at FL2.
Insulation	Place 3 layers of tape Item [6] for insulation and secure the windings.
Core shield	Gap core halves to get 490 μ H inductance. Secure core and wind bifilar tin wire around the core. Terminate the wire at pin 1.
Finish Assembly	Cover core with 2 layers of tape. Varnish Item [7].

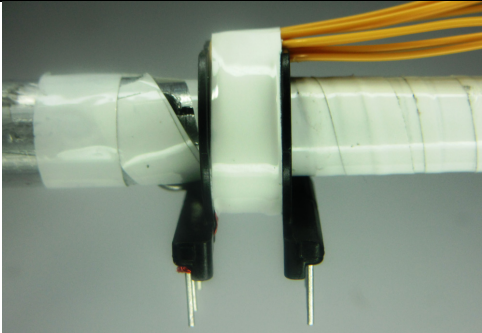
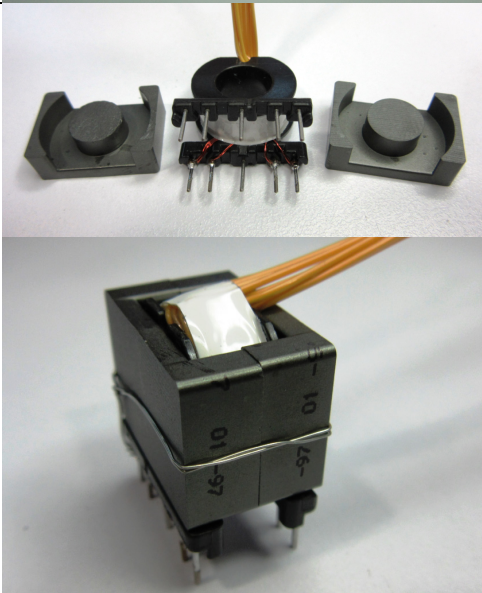
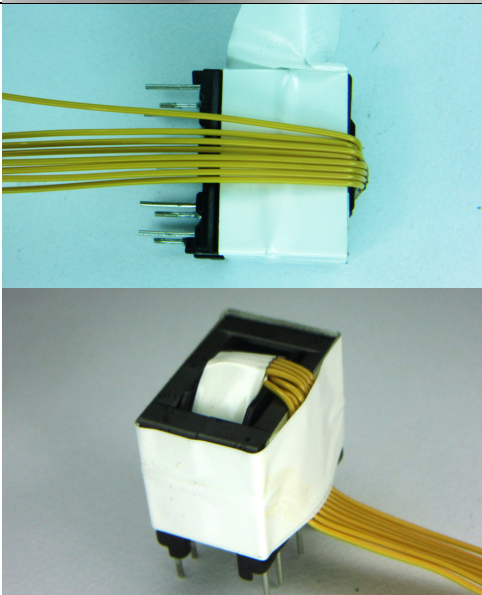


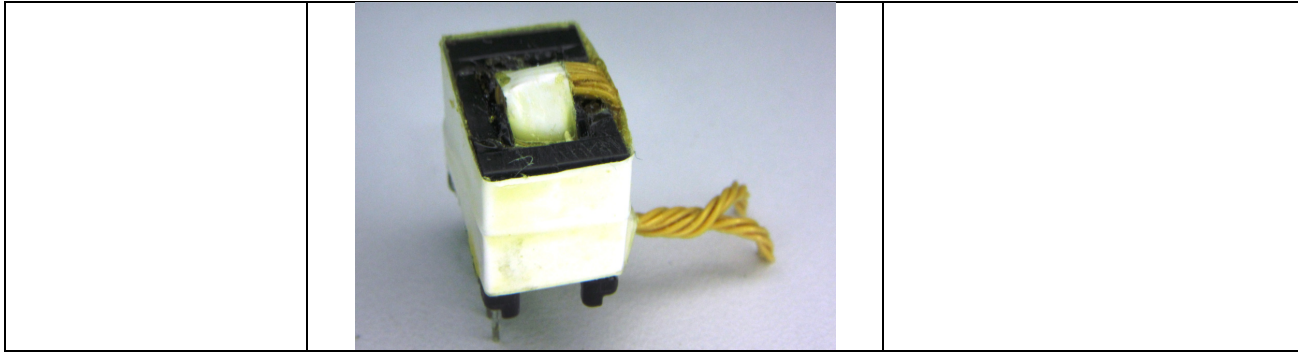
7.6 Winding Illustrations

<p>Winding preparation</p>		<p>Place the bobbin Item [2] on the mandrel with the pin side is on the left side Winding direction is clockwise direction.</p>
<p>WD1 1st Primary</p>		<p>Start at pin 2, wind 20 turns of wire Item [3] in 1 layer. At the last turn, bring wire back to the left side.</p>
<p>Insulation</p>		<p>Place 1 layer of tape Item [6] for insulation.</p>
<p>WD2 Bias/Shield</p>		<p>Start at pin 5, wind 6 (5- filars) turns of wire Item [4] in 1 layer. At the last turn, bring bifilar wire back to the left and finish at pin 4. Cut the remaining trifilar wire then no connect.</p>

<p>Insulation</p>		<p>Place 1 layer of tape Item [6] for insulation.</p>
<p>WD3 Secondary</p>		<p>Start at FL1 from the left side of the bobbin, wind 4 bifilar turns of wire Item [5] in 1 layer. At the last turn, finish winding at FL2.</p>
<p>Insulation</p>		<p>Place 1 layer of tape Item [6] for insulation.</p>
<p>WD4 2nd Primary</p>		<p>Continue primary winding of 19 turns from left to right. At the last turn finish at pin 1.</p>

		
<p>Insulation</p>		<p>Place 1 layer of tape Item [6] for insulation.</p>
<p>WD5 Secondary</p>		<p>Start at FL1 from the left side of the bobbin, wind 4 bifilar turns of wire Item [5] in 1 layer. At the last turn, finish winding at FL2.</p>
<p>Insulation</p>		<p>Place 3 layers of tape Item [6] for insulation and bring FL1 to right side then secure the windings.</p>

		
<p>Core shield</p>		<p>Gap core halves to get 490 μH inductance. Secure core and wind bifilar tin wire around the core. Terminate the wire at pin 1.</p>
<p>Finish Assembly</p>		<p>Cover core with 2 layers of tape. Varnish Item [7].</p>



8 Inductor Design Spreadsheet

ACDC_InnoSwitch3-CP_Flyback_062117; Rev.0.1; Copyright Power Integrations 2017	INPUT	OUTPUT	UNITS	InnoSwitch3 CP Flyback Design Spreadsheet
APPLICATION VARIABLES				
VIN_MIN	100	100	Volts RMS	Minimum AC input voltage
VIN_TYP	115	115	Volts RMS	Typical AC input voltage
VIN_MAX	132	132	Volts RMS	Maximum AC input voltage
VIN_RANGE		LOW LINE		Range of AC input voltage
FREQIN	60	60	Hertz	AC Input voltage frequency
CAP_INPUT	54.0	54.0	u-Farads	Input capacitor
Output 1				
VOU1	15.00	15.60	Volts DC	Output voltage 1: Enter the highest output voltage required at the end of cable
IOUT1	2.00	2.00	Amperes	Output current 1
POU1		31.20	Watts	Output power 1
EFFICIENCY1	0.90	0.90		Output 1 efficiency estimate
Z_FACTOR1	0.50	0.50		Output 1 Z-factor estimate
Output 2				
VOU2	9.00	9.59	Volts DC	Output voltage 2
IOUT2	3.30	3.30	Amperes	Output current 2
POU2		31.66	Watts	Output power 2
EFFICIENCY2	0.90	0.90		Output 2 efficiency estimate
Z_FACTOR2	0.50	0.50		Output 2 Z-factor estimate
Output 3				
VOU3	5.00	5.60	Volts DC	Output voltage 3
IOUT3	6.00	6.00	Amperes	Output current 3
POU3		33.60	Watts	Output power 3
EFFICIENCY3	0.90	0.90		Output 3 efficiency estimate
Z_FACTOR3	0.50	0.50		Output 3 Z-factor estimate
IMPEDANCE_CABLE		0.100	Ohms	Cable impedance
FEEDBACK_METHOD	RESISTOR DIVIDER	RESISTOR DIVIDER		Select the type of feedback method
PRIMARY CONTROLLER SELECTION				
ENCLOSURE	ADAPTER	ADAPTER		Power supply enclosure type
ILIMIT_MODE	STANDARD	STANDARD		Device current limit mode
VDRAIN_BREAKDOWN	650	650	Volts DC	Device breakdown voltage
DEVICE_GENERIC	INN3268	INN3268		Generic device code
DEVICE_CODE		INN3268C		Actual device code
POUT_MAX		45	Watts	Power capability of the device based on thermal performance
RDSON_100DEG		1.30	Ohms	Primary MOSFET on time drain resistance at 100 degC
ILIMIT_MIN		1.60	Amperes	Minimum current limit of the primary MOSFET
ILIMIT_TYP		1.65	Amperes	Typical current limit of the primary MOSFET
ILIMIT_MAX		1.72	Amperes	Maximum current limit of the primary MOSFET
VDRAIN_ON_MOSFET		0.45	Volts DC	Primary MOSFET on time drain voltage
VDRAIN_OFF_RING		476.7	Volts DC	Primary MOSFET peak drain voltage
WORST CASE PRIMARY PARAMETERS				
FREQUENCY_IOUT_MAX	78000	78000	Hertz	Switching frequency at full load and valley of the rectified minimum AC input voltage
VOR	150	150	Volts DC	Secondary voltage reflected to the primary when the primary MOSFET turns OFF
VMIN		107.1	Volts DC	Valley of the rectified minimum AC input voltage at full load
KP		0.546		Measure of continuous/discontinuous mode of operation
MODE_OPERATION		CCM		Mode of operation
DUTYCYCLE		0.432		Duty cycle at the valley of the rectified input voltage

TIME_ON		5.543	u-Seconds	Primary MOSFET on-time
IPEAK_PRIMARY		1.64	Amperes	Primary MOSFET peak current
IPEDESTAL_PRIMARY		0.70	Amperes	Primary MOSFET current pedestal
IAVG_PRIMARY		0.35	Amperes	Primary MOSFET average current
IRIPPLE_PRIMARY		1.59	Amperes	Primary MOSFET ripple current
IRMS_PRIMARY		0.65	Amperes	Primary MOSFET RMS current
LPRIMARY_MIN		465	u-Henrys	Minimum primary inductance
LPRIMARY_TYP		490	u-Henrys	Typical primary inductance
LPRIMARY_TOL	5	5	%	Primary inductance tolerance
LPRIMARY_MAX		514	u-Henrys	Maximum primary inductance
WORST CASE SECONDARY PARAMETERS				
IPEAK_SECONDARY		15.54	Amperes	Secondary winding peak current
IPEDESTAL_SECONDARY		6.65	Amperes	Secondary winding current pedestal
IRMS_SECONDARY		9.15	Amperes	Secondary winding RMS current
IRIPPLE_CAP_OUTPUT		9.10	Amperes	Output capacitor current ripple
TRANSFORMER CONSTRUCTION PARAMETERS				
Core selection				
CORE	Custom	Custom		Core selection
CORE CODE		0		Core code
AE	59.80	59.80	mm^2	Core cross sectional area
LE	25.10	25.10	mm	Core magnetic path length
AL	3150	3150	n-Henrys/(turns^2)	Ungapped core effective inductance
VE	1500.0	1500.0	mm^3	Core volume
BOBBIN	EQ20	EQ20		Enter the custom bobbin information
AW			mm^2	Enter the window area of the custom bobbin
BW	6.00	6.00	mm	Bobbin width
MARGIN		0.0	mm	Safety margin width (Half the primary to secondary creepage distance)
Primary winding				
NPRIMARY		39		Primary turns
BPEAK		3985	Gauss	Peak flux density
BMAX		3665	Gauss	Maximum flux density
BAC		1734	Gauss	AC flux density
ALG		322	n-Henrys/(turns^2)	Gapped core effective inductance
LG		0.209	mm	Core gap length
LAYERS_PRIMARY		3		Number of primary layers
AWG_PRIMARY		27	AWG	Primary winding wire AWG
OD_PRIMARY_INSULATED		0.418	mm	Primary winding wire outer diameter with insulation
OD_PRIMARY_BARE		0.361	mm	Primary winding wire outer diameter without insulation
CMA_PRIMARY		311	mil^2/Amperes	Primary winding wire CMA
Secondary winding				
NSECONDARY	4	4		Secondary turns
AWG_SECONDARY		17	AWG	Secondary winding wire AWG
OD_SECONDARY_INSULATED		1.454	mm	Secondary winding wire outer diameter with insulation
OD_SECONDARY_BARE		1.150	mm	Secondary winding wire outer diameter without insulation
CMA_SECONDARY		224	mil^2/Amperes	Secondary winding wire CMA
Bias winding				
NBIAS		10		Bias turns required to ensure minimum bias voltage
PRIMARY COMPONENTS SELECTION				
Line undervoltage				
BROWN-IN REQUIRED	40.0	40.0	Volts RMS	Required line brown-in threshold
RLS		2.26	MOhms	Resistor connected to the V-pin for the required UV/OV threshold
BROWN-IN ACTUAL		39.9	Volts RMS	Actual brown-in threshold
BROWN-OUT ACTUAL		33.9	Volts RMS	Actual brown-out threshold



Line overvoltage				
OVERVOLTAGE_LINE		181.3	Volts RMS	Actual line over-voltage threshold
Bias diode				
VBIAS_MIN	10.0	10.0	Volts DC	Minimum rectified bias winding voltage required
VF_BIAS		0.70	Volts DC	Bias winding diode forward drop
VBIAS_MAX		31.40	Volts DC	Maximum rectified bias winding voltage
VREVERSE_BIASDIODE		79.27	Volts DC	Bias diode reverse voltage (not accounting parasitic voltage ring)
CBIAS		22	u-Farads	Bias winding rectification capacitor
CBPP		0.47	u-Farads	BPP pin capacitor
SECONDARY COMPONENTS SELECTION				
Rectifier				
VREVERSE_RECTIFIER		39.63	Volts DC	Secondary rectifier reverse voltage (not accounting parasitic voltage ring)
SRFET	Auto	CSD18531Q5A		Secondary MOSFET selection
VF_SRFET		0.03	Volts DC	SRFET on time drain voltage
VDRAIN_OFF_SRFET		60	Volts DC	Maximum SRFET off time drain voltage
RDSON_SRFET		4.4	m-Ohms	SRFET on time drain resistance at 25degC for VGS=4.4V
Feedback Components				
RFB_UPPER	100	100.0	k-Ohms	Upper feedback resistor (connected to output voltage)
CFB_LOWER		330	p-Farads	Lower feedback resistor decoupling capacitor
DESIGN OUTPUT PARAMETERS				
OUTPUT_3		3		Select an output
VOUT		5.60	Volts DC	Output voltage
IOUT		6.00	Amperes	Output current
POUT		33.60	Watts	Output power
EFFICIENCY		0.90		Output efficiency
Z_FACTOR		0.50		Output Z-factor
Primary Parameters				
DUTYCYCLE		0.311		Duty cycle at the valley of the rectified input voltage
VOR		48.1	Volts DC	Secondary voltage reflected to the primary when the primary MOSFET turns OFF
KP		0.546		Measure of continuous/discontinuous mode of operation
FREQUENCY_IOUT_MAX		78000	Hertz	Maximum switching frequency at full load and valley of the rectified minimum AC input voltage
FREQUENCY_IOUT_MEAN		69691	Hertz	Mean switching frequency at full load and valley of the rectified minimum AC input voltage
TIME_ON		3.985	u-seconds	Primary MOSFET on-time
IPEAK_PRIMARY		1.636	Amperes	Primary MOSFET peak current
IPEDESTAL_PRIMARY		0.700	Amperes	Primary MOSFET current pedestal
I AVG_PRIMARY		0.349	Amperes	Primary MOSFET average current
IRIPPLE_PRIMARY		1.028	Amperes	Primary MOSFET ripple current
IRMS_PRIMARY		0.647	Amperes	Primary MOSFET RMS current
Sedondary Parameters				
IPEAK_SECONDARY		15.706	Amperes	Secondary winding peak current
IPEDESTAL_SECONDARY		6.723	Amperes	Secondary winding current pedestal
IRMS_SECONDARY		9.249	Amperes	Secondary winding RMS current
IRIPPLE_CAP_OUTPUT		7.039	Amperes	Output capacitor current ripple
Feedback Components				
RFB_LOWER		40.20	k-Ohms	Lower feedback resistor
OUTPUT_2		2		Select an output
VOUT		9.59	Volts DC	Output voltage
IOUT		3.30	Amperes	Output current
POUT		31.66	Watts	Output power

EFFICIENCY		0.90		Output efficiency
Z_FACTOR		0.50		Output Z-factor
Primary Parameters				
DUTYCYCLE		0.432		Duty cycle at the valley of the rectified input voltage
VOR		92.3	Volts DC	Secondary voltage reflected to the primary when the primary MOSFET turns OFF
KP		1.114		Measure of continuous/discontinuous mode of operation
FREQUENCY_IOUT_MAX		62949	Hertz	Maximum switching frequency at full load and valley of the rectified minimum AC input voltage
FREQUENCY_IOUT_MEAN		57613	Hertz	Mean switching frequency at full load and valley of the rectified minimum AC input voltage
TIME_ON		6.868	u-seconds	Primary MOSFET on-time
IPEAK_PRIMARY		1.594	Amperes	Primary MOSFET peak current
IPEDESTAL_PRIMARY		0.000	Amperes	Primary MOSFET current pedestal
IAVG_PRIMARY		0.322	Amperes	Primary MOSFET average current
IRIPPLE_PRIMARY		1.594	Amperes	Primary MOSFET ripple current
IRMS_PRIMARY		0.585	Amperes	Primary MOSFET RMS current
Sedondary Parameters				
IPEAK_SECONDARY		15.302	Amperes	Secondary winding peak current
IPEDESTAL_SECONDARY		0.000	Amperes	Secondary winding current pedestal
IRMS_SECONDARY		6.099	Amperes	Secondary winding RMS current
IRIPPLE_CAP_OUTPUT		5.130	Amperes	Output capacitor current ripple
Feedback Components				
RFB_LOWER		16.90	k-Ohms	Lower feedback resistor
OUTPUT_1		1		Select an output
VOUT		15.60	Volts DC	Output voltage
IOUT		2.00	Amperes	Output current
POUT		31.20	Watts	Output power
EFFICIENCY		0.90		Output efficiency
Z_FACTOR		0.50		Output Z-factor
Primary Parameters				
DUTYCYCLE		0.425		Duty cycle at the valley of the rectified input voltage
VOR		150.0	Volts DC	Secondary voltage reflected to the primary when the primary MOSFET turns OFF
KP		1.859		Measure of continuous/discontinuous mode of operation
FREQUENCY_IOUT_MAX		62257	Hertz	Maximum switching frequency at full load and valley of the rectified minimum AC input voltage
FREQUENCY_IOUT_MEAN		56995	Hertz	Mean switching frequency at full load and valley of the rectified minimum AC input voltage
TIME_ON		6.826	u-seconds	Primary MOSFET on-time
IPEAK_PRIMARY		1.591	Amperes	Primary MOSFET peak current
IPEDESTAL_PRIMARY		0.000	Amperes	Primary MOSFET current pedestal
IAVG_PRIMARY		0.316	Amperes	Primary MOSFET average current
IRIPPLE_PRIMARY		1.591	Amperes	Primary MOSFET ripple current
IRMS_PRIMARY		0.579	Amperes	Primary MOSFET RMS current
Sedondary Parameters				
IPEAK_SECONDARY		15.272	Amperes	Secondary winding peak current
IPEDESTAL_SECONDARY		0.000	Amperes	Secondary winding current pedestal
IRMS_SECONDARY		4.744	Amperes	Secondary winding RMS current
IRIPPLE_CAP_OUTPUT		4.302	Amperes	Output capacitor current ripple
Feedback Components				
RFB_LOWER		9.31	k-Ohms	Lower feedback resistor



9 Performance Data

9.1 Efficiency

Note: Output voltage measured at PCB end. This considers the 300 mV cable drop compensation.

9.1.1 Efficiency vs. Line

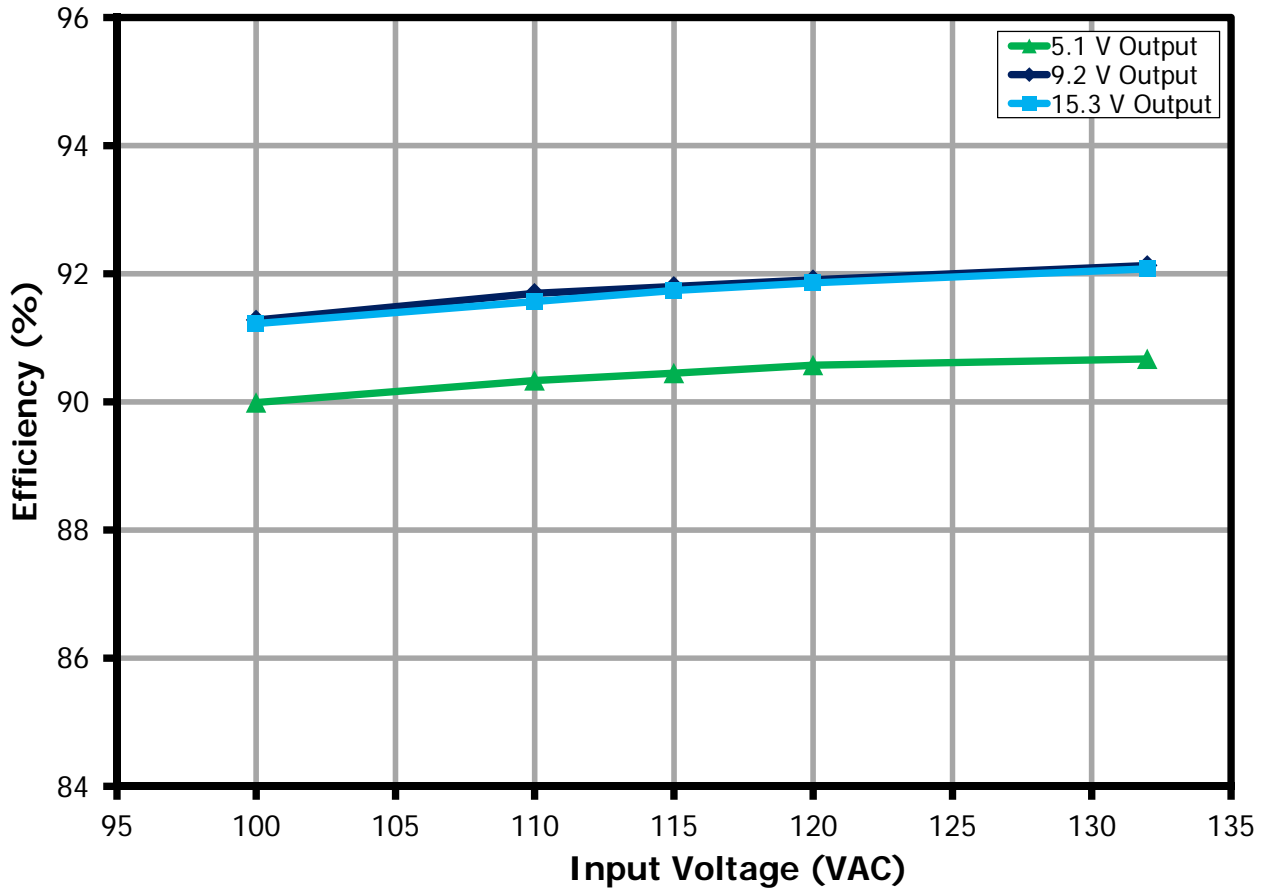


Figure 8 – Efficiency vs. Input Line Voltage.



9.1.2 Efficiency vs. Load

Note: Output voltage measured at PCB end. This considers the 300mV cable drop compensation.

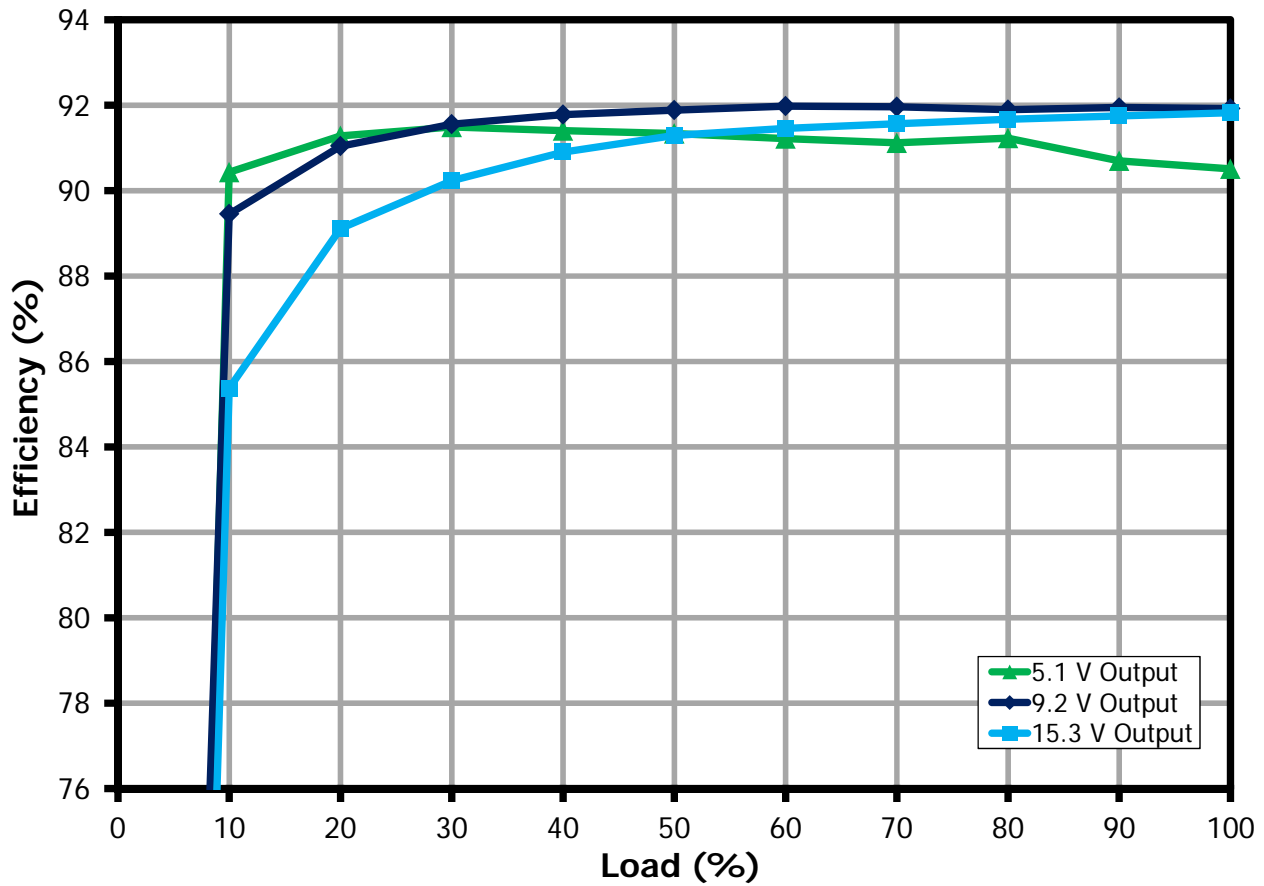


Figure 9 – Efficiency vs. Percent Load.

9.1.3 No-Load Input Power

Note: 5 V outputs at no-load.

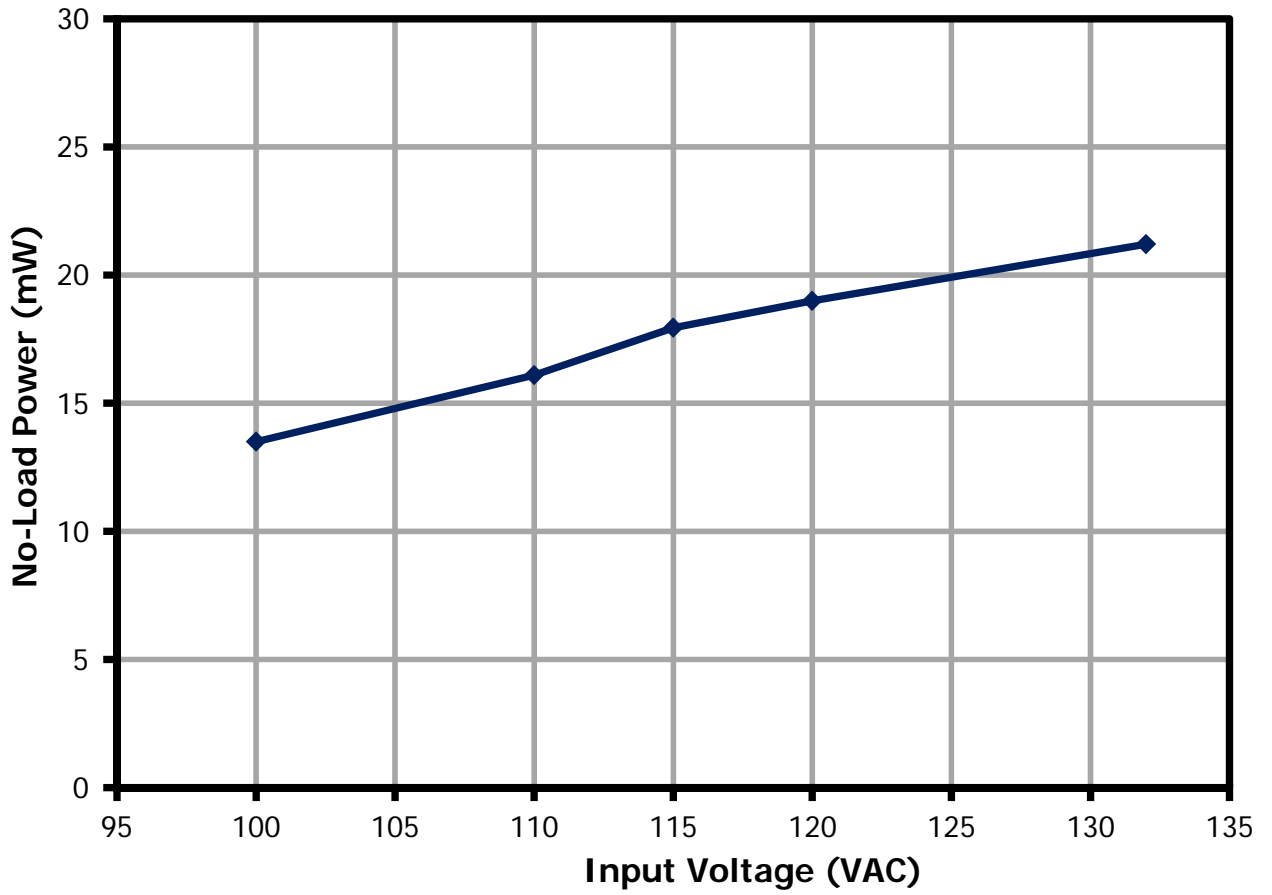


Figure 10 – No Load Power vs. Input Line Voltage.



9.2 Line and Load Regulation

9.2.1 5.1 V Line Regulation at 6 A Load

Note: Output voltage measured at PCB end. This considers the 300 mV cable drop compensation.

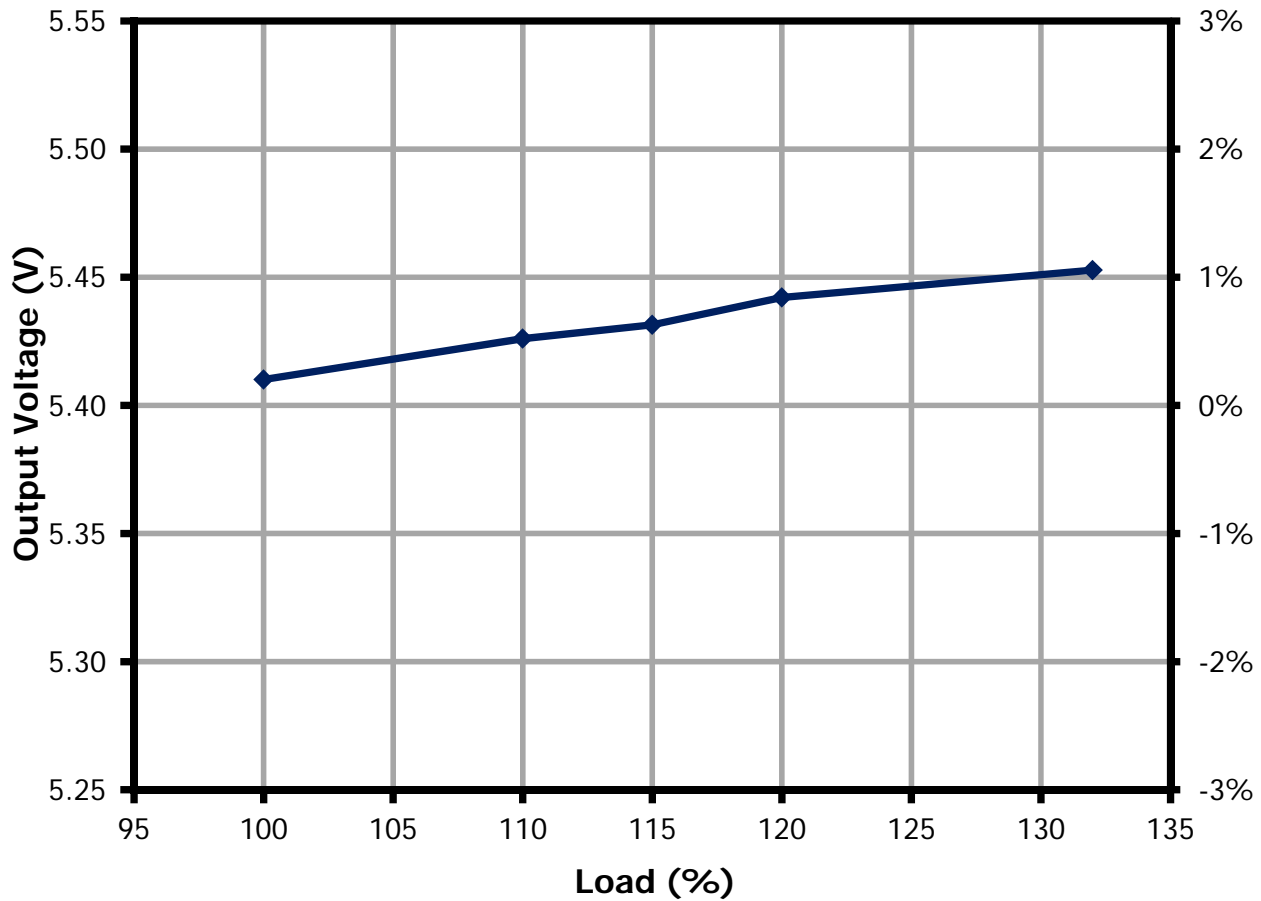


Figure 11 – 5.1 V Output Regulation vs. Input Line Voltage.

9.2.2 9.2 V Line Regulation at 3.3 A Load

Note: Output voltage measured at PCB end. This considers the 300 mV cable drop compensation.

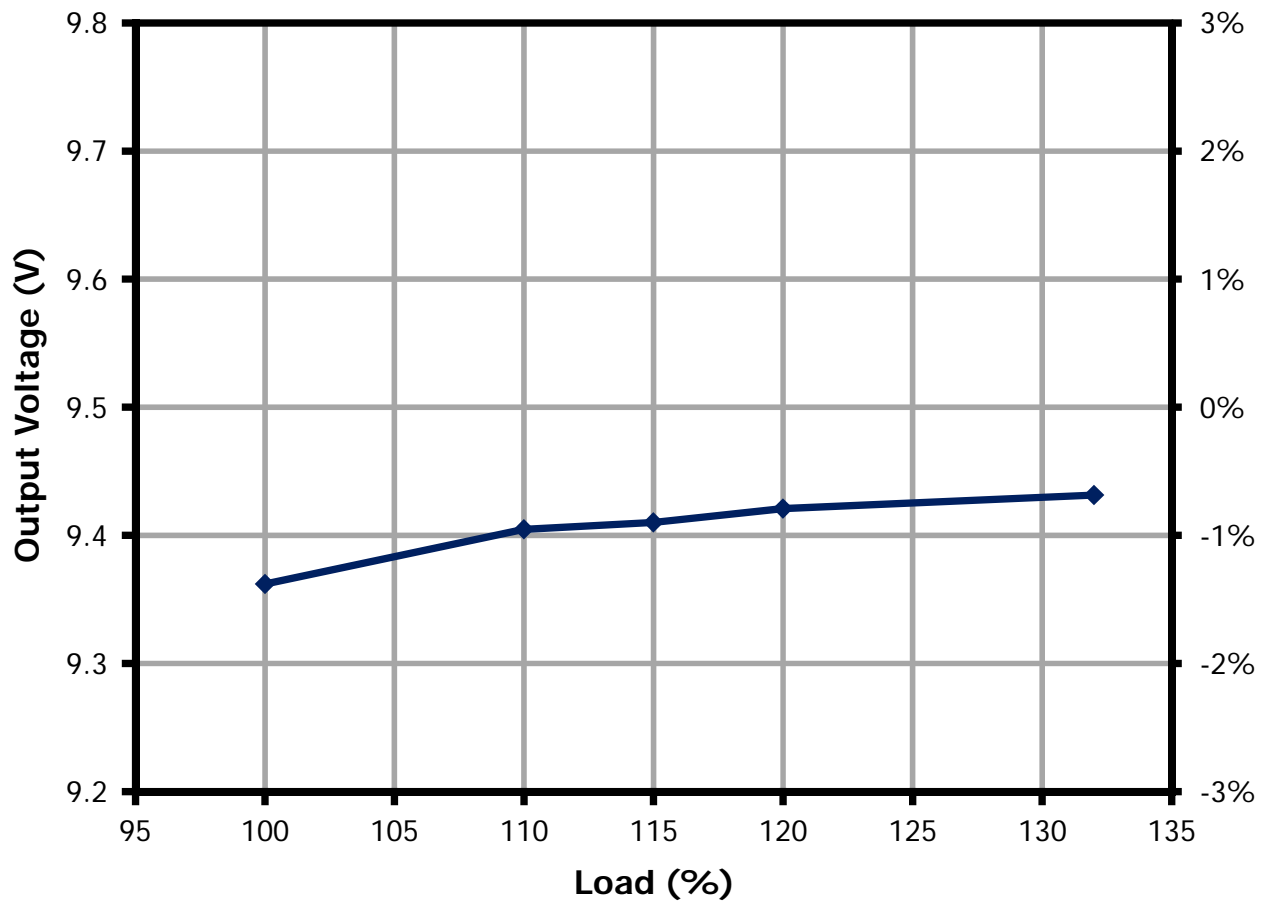


Figure 12 – 9.2 V Output Regulation vs. Input Line Voltage

9.2.3 15.3 V Line Regulation at 2 A Load

Note: Output voltage measured at PCB end. This considers the 300 mV cable drop compensation.

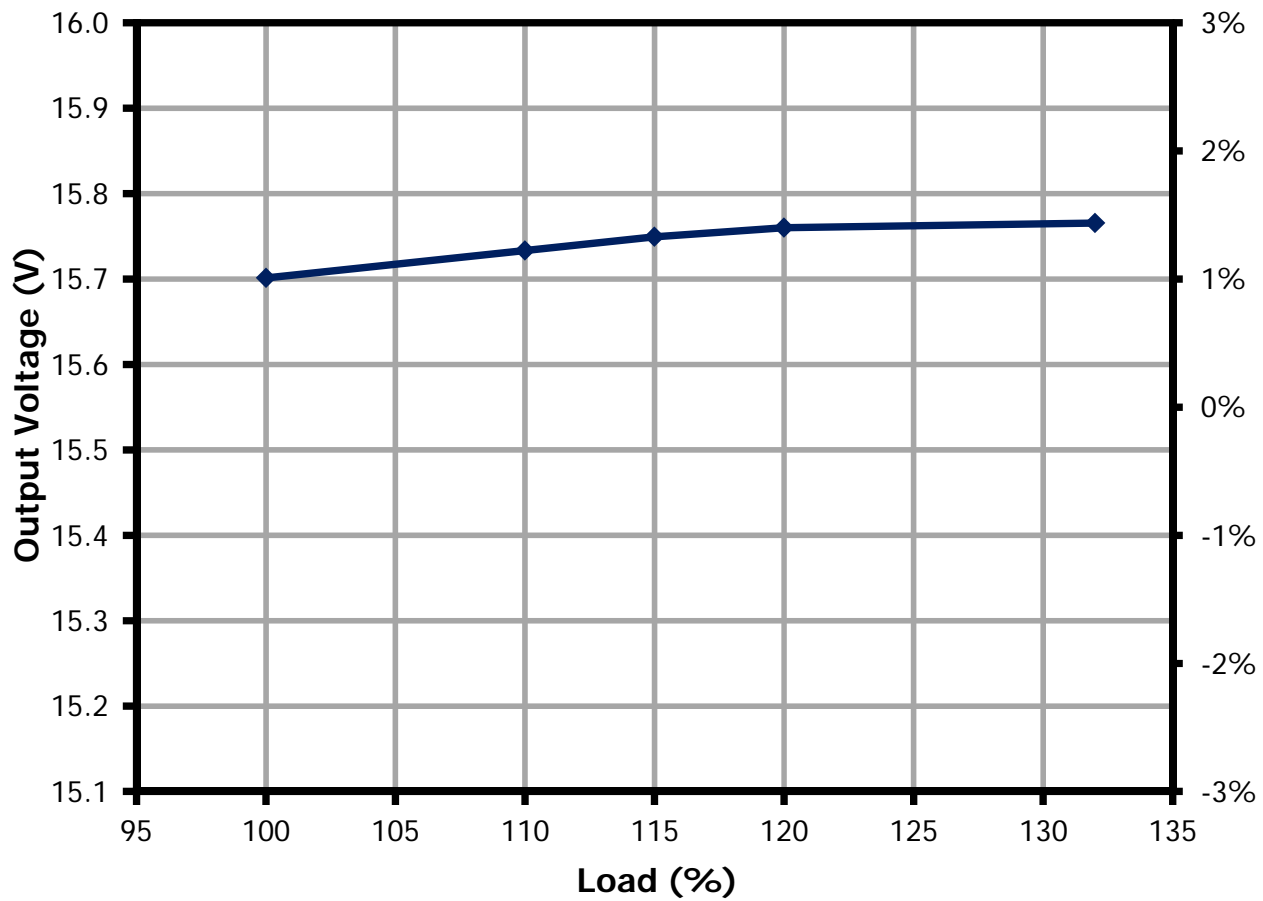


Figure 13 – 15.3 V Output Regulation vs. Input Line Voltage.

9.2.4 5.1 V Load Regulation

Note: Output voltage measured at PCB end. This considers the 300 mV cable drop compensation.

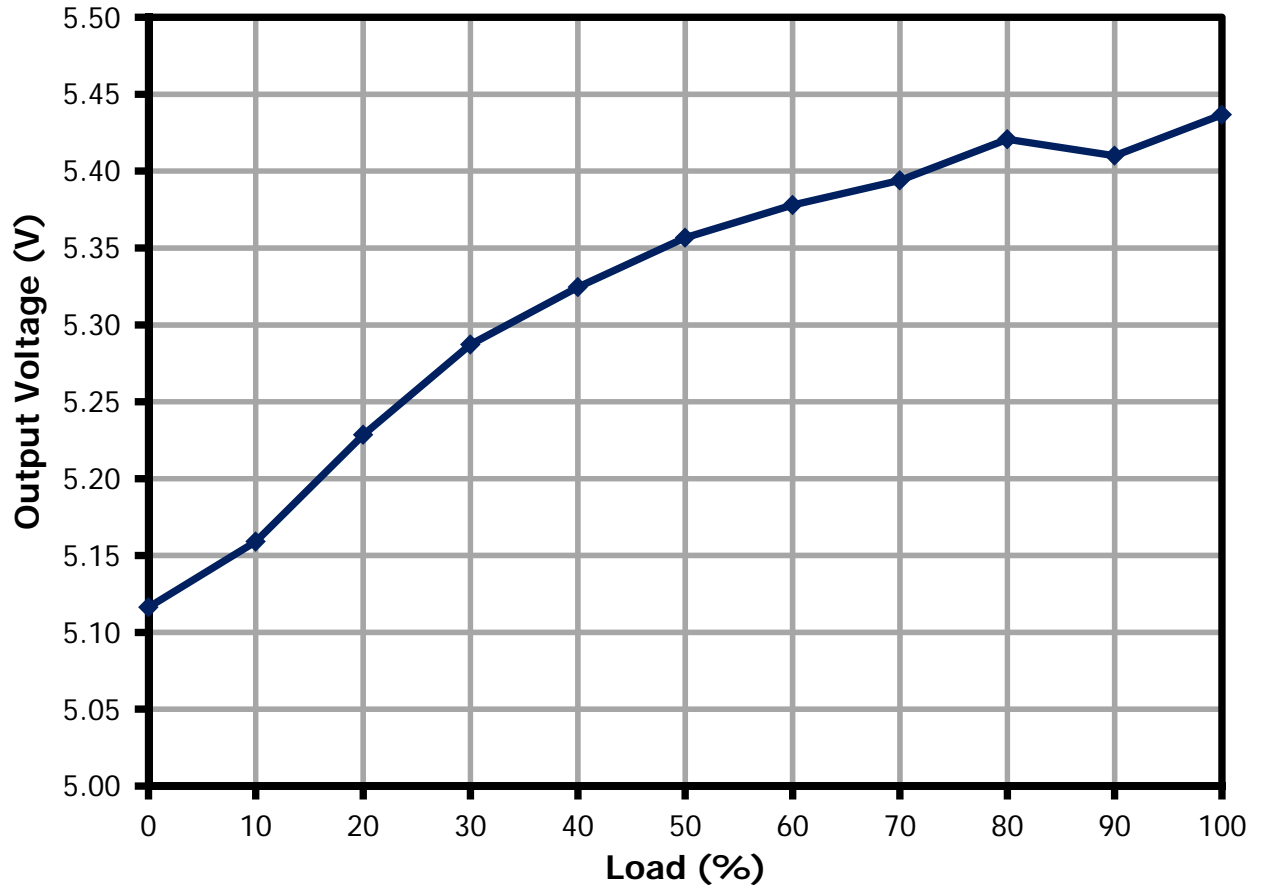


Figure 14 – 5.1 V Output Regulation vs. Percent Load.

9.2.5 9.2 V Load Regulation

Note: Output voltage measured at PCB end. This considers the 300 mV cable drop compensation.

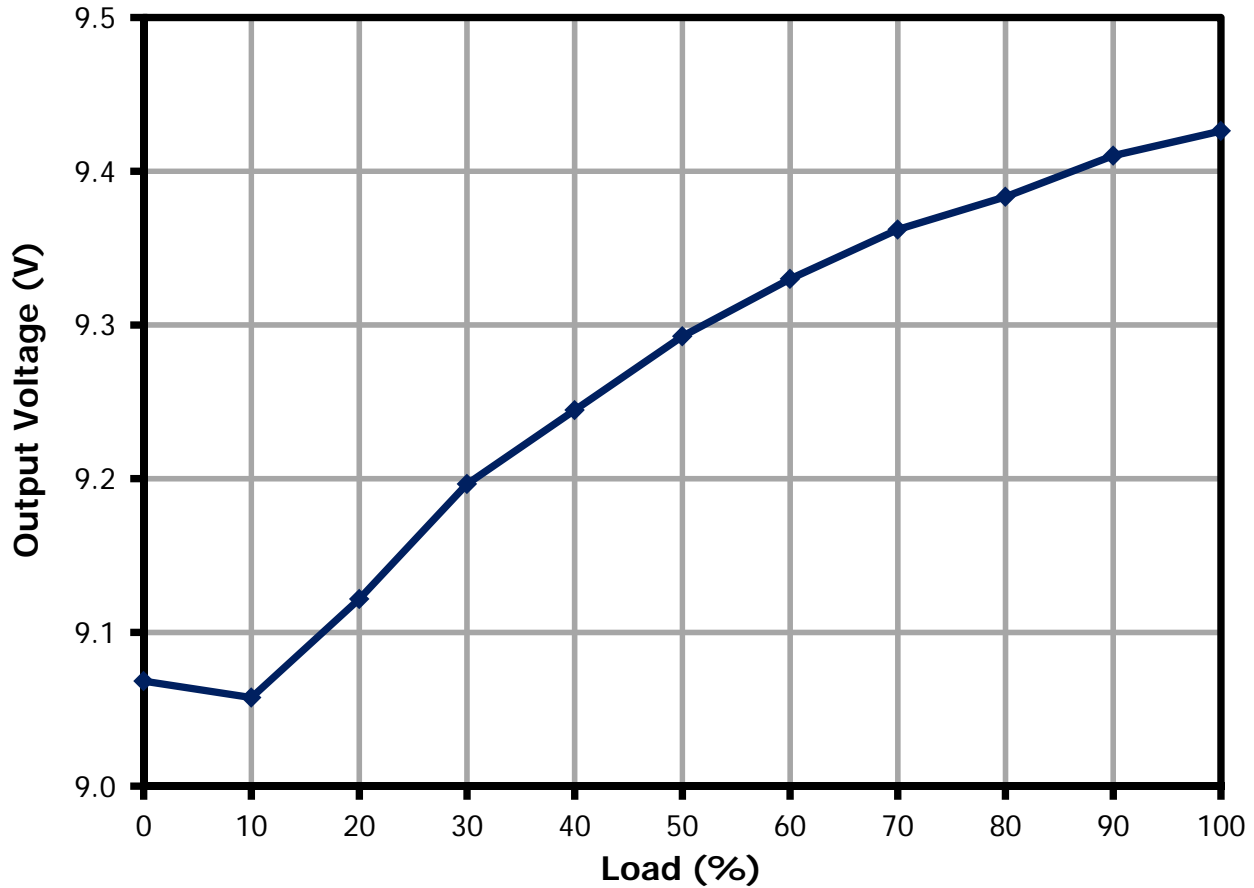


Figure 15 – 9.2 V Output Regulation vs. Percent Load.

9.2.6 15.3 V Load Regulation

Note: Output voltage measured at PCB end. This considers the 300 mV cable drop compensation.

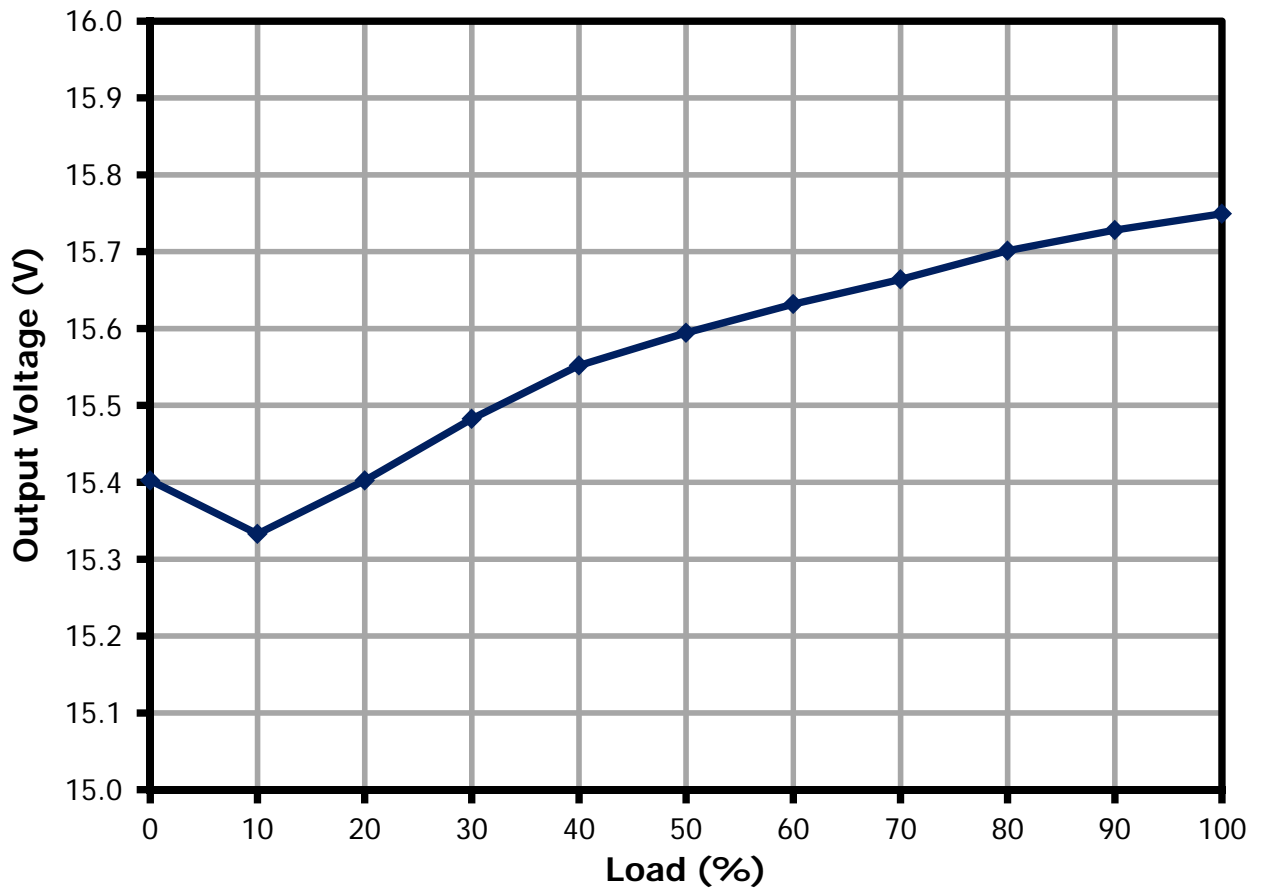


Figure 16 – 15.3 V Output Regulation vs. Percent Load.

9.2.7 CP Profile vs. Line (5.1 V / 6 A)

Note: Output voltage measured at PCB end. This considers the 300 mV cable drop compensation.

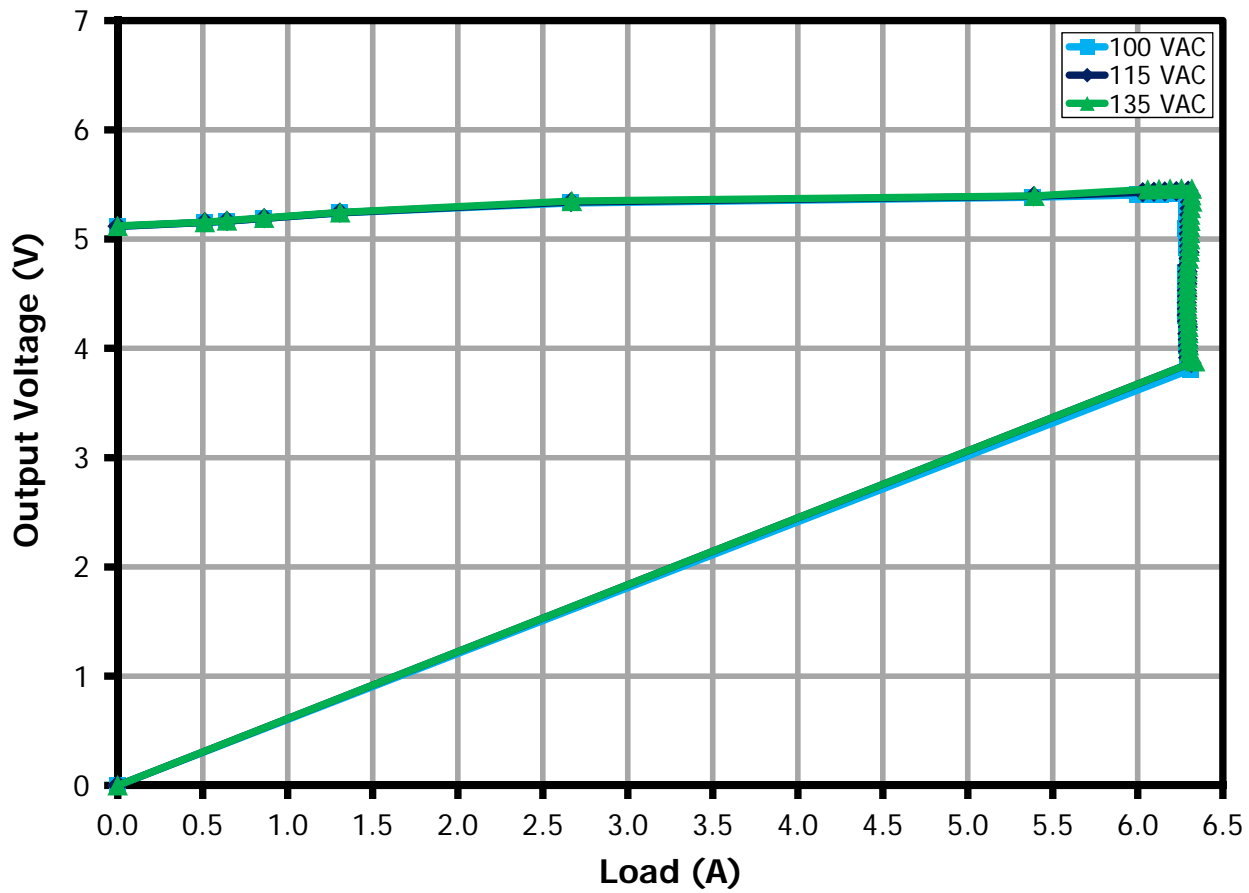


Figure 17 – CP Profile for 5.1 V Output at Different Input Line.

9.2.8 CP Profile vs. Line (9.2 V / 3.3 A)

Note: Output voltage measured at PCB end. This considers the 300 mV cable drop compensation.

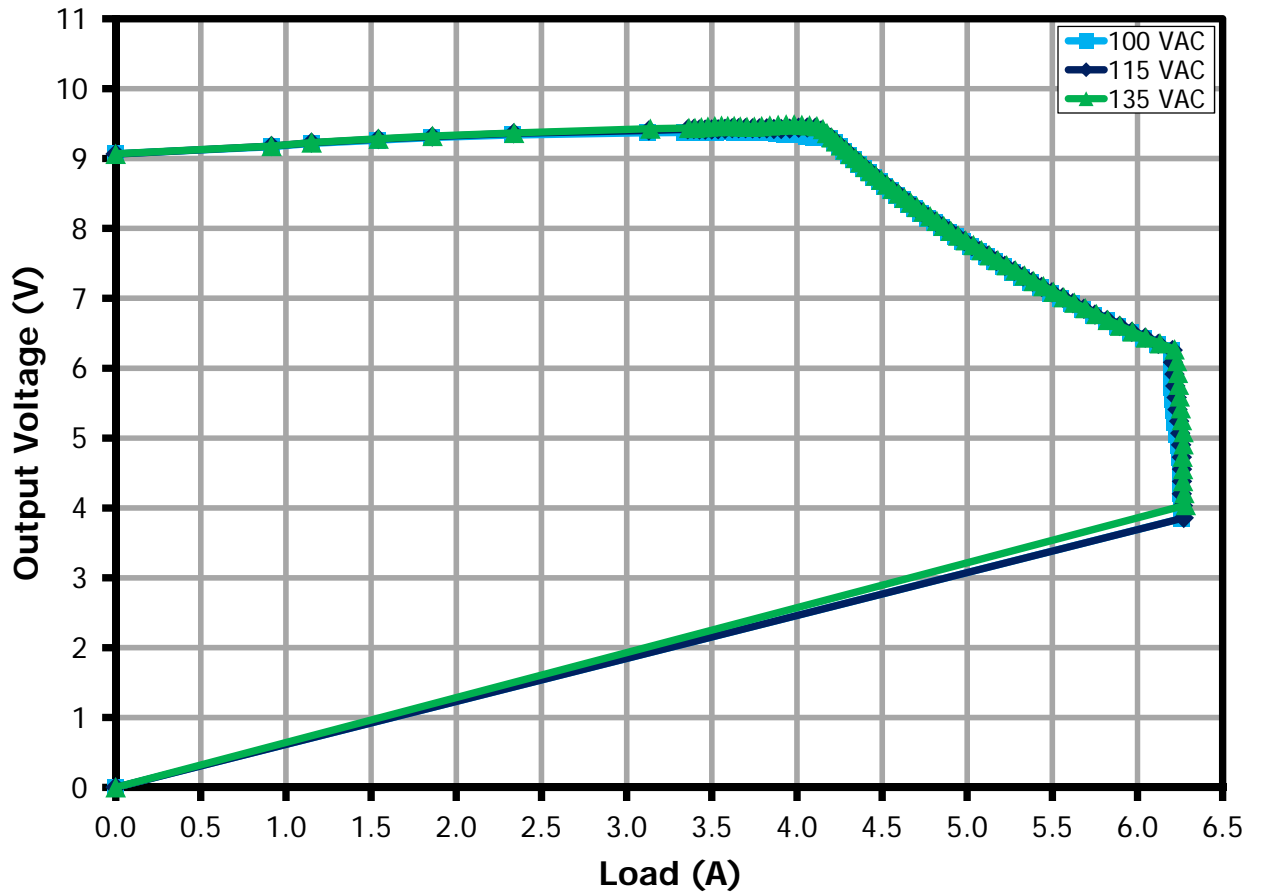


Figure 18 – CP Profile for 9.2 V Output at Different Input Line.



9.2.9 CP Profile vs. Line (15.3 V / 2 A)

Note: Output voltage measured at PCB end. This considers the 300 mV cable drop compensation.

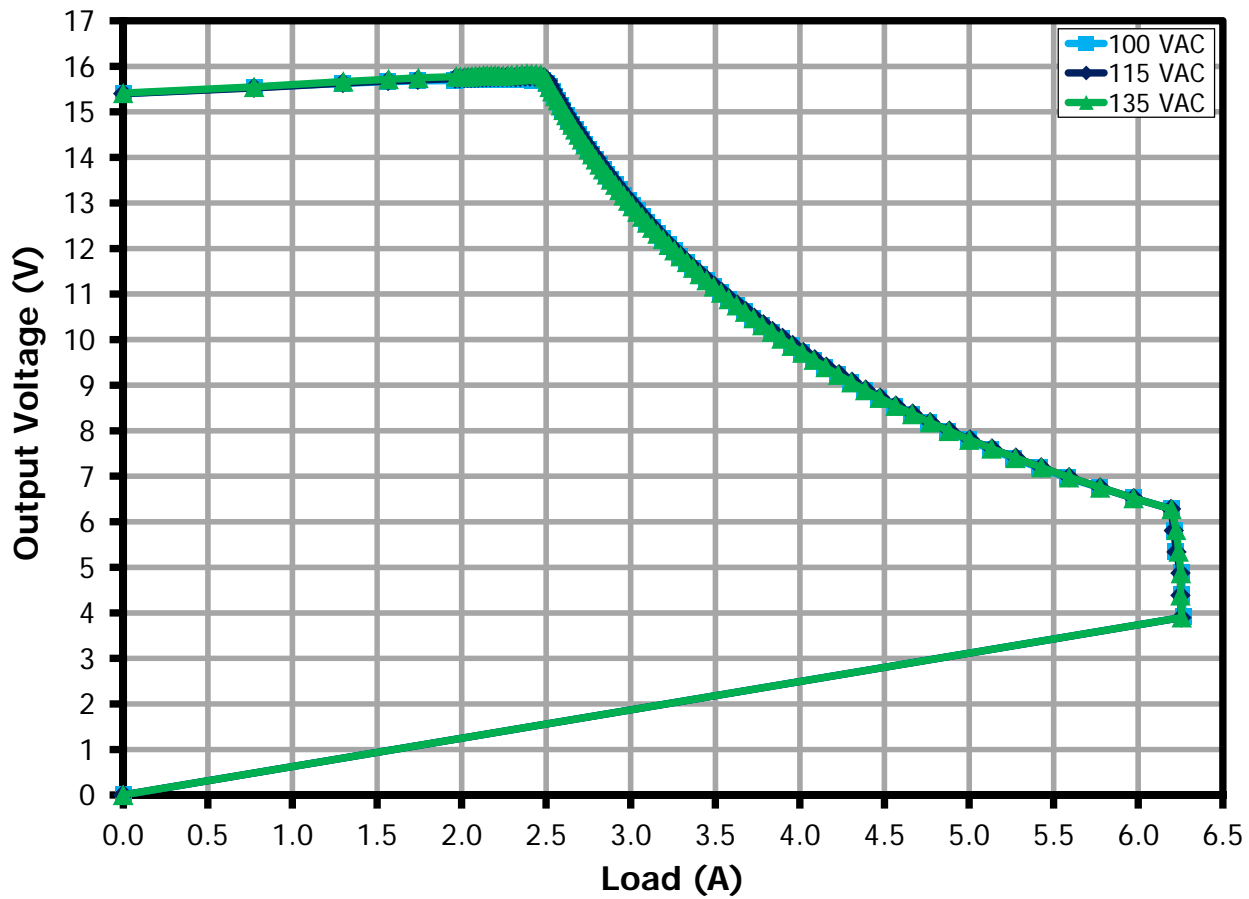


Figure 19 – CP Profile for 15 V Output at Different Input Line.

10 Test Data

10.1 Test Data Efficiency vs. Line, 5.1 V / 6 A (PCB End)

Input		Input Measurement			5.1 V / 6 A			Efficiency (%)
VAC (V _{RMS})	Freq (Hz)	V _{IN} (V _{RMS})	I _{IN} (A _{RMS})	P _{IN} (W)	V _{OUT} (V _{DC})	I _{OUT} (A _{DC})	P _{OUT} (W)	
100	47	99.85	0.64	36.07	5.41	6.00	32.46	89.99
110	47	109.88	0.60	36.04	5.43	6.00	32.56	90.33
115	50	114.94	0.59	36.03	5.43	6.00	32.59	90.45
120	60	119.92	0.59	36.05	5.44	6.00	32.65	90.57
132	60	131.89	0.56	36.08	5.45	6.00	32.71	90.67

10.2 Test Data Efficiency vs. Line, 9.2 V / 3.3 A (PCB End)

Input		Input Measurement			9.2 V / 3.3 A			Efficiency (%)
VAC (V _{RMS})	Freq (Hz)	V _{IN} (V _{RMS})	I _{IN} (A _{RMS})	P _{IN} (W)	V _{OUT} (V _{DC})	I _{OUT} (A _{DC})	P _{OUT} (W)	
100	47	99.86	0.60	33.84	9.36	3.30	30.89	91.28
110	47	109.89	0.56	33.84	9.40	3.30	31.03	91.70
115	50	114.95	0.56	33.82	9.41	3.30	31.05	91.80
120	60	119.93	0.56	33.82	9.42	3.30	31.08	91.91
132	60	131.91	0.53	33.78	9.43	3.300	31.12	92.13

10.3 Test Data Efficiency vs. Line, 15.3 V / 2 A (PCB End)

Input		Input Measurement			15 V / 2 A			Efficiency (%)
VAC (V _{RMS})	Freq (Hz)	V _{IN} (V _{RMS})	I _{IN} (A _{RMS})	P _{IN} (W)	V _{OUT} (V _{DC})	I _{OUT} (A _{DC})	P _{OUT} (W)	
100	47	99.86	0.61	34.42	15.70	2.00	31.40	91.22
110	47	109.88	0.57	34.36	15.73	2.00	31.46	91.57
115	50	114.94	0.56	34.33	15.75	2.00	31.49	91.74
120	60	119.92	0.57	34.31	15.76	2.00	31.52	91.86
132	60	131.90	0.54	34.24	15.77	2.00	31.53	92.08

Note: Outputs measurement at PCB end.

10.4 Test Data Efficiency vs Percent Load, 5.1 V / 6 A @ 115 VAC (PCB End)

Load Settings	Input Measurement			5.1 V / 6 A Measurement Variable			
% Load	V _{IN} (V _{RMS})	I _{IN} (A _{RMS})	P _{IN} (W)	V _{OUT} (V _{DC})	I _{OUT} (A _{DC})	P _{OUT} (W)	Efficiency (%)
100	114.96	0.61	36.04	5.44	6.00	32.62	90.51
90	114.96	0.55	32.21	5.41	5.40	29.21	90.70
80	114.97	0.50	28.52	5.42	4.80	26.02	91.23
70	114.97	0.45	24.86	5.39	4.20	22.65	91.12
60	114.98	0.40	21.22	5.38	3.60	19.36	91.22
50	114.99	0.35	17.59	5.36	3.00	16.07	91.34
40	114.99	0.29	13.98	5.32	2.40	12.78	91.41
30	115.00	0.23	10.40	5.29	1.80	9.52	91.49
20	115.00	0.17	6.87	5.23	1.20	6.27	91.28
10	115.01	0.10	3.42	5.16	0.60	3.09	90.43

10.5 Test Data Efficiency vs Percent Load, 9 V / 3.3 A @ 115 VAC (PCB End)

Load Settings	Input Measurement			9.2 V / 3.3 A Measurement Variable			
% Load	V _{IN} (V _{RMS})	I _{IN} (A _{RMS})	P _{IN} (W)	V _{OUT} (V _{DC})	I _{OUT} (A _{DC})	P _{OUT} (W)	Efficiency (%)
100	114.96	0.58	33.83	9.43	3.30	31.10	91.92
90	114.97	0.53	30.39	9.41	2.97	27.94	91.95
80	114.97	0.48	26.95	9.38	2.64	24.77	91.89
70	114.98	0.43	23.51	9.36	2.31	21.62	91.96
60	114.99	0.38	20.08	9.33	1.98	18.47	91.98
50	114.99	0.33	16.68	9.29	1.65	15.33	91.88
40	115.00	0.28	13.29	9.24	1.32	12.20	91.78
30	115.00	0.22	9.94	9.20	0.99	9.10	91.56
20	115.01	0.16	6.61	9.12	0.66	6.02	91.04
10	115.01	0.10	3.34	9.06	0.33	2.99	89.45

10.6 Test Data Efficiency vs Percent Load, 15.3 V / 2 A @ 115 VAC (PCB End)

Load Settings	Input Measurement			9.2 V / 3.3 A Measurement Variable			
% Load	V _{IN} (V _{RMS})	I _{IN} (A _{RMS})	P _{IN} (W)	V _{OUT} (V _{DC})	I _{OUT} (A _{DC})	P _{OUT} (W)	Efficiency (%)
100	114.96	0.58	34.30	15.75	2.00	31.49	91.82
90	114.96	0.54	30.85	15.73	1.80	28.30	91.75
80	114.97	0.49	27.39	15.70	1.60	25.11	91.67
70	114.98	0.44	23.94	15.66	1.40	21.92	91.57
60	114.98	0.39	20.50	15.63	1.20	18.75	91.46
50	114.99	0.34	17.07	15.59	1.00	15.58	91.29
40	114.99	0.28	13.68	15.55	0.80	12.44	90.90
30	115.00	0.23	10.28	15.48	0.60	9.28	90.23
20	115.01	0.17	6.91	15.40	0.40	6.16	89.11
10	115.01	0.10	3.58	15.33	0.20	3.06	85.37

Note: Outputs measurement at PCB end.

10.7 Test Data Line Regulation, 5.1 V / 6 A

Input		5.1 V / 6 A		
VAC (V _{RMS})	Freq (Hz)	V _{OUT} (V _{DC})	I _{OUT} (A _{DC})	P _{OUT} (W)
100	47	5.41	6.00	32.46
110	47	5.43	6.00	32.56
115	50	5.43	6.00	32.59
120	60	5.44	6.00	32.65
132	60	5.45	6.00	32.71

10.8 Test Data Line Regulation, 9.2 V / 3.3 A

Input		9.2 V / 3.3 A		
VAC (V _{RMS})	Freq (Hz)	V _{OUT} (V _{DC})	I _{OUT} (A _{DC})	P _{OUT} (W)
100	47	9.36	3.30	30.89
110	47	9.40	3.30	31.03
115	50	9.41	3.30	31.04
120	60	9.42	3.30	31.08
132	60	9.43	3.30	31.12

10.9 Test Data Line Regulation, 15.3 V / 2 A

Input		15.3 V / 2 A		
VAC (V _{RMS})	Freq (Hz)	V _{OUT} (V _{DC})	I _{OUT} (A _{DC})	P _{OUT} (W)
100	47	15.70	2.00	31.40
110	47	15.73	2.00	31.46
115	50	15.75	2.00	31.50
120	60	15.76	2.00	31.52
132	60	15.77	2.00	31.53

Note: Output voltage measurement at PCB end.

10.10 Test Data Load Regulation, 5.1 V @ 115 VAC

Load Settings	5.1 V / 6 A Measurement Variable		
% Load	V _{OUT} (V _{DC})	I _{OUT} (A _{DC})	P _{OUT} (W)
100	5.43	6.00	32.62
90	5.41	5.40	29.21
80	5.42	4.80	26.01
70	5.39	4.20	22.65
60	5.37	3.59	19.35
50	5.35	2.99	16.06
40	5.32	2.40	12.77
30	5.28	1.80	9.51
20	5.22	1.19	6.27
10	5.15	0.60	3.09
0	5.11	0.00	0.00

10.11 Test Data Load Regulation, 9.2 V / 3.3 A @ 115 VAC

Load Settings	5.1 V / 6 A Measurement Variable		
% Load	V _{OUT} (V _{DC})	I _{OUT} (A _{DC})	P _{OUT} (W)
100	9.43	3.30	31.10
90	9.41	2.97	27.94
80	9.38	2.64	24.77
70	9.36	2.31	21.62
60	9.33	1.98	18.47
50	9.29	1.65	15.33
40	9.24	1.32	12.20
30	9.20	0.99	9.10
20	9.12	0.66	6.02
10	9.06	0.33	2.99
0	9.07	0.00	0.00

Note: Output voltage measurement at PCB end.

10.12 Test Data Load Regulation, 15.3 V / 2 A @ 115 VAC

Load Settings	5.1 V / 6 A Measurement Variable		
% Load	V _{OUT} (V _{DC})	I _{OUT} (A _{DC})	P _{OUT} (W)
100	15.75	2.00	31.49
90	15.73	1.80	28.30
80	15.70	1.60	25.11
70	15.66	1.40	21.92
60	15.63	1.20	18.75
50	15.59	1.00	15.58
40	15.55	0.80	12.44
30	15.48	0.60	9.28
20	15.40	0.40	6.16
10	15.33	0.20	3.06
0	15.40	0.00	0.00

Note: Output voltage measurement at PCB end.

10.13 Test Data No-Load Consumption, 5.1 V / 0 A

Input		Input Measurement		
VAC (V _{RMS})	Freq (Hz)	V _{IN} (V _{RMS})	I _{IN} (mA _{RMS})	P _{IN} (mW)
100	60	99.95	19.32	13.49
110	60	109.97	19.30	16.09
115	60	115.02	19.13	17.95
120	60	119.99	19.04	18.99
132	60	131.95	20.17	21.20

11 Thermal Performance

11.1 Open Case at 5.1 V / 6 A (30 °C)

11.1.1 100 VAC @ 30 °C Ambient

Ambient (°C)	Inn3268C (U1)	SR FET (Q3)	Transformer (T2)	Bridge Diode (BR1)
27	83.0	80.6	76.7	71.5

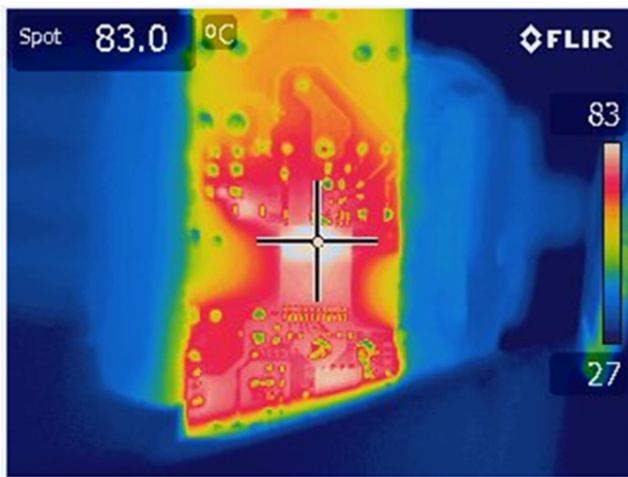


Figure 20 – Ambient = 27 °C.
INN3168C, U1 = 83 °C.

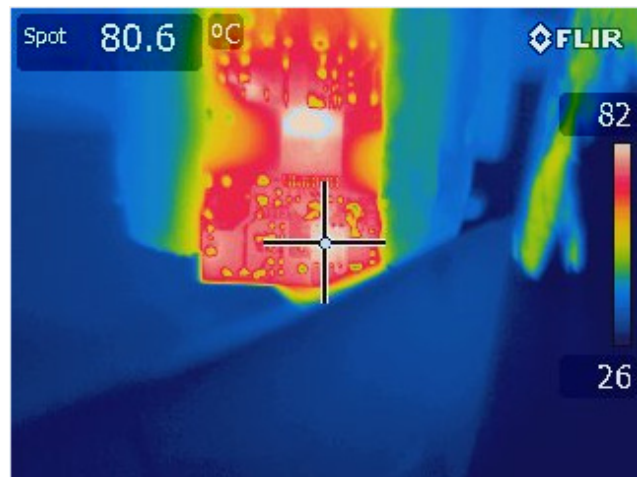


Figure 21 – Ambient = 26 °C.
SR FET, Q3 = 80.6 °C.

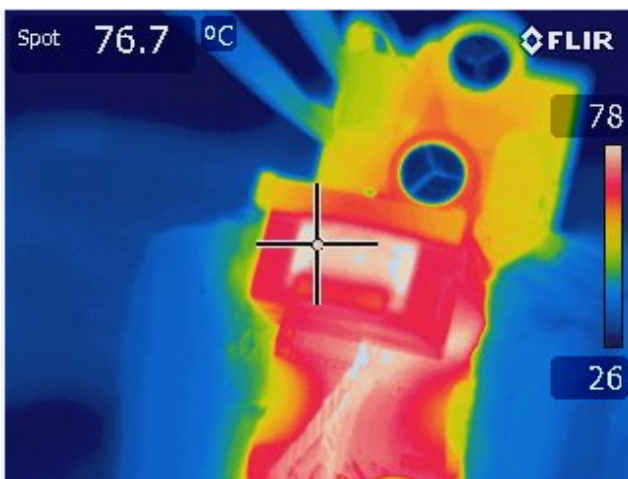


Figure 22 – Ambient = 26 °C.
Transformer, T2 = 76.7 °C.

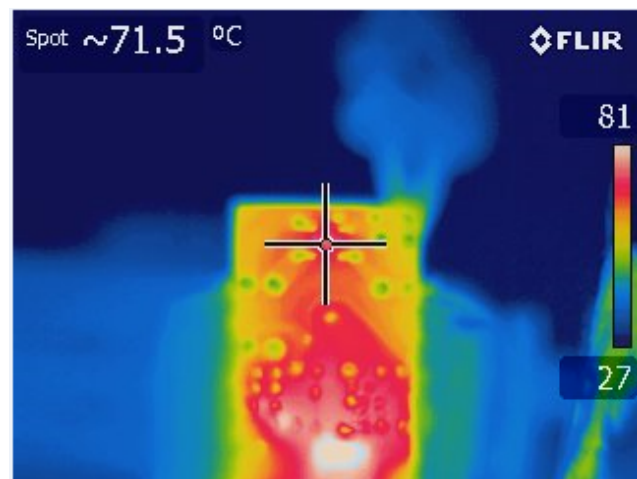


Figure 23 – Ambient = 27 °C.
Bridge Diode, BR1 = 71.5 °C.

11.1.2 132 VAC @ 30 °C Ambient

Ambient (°C)	Inn3268C (U1)	SR FET (Q3)	Transformer (T2)	Bridge Diode (BR1)
27	81.7	80.6	76.7	64.3

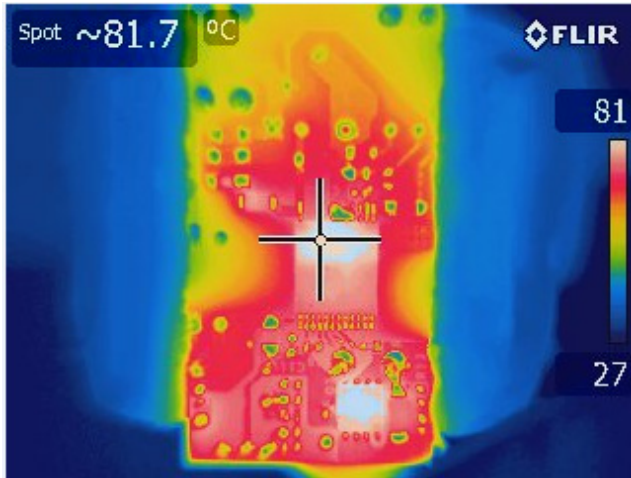


Figure 24 – Ambient = 27 °C.
INN3168C, U1 = 81.7 °C.

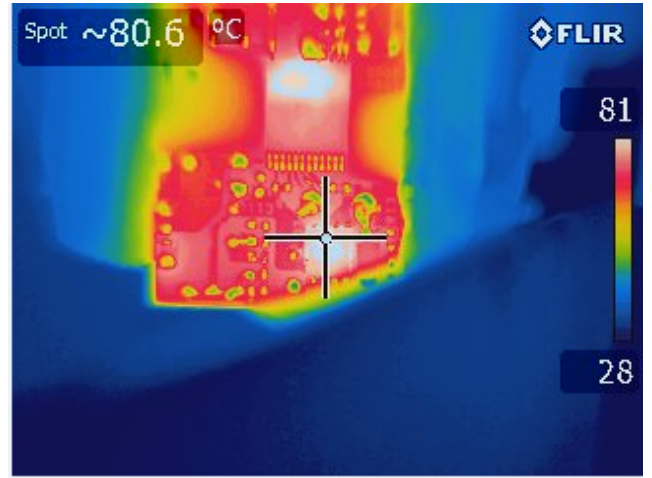


Figure 25 – Ambient = 28 °C.
SR FET, Q3 = 80.6 °C.

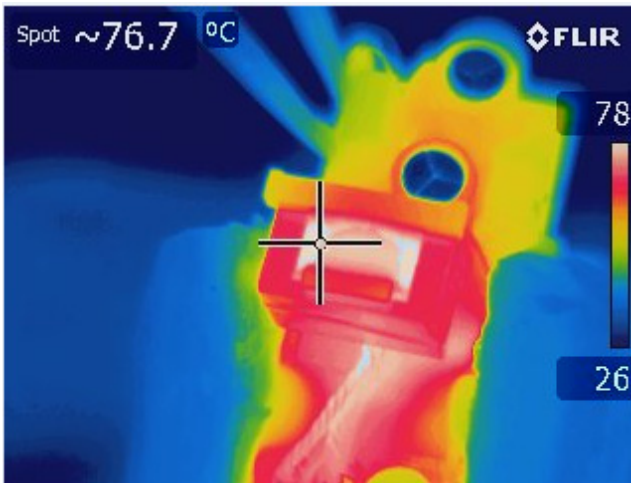


Figure 26 – Ambient = 26 °C.
Transformer, T2 = 76.7 °C.

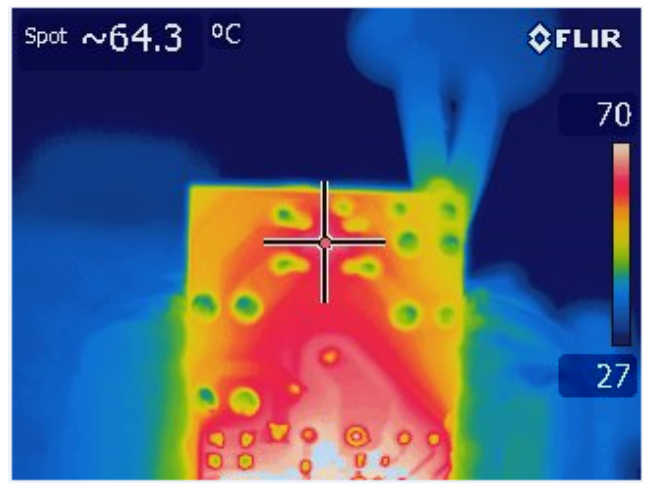


Figure 27 – Ambient = 27 °C.
Bridge Diode, BR1 = 64.3 °C.

11.2 Open Case at 9.2 V / 3.3 A (30 °C)

11.2.1 100 VAC @ 30 °C Ambient

Ambient (°C)	Inn3268C (U1)	SR FET (Q3)	Transformer (T2)	Bridge Diode (BR1)
27	70.7	63.4	71	67.3

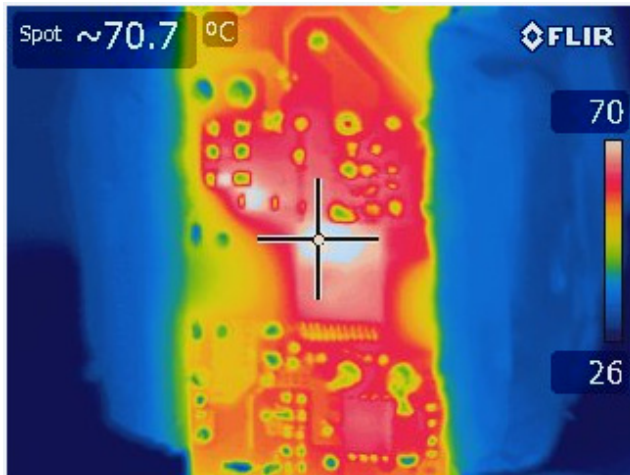


Figure 28 – Ambient = 27 °C.
INN3168C, U1 = 70.7 °C.



Figure 29 – Ambient = 28 °C.
SR FET, Q3 = 63.4 °C.

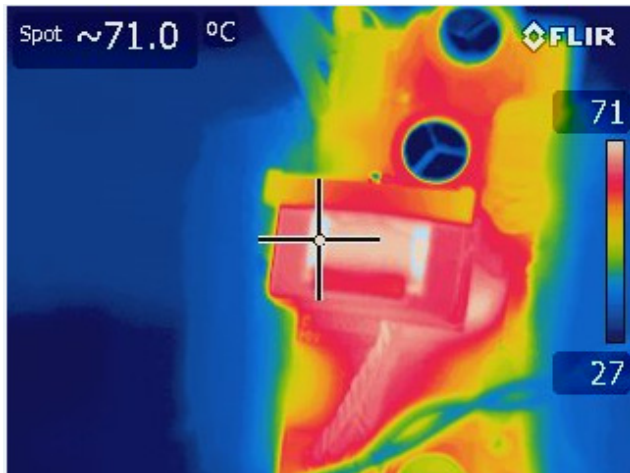


Figure 30 – Ambient = 26 °C.
Transformer, T2 = 71 °C.

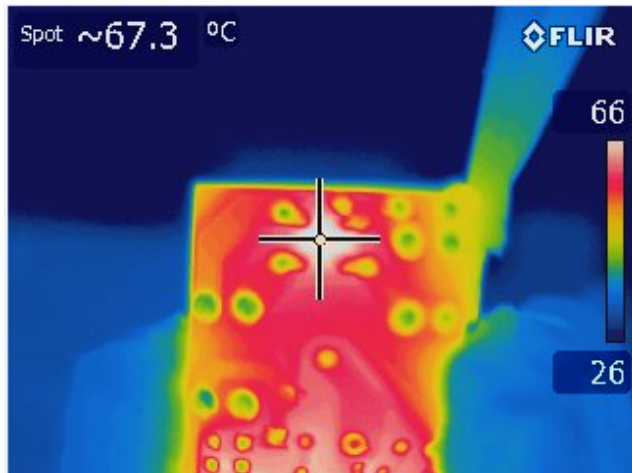


Figure 31 – Ambient = 27 °C.
Bridge Diode, BR1 = 67.3 °C.

11.2.2 132 VAC @ 30 °C Ambient

Ambient (°C)	Inn3268C (U1)	SR FET (Q3)	Transformer (T2)	Bridge Diode (BR1)
28	69.4	64.4	69.5	61.1

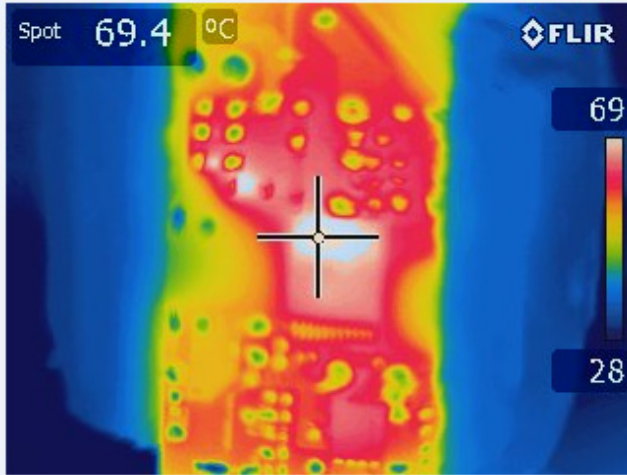


Figure 32 – Ambient = 27 °C.
INN3168C, U1 = 69.4 °C.

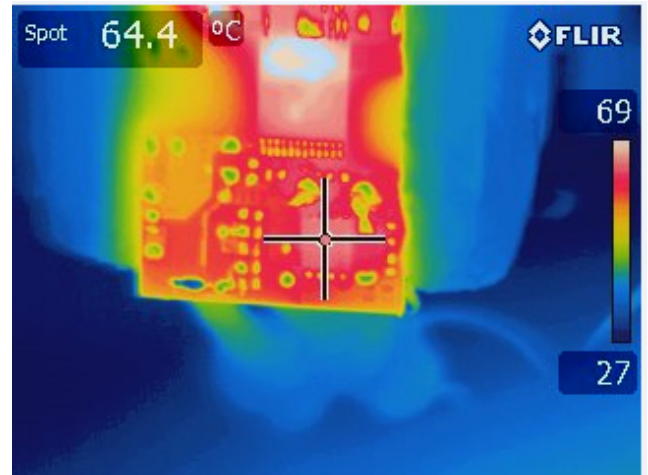


Figure 33 – Ambient = 28 °C.
SR FET, Q3 = 64.4 °C.

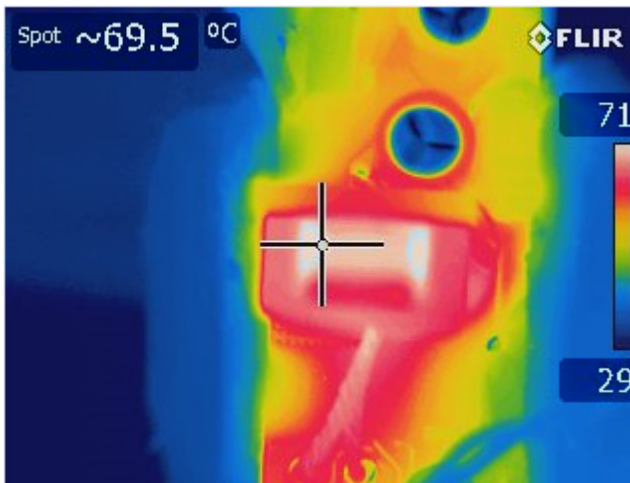


Figure 34 – Ambient = 26 °C.
Transformer, T2 = 69.5 °C.

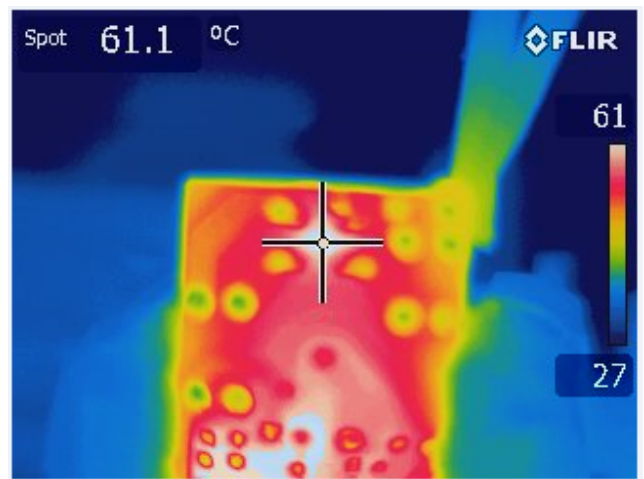


Figure 35 – Ambient = 27 °C.
Bridge Diode, BR1 = 61.1 °C.

11.3 Open Case at 15.3 V / 2 A (30 °C)

11.3.1 100 VAC @ 30 °C Ambient

Ambient (°C)	Inn3268C (U1)	SR FET (Q3)	Transformer (T2)	Bridge Diode (BR1)
27	74.5	63.2	70.8	68.5



Figure 36 – Ambient = 27 °C.
INN3168C, U1 = 74.5 °C.

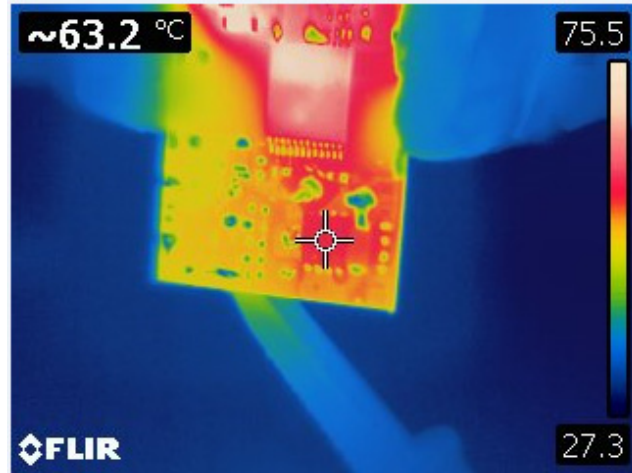


Figure 37 – Ambient = 28 °C.
SR FET, Q3 = 63.2 °C.

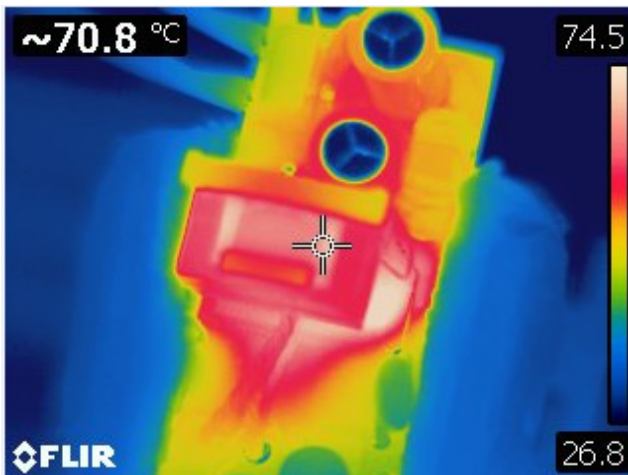


Figure 38 – Ambient = 26 °C.
Transformer, T2 = 70.8 °C.

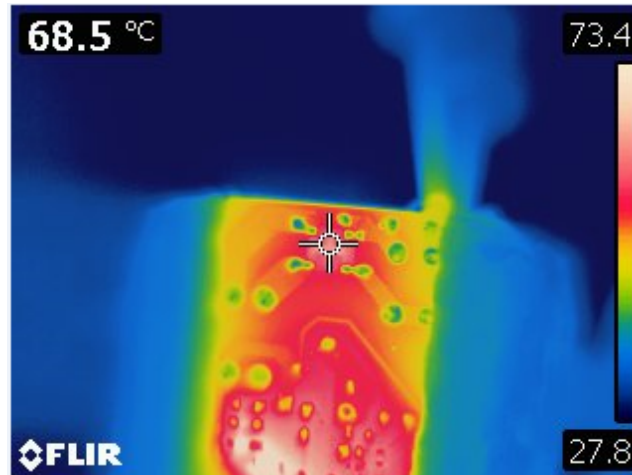


Figure 39 – Ambient = 27 °C.
Bridge Diode, BR1 = 68.5 °C.

11.3.2 132 VAC @ 30 °C Ambient

Ambient (°C)	INN3268C (U1)	SR MOSFET (Q3)	Transformer (T2)	Bridge Diode (BR1)
27	73.4	63.6	68.2	62.2



Figure 40 – Ambient = 27 °C.
Inn3168C, U1 = 73.4 °C.

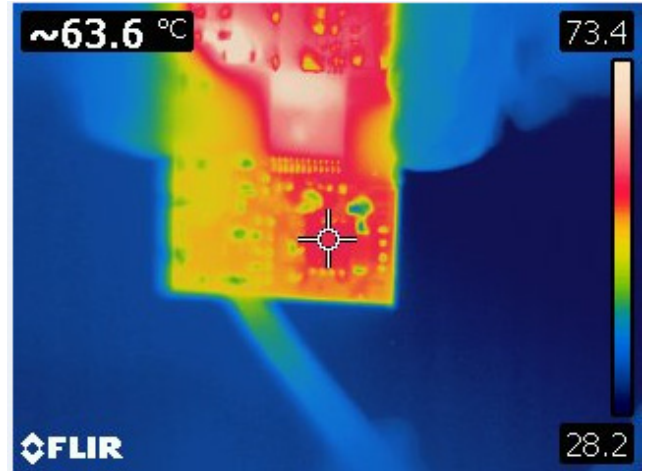


Figure 41 – Ambient = 28 °C.
SR FET, Q3 = 63.6 °C.

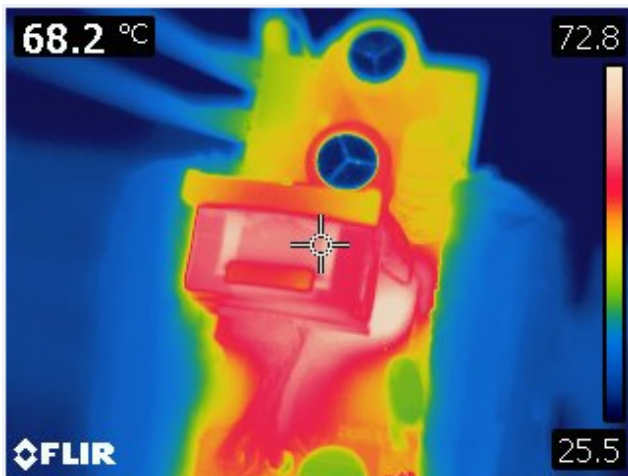


Figure 42 – Ambient = 26 °C.
Transformer, T2 = 68.2 °C.

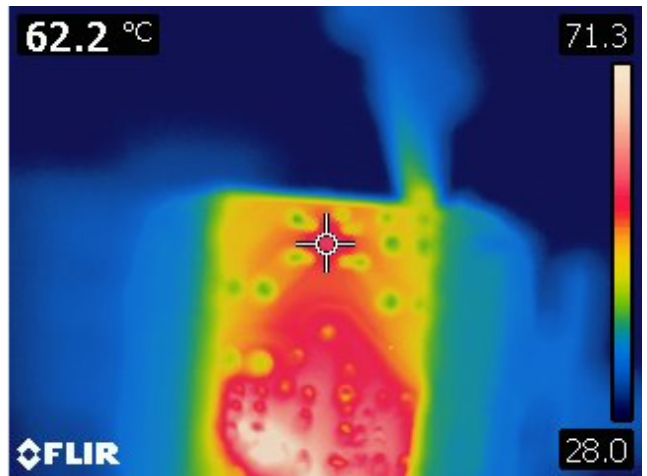


Figure 43 – Ambient = 27 °C.
Bridge Diode, BR1 = 62.2 °C.

11.4 Open Case at 5.1 V / 6 A (50 °C)

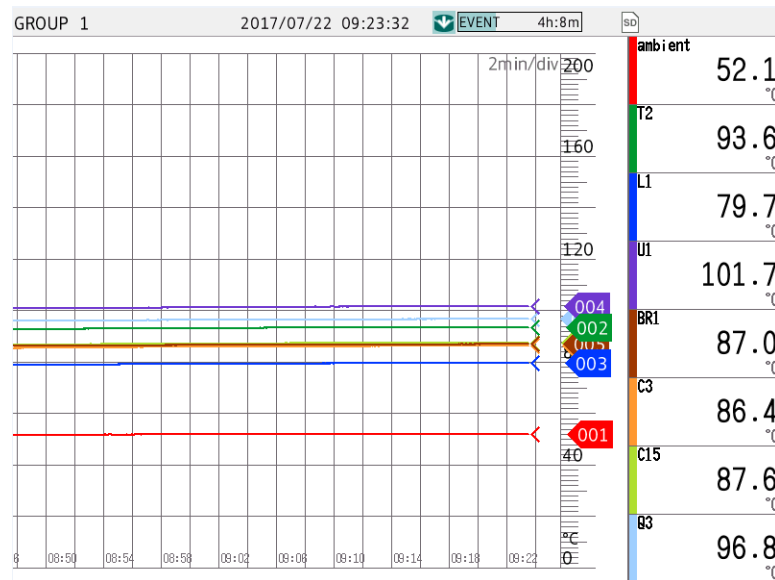


Figure 44 – Test Set-up Picture.

Unit was placed inside a box enclosure to prevent airflow that might affect the thermal measurements. Ambient temperature was set to 50 °C. Temperature was measured using type T thermocouple.

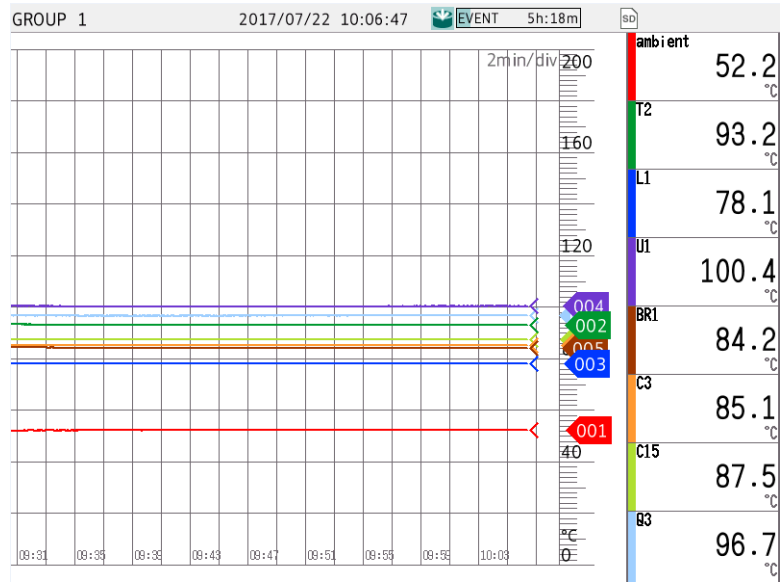
11.4.1 100 VAC @ 50 °C Ambient

Ambient (°C)	INN3268C (U1)	SR FET (Q3)	Transformer (T2)	Bridge (BR1)	CMC (L1)	Input Capacitor (C3)	Output Capacitor (C15)
52.1	101.7	96.8	93.6	87	79.7	86.4	87.6



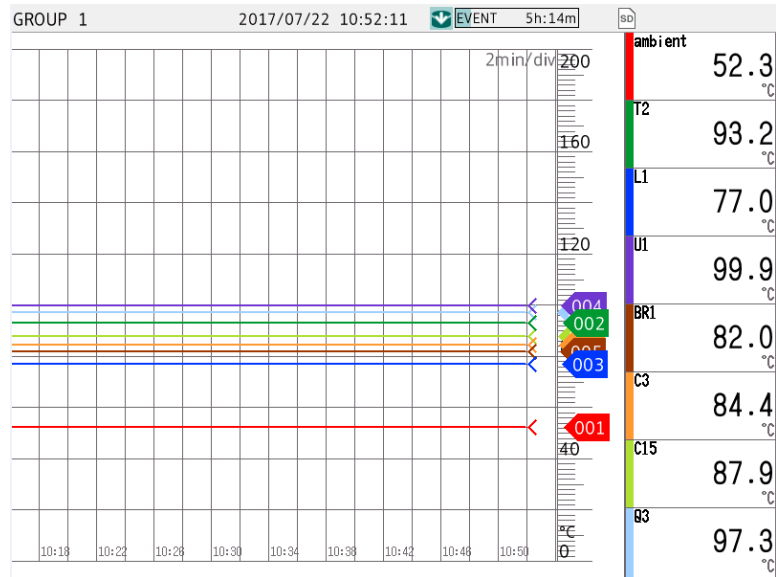
11.4.2 115 VAC @ 50 °C Ambient

Ambient (°C)	Inn3268C (U1)	SR FET (Q3)	Transformer (T2)	Bridge (BR1)	CMC (L1)	Input Capacitor (C3)	Output Capacitor (C15)
52.2	100.4	96.7	93.2	84.2	78.1	85.1	87.5



11.4.3 132 VAC @ 50 °C Ambient

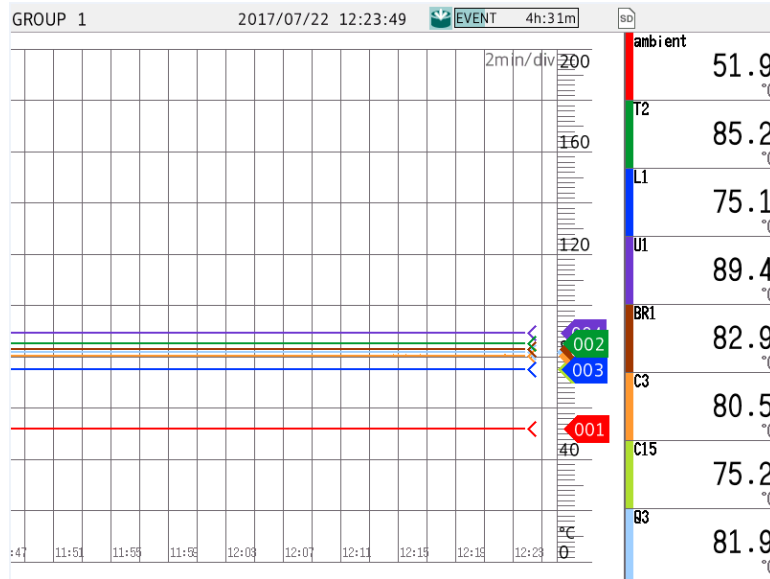
Ambient (°C)	Inn3268C (U1)	SR FET (Q3)	Transformer (T2)	Bridge (BR1)	CMC (L1)	Input Capacitor (C3)	Output Capacitor (C15)
52.3	99.9	97.3	93.2	82	77	84.4	87.9



11.5 Open Case at 9.2 V / 3.3 A (50 °C)

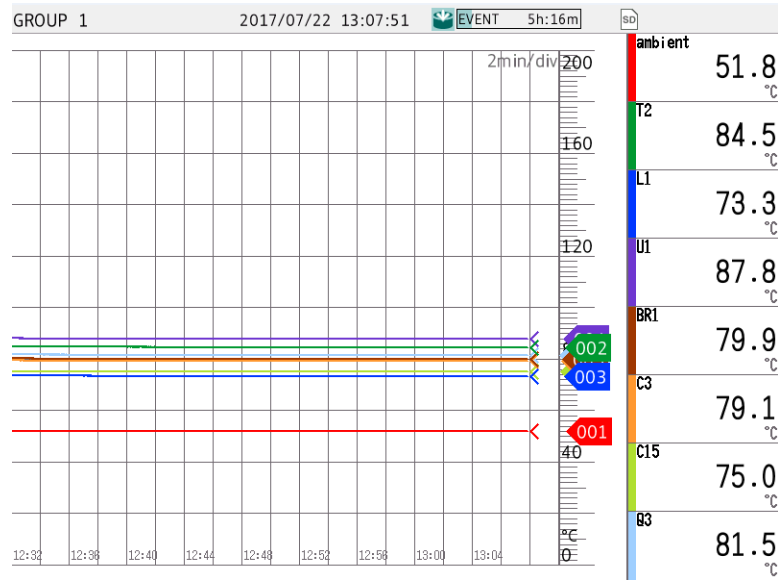
11.5.1 100 VAC @ 50 °C Ambient

Ambient (°C)	Inn3268C (U1)	SR FET (Q3)	Transformer (T2)	Bridge (BR1)	CMC (L1)	Input Capacitor (C3)	Output Capacitor (C15)
51.9	89.4	81.9	85.2	82.9	75.1	80.5	75.2



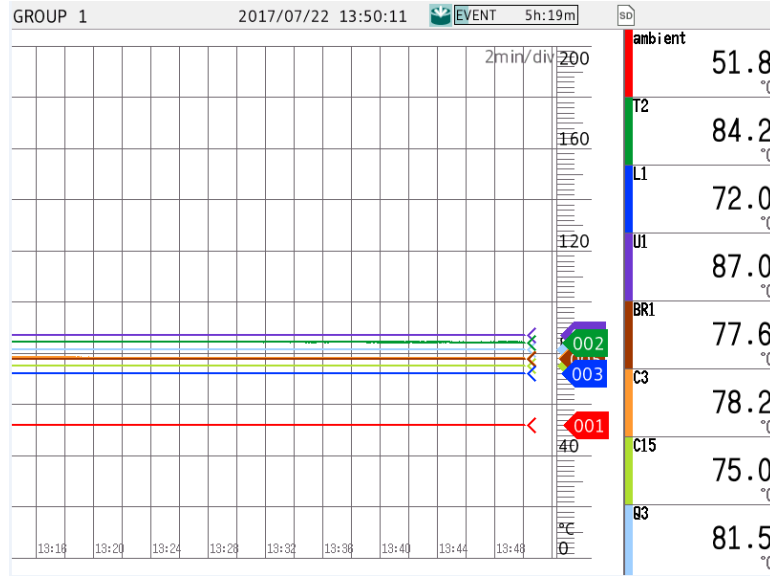
11.5.2 115VAC @ 50 °C Ambient

Ambient (°C)	Inn3268C (U1)	SR FET (Q3)	Transformer (T2)	Bridge (BR1)	CMC (L1)	Input Capacitor (C3)	Output Capacitor (C15)
51.8	87.8	81.5	84.5	79.9	73.3	79.1	75



11.5.3 132 VAC @ 50 °C Ambient

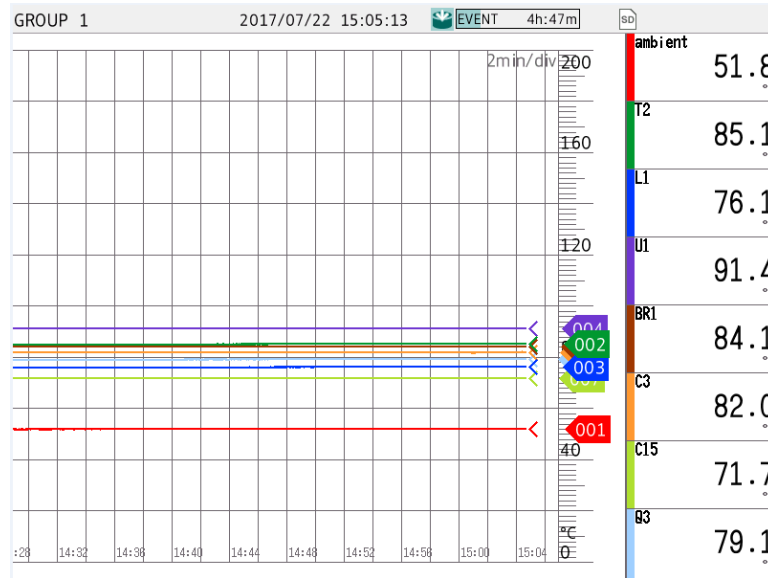
Ambient (°C)	Inn3268C (U1)	SR FET (Q3)	Transformer (T2)	Bridge (BR1)	CMC (L1)	Input Capacitor (C3)	Output Capacitor (C15)
51.8	87.0	81.5	84.2	77.6	72	78.2	75



11.6 Open Case at 15.3 V / 2 A (50°C)

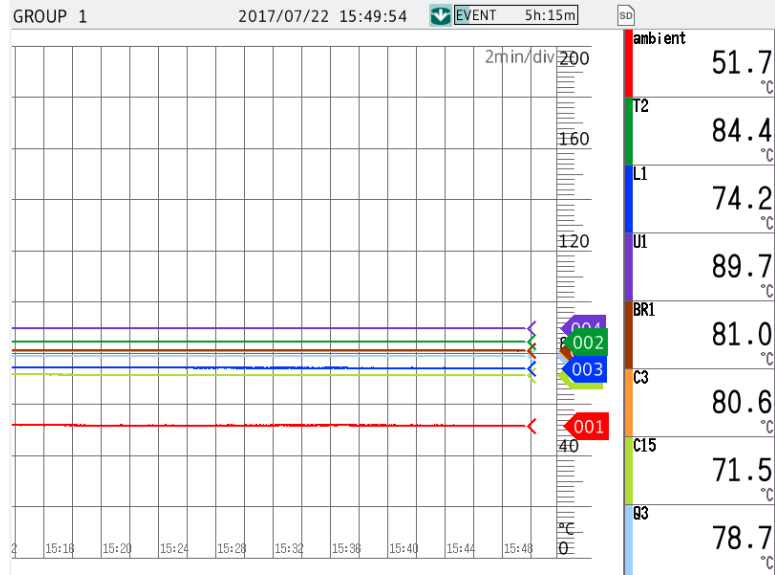
11.6.1 100 VAC @ 50 °C Ambient

Ambient (°C)	Inn3268C (U1)	SR FET (Q3)	Transformer (T2)	Bridge (BR1)	CMC (L1)	Input Capacitor (C3)	Output Capacitor (C15)
51.8	91.4	79.1	85.1	84.1	76.1	82	71.7



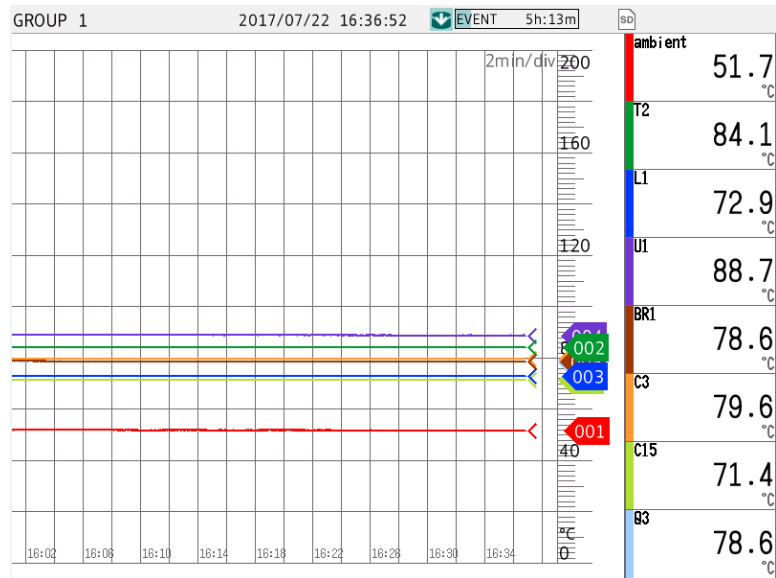
11.6.2 115 VAC @ 50 °C Ambient

Ambient (°C)	Inn3268C (U1)	SR FET (Q3)	Transformer (T2)	Bridge (BR1)	CMC (L1)	Input Capacitor (C3)	Output Capacitor (C15)
50	89.7	78.7	84.4	81	74.2	80.6	71.5



11.6.3 132 VAC @ 50 °C Ambient

Ambient (°C)	INN3268C (U1)	SR MOSFET (Q3)	Transformer (T2)	Bridge (BR1)	CMC (L1)	Input Capacitor (C3)	Output Capacitor (C15)
50	88.7	78.6	84.1	78.6	72.9	79.6	71.4



12 Waveforms

12.1 Load Transient Response (PCB End)

12.1.1 5.1 V Output

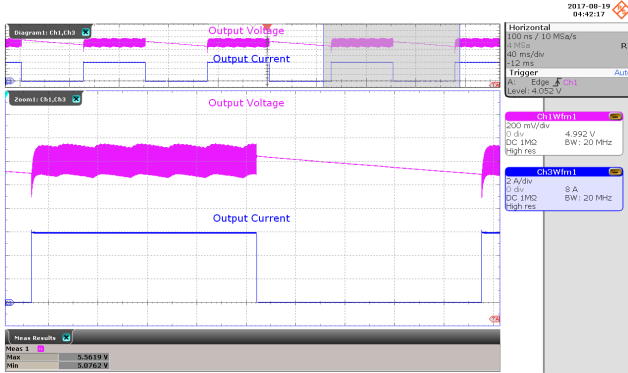


Figure 45 – Transient Response.
 100 VAC, 5.1 V, 0 – 6 A Load Step.
 V_{MIN} : 5.07 V, V_{MAX} : 5.56 V.
 Upper: V_{OUT} , 0.2 V / div., 40 ms / div.
 Lower: I_{LOAD} , 2 A / div.

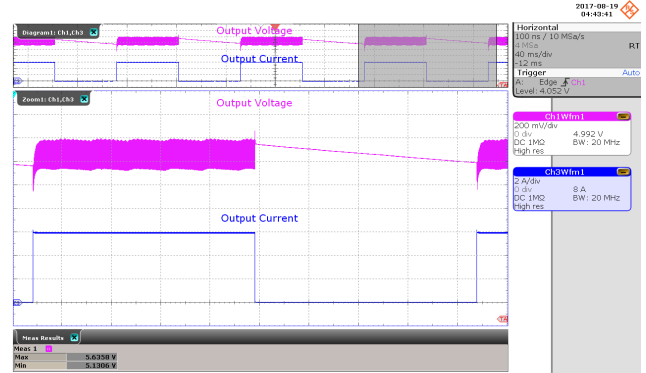


Figure 46 – Transient Response.
 132 VAC, 5.1 V, 0 – 6 A Load Step.
 V_{MIN} : 5.13 V, V_{MAX} : 5.63 V.
 Upper: V_{OUT} , 0.2 V / div., 40 ms / div.
 Lower: I_{LOAD} , 2 A / div.

12.1.2 9.2 V Output

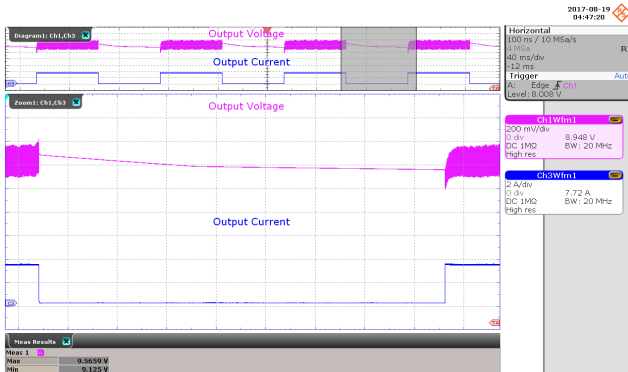


Figure 47 – Transient Response.
 100 VAC, 9.2 V, 0 – 3.3 A Load Step.
 V_{MIN} : 9.12 V, V_{MAX} : 9.56 V.
 Upper: V_{OUT} , .2 V / div., 40 ms / div.
 Lower: I_{LOAD} , 2 A / div.

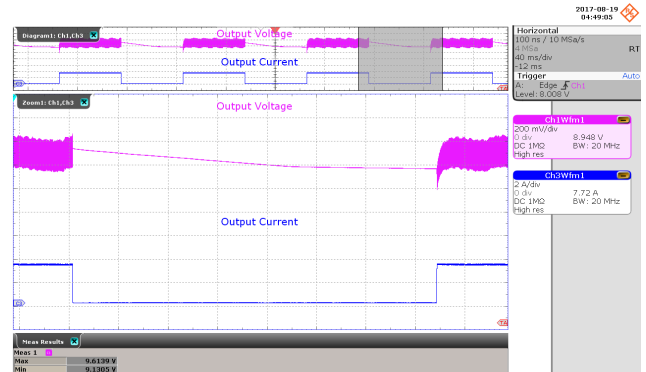


Figure 48 – Transient Response.
 132 VAC, 9.2 V, 0 – 3.3 A Load Step.
 V_{MIN} : 9.13 V, V_{MAX} : 9.61 V.
 Upper: V_{OUT} , .2 V / div., 40 ms / div.
 Lower: I_{LOAD} , 2 A / div.



12.1.3 15.3 V Output

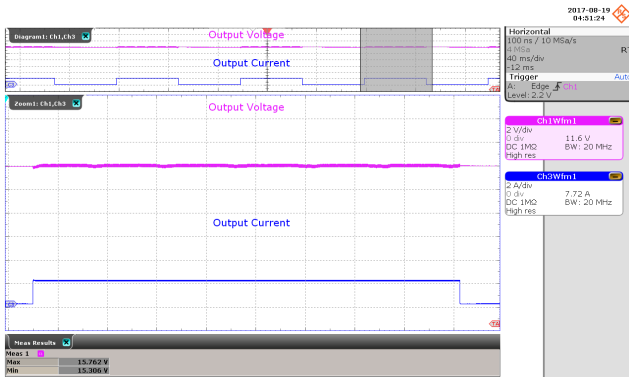


Figure 49 – Transient Response.
 100 VAC, 15.3 V, 0 – 2 A Load Step.
 V_{MIN} : 15.31 V, V_{MAX} : 15.76 V.
 Upper: V_{OUT} , 2 V / div., 40 ms / div.
 Lower: I_{LOAD} , 2 A / div.

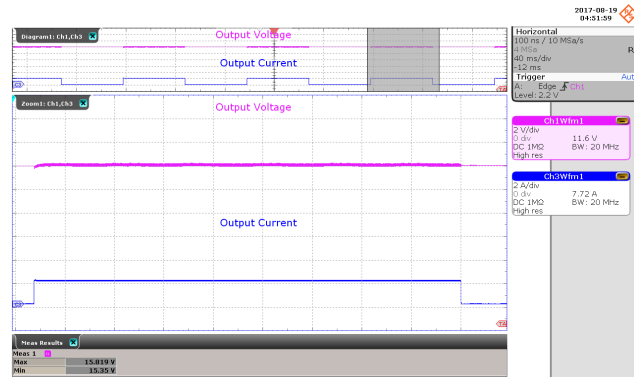


Figure 50 – Transient Response.
 132 VAC, 15.3 V, 0 – 2 A Load Step.
 V_{MIN} : 15.35 V, V_{MAX} : 15.82 V.
 Upper: V_{OUT} , 2 V / div., 40 ms / div.
 Lower: I_{LOAD} , 2 A / div.

12.2 Switching Waveforms

12.2.1 Drain Voltage and Current (Normal Operation)

12.2.1.1 5 V Output

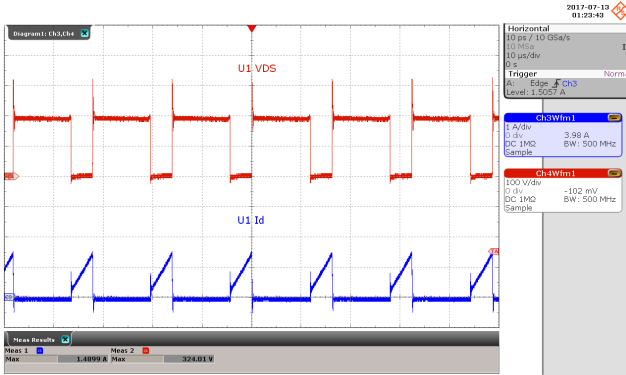


Figure 51 – Drain Voltage and Current Waveforms.
 100 VAC, 5.1 V, 6.0 A Load, (324 V_{MAX}).
 Upper: V_{DRAIN} , 100 V, 10 μ s / div.
 Lower: I_{DRAIN} , 1 A / div.

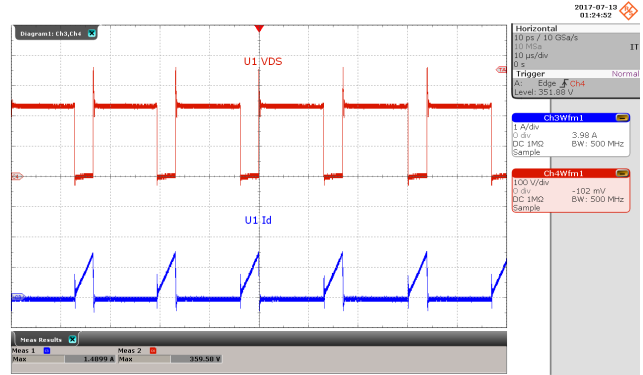


Figure 52 – Drain Voltage and Current Waveforms.
 132 VAC, 5.1 V, 6.0 A Load, (360 V_{MAX}).
 Upper: V_{DRAIN} , 100 V, 10 μ s / div.
 Lower: I_{DRAIN} , 1 A / div.

12.2.1.2 9 V Output

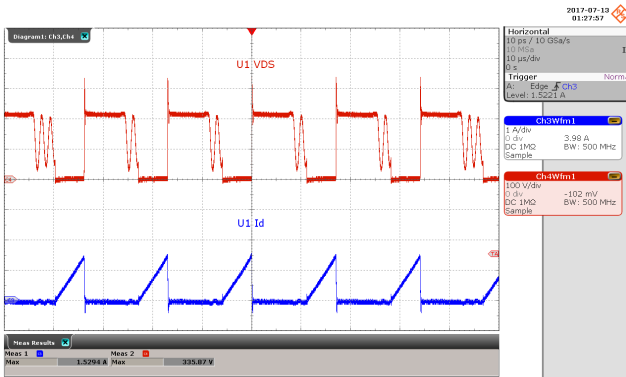


Figure 53 – Drain Voltage and Current Waveforms.
 100 VAC, 9.0 V, 3.3 A Load, (336 V_{MAX}).
 Upper: V_{DRAIN} , 100 V, 10 μ s / div.
 Lower: I_{DRAIN} , 1 A / div.

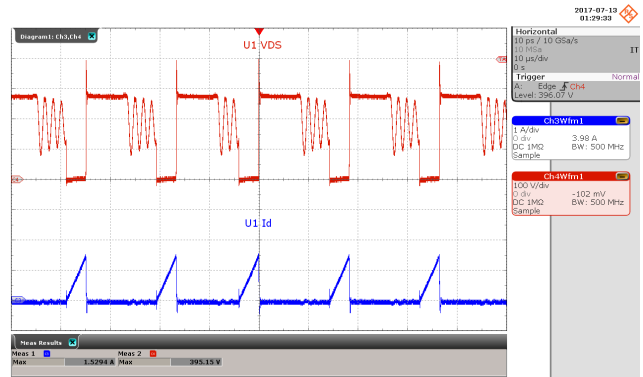


Figure 54 – Drain Voltage and Current Waveforms.
 132 VAC, 9.0 V, 3.3 A Load, (395 V_{MAX}).
 Upper: V_{DRAIN} , 100 V, 10 μ s / div.
 Lower: I_{DRAIN} , 1 A / div.



12.2.1.3 15 V Output

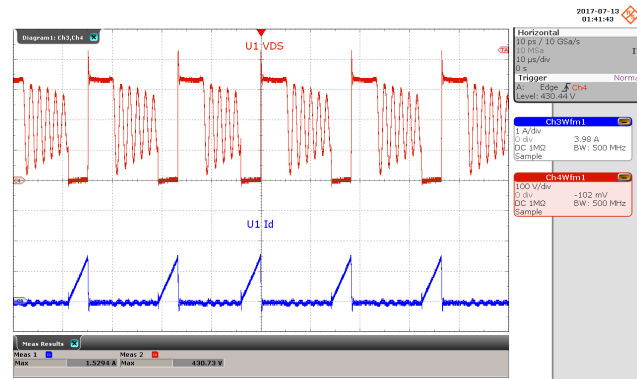
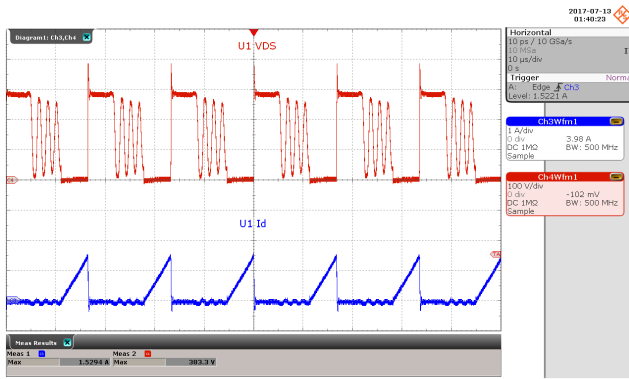


Figure 55 – Drain Voltage and Current Waveforms.
 100 VAC, 15.0 V, 2.0 A Load, (383 V_{MAX}).
 Upper: V_{DRAIN} , 100 V, 10 μs / div.
 Lower: I_{DRAIN} , 1 A / div.

Figure 56 – Drain Voltage and Current Waveforms.
 132 VAC, 15.0 V, 2.0 A Load, (431 V_{MAX}).
 Upper: V_{DRAIN} , 100 V, 10 μs / div.
 Lower: I_{DRAIN} , 1 A / div.

12.2.2 Drain Voltage and Current (Start-up)

12.2.2.1 5 V Output

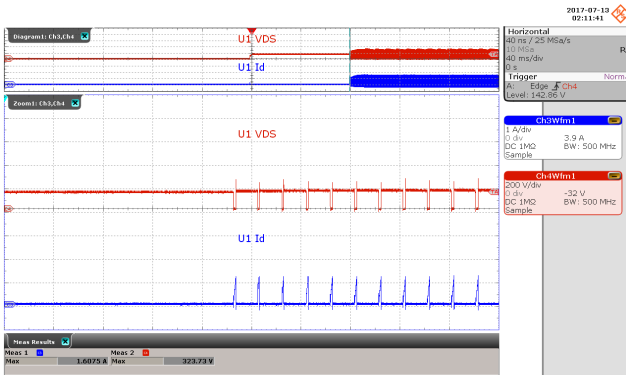


Figure 57 – Drain Voltage and Current Waveforms.
 100 VAC, 5.1 V, 6.0 A Load, (324 V_{MAX}).
 Upper: V_{DRAIN} , 100 V, 40 ms / div.
 Lower: I_{DRAIN} , 1 A / div.

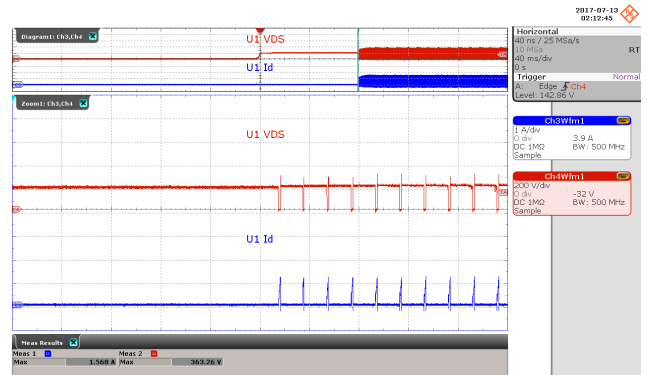


Figure 58 – Drain Voltage and Current Waveforms.
 132 VAC, 5.1 V, 6.0 A Load, (363 V_{MAX}).
 Upper: V_{DRAIN} , 100 V, 40 ms / div.
 Lower: I_{DRAIN} , 1 A / div.

12.2.2.2 9 V Output

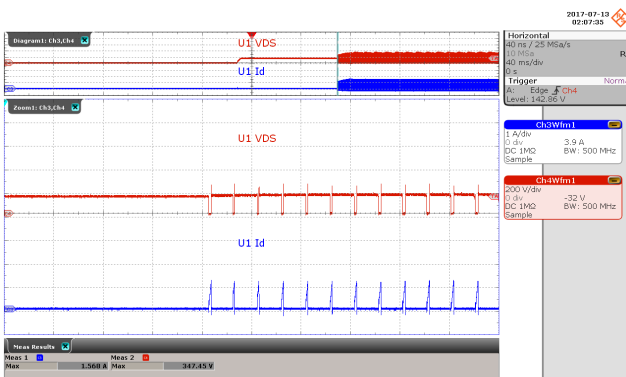


Figure 59 – Drain Voltage and Current Waveforms.
 100 VAC, 9.0 V, 3.3 A Load, (347 V_{MAX}).
 Upper: V_{DRAIN} , 100 V, 40 ms / div.
 Lower: I_{DRAIN} , 1 A / div.

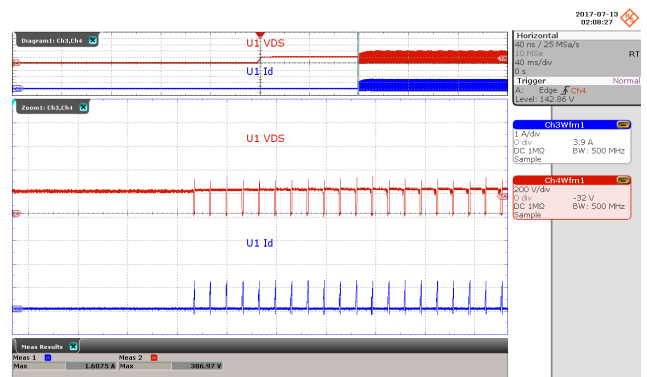


Figure 60 – Drain Voltage and Current Waveforms.
 132 VAC, 9.0 V, 3.3 A Load, (387 V_{MAX}).
 Upper: V_{DRAIN} , 100 V, 40 ms / div.
 Lower: I_{DRAIN} , 1 A / div.



12.2.2.3 15 V Output

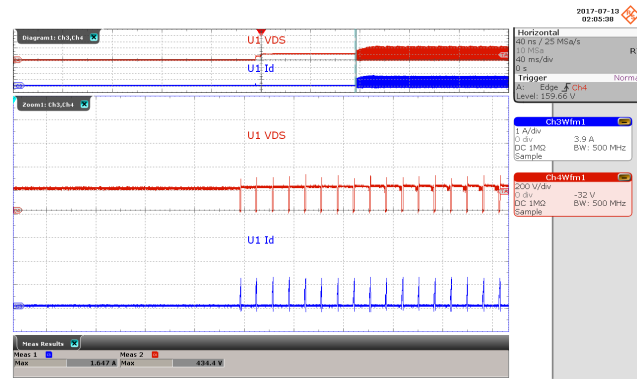
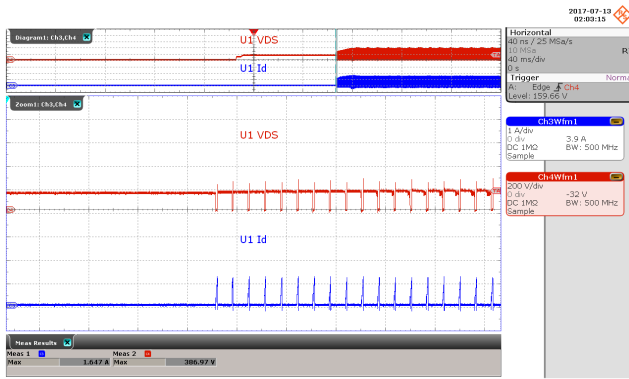


Figure 61 – Drain Voltage and Current Waveforms.
 100 VAC, 15.0 V, 2.0 A Load, (387 V_{MAX}).
 Upper: V_{DRAIN}, 100 V, 40 ms / div.
 Lower: I_{DRAIN}, 1 A / div.

Figure 62 – Drain Voltage and Current Waveforms.
 132 VAC, 15.0 V, 2.0 A Load, (434 V_{MAX}).
 Upper: V_{DRAIN}, 100 V, 40 ms / div.
 Lower: I_{DRAIN}, 1 A / div.

12.2.3 SR MOSFET Voltage

12.2.3.1 5 V Output

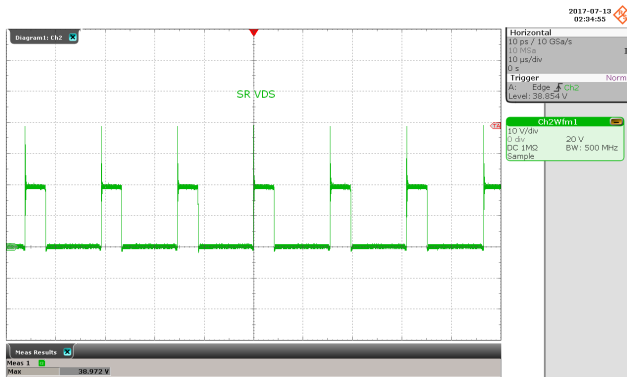


Figure 63 – SR FET Voltage Waveform.
 100 VAC, 5.1 V, 6.0 A Load, (38.9 V_{MAX}).
 V_{DRAIN}, 10 V, 10 μs / div.

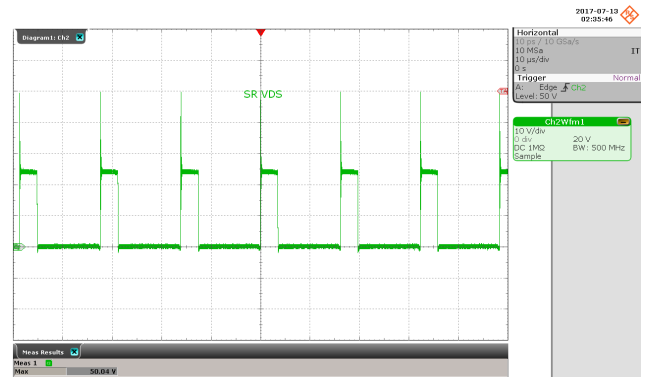


Figure 64 – SR FET Voltage Waveform.
 132 VAC, 5.1 V, 6.0 A Load, (50.1 V_{MAX}).
 V_{DRAIN}, 10 V, 10 μs / div.

12.2.3.2 9 V Output

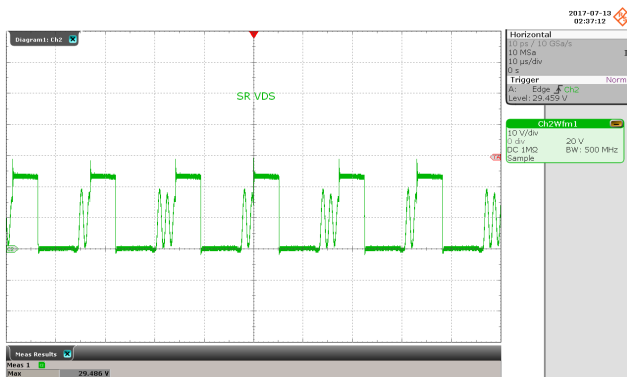


Figure 65 – SR1 FET Voltage Waveform.
 100 VAC, 9.0 V, 3.3 A Load, (29.5 V_{MAX}).
 V_{DRAIN}, 10 V, 10 μs / div.

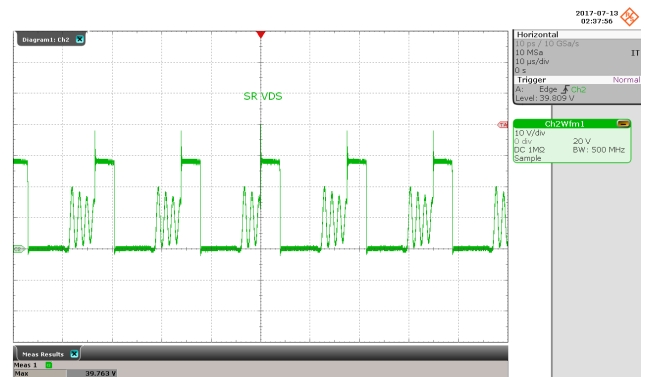


Figure 66 – SR1 FET Voltage Waveform.
 132 VAC, 9.0 V, 3.3 A Load, (39.7 V_{MAX}).
 V_{DRAIN}, 10 V, 10 μs / div.



12.2.3.3 15 V Output

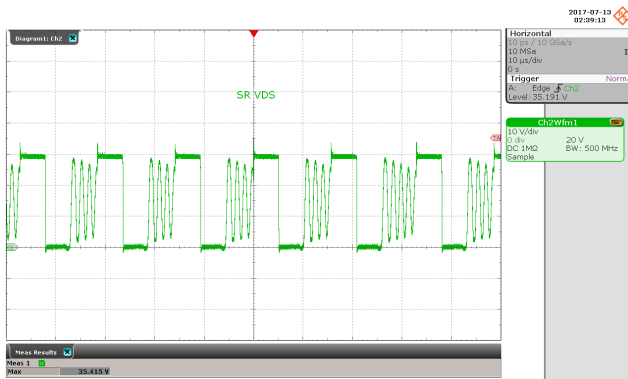


Figure 67 – SR FET Voltage Waveform.
100 VAC, 15.0 V, 2.0 A Load, (35.4 V_{MAX}).
V_{DRAIN}, 10 V, 10 μs / div.

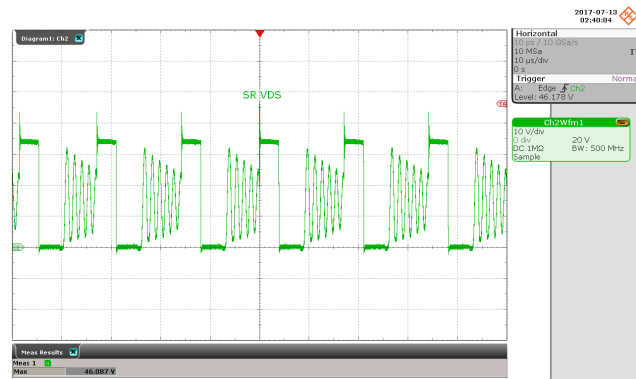


Figure 68 – SR FET Voltage Waveform.
132 VAC, 15.0 V, 2.0 A Load, (46.1 V_{MAX}).
V_{DRAIN}, 10 V, 10 μs / div.

12.2.4 Output Voltage and Current Start-up (End of 100 mΩ Cable)

12.2.4.1 5 V Output

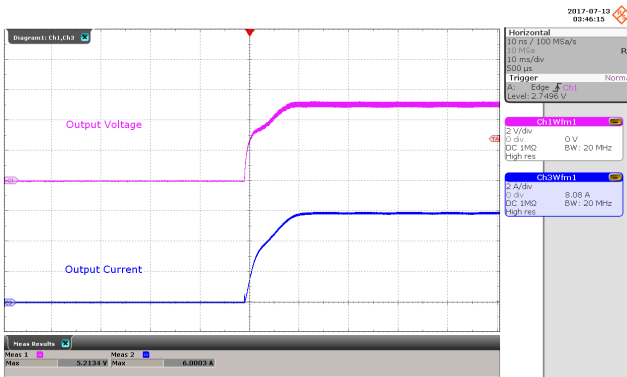


Figure 69 – Output Voltage and Current Waveforms.
 100 VAC Input, 5.1 V, 0.85 Ω Load .
 Upper: I_{OUT} , 2 A, 10 ms / div.
 Lower: V_{OUT} , 2 V / div.

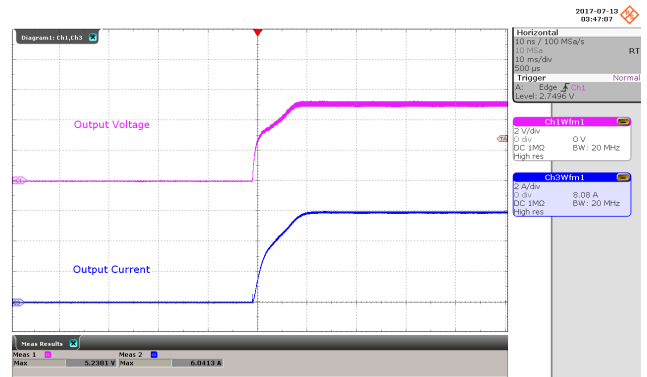


Figure 70 – Output Voltage and Current Waveforms.
 132 VAC Input, 5.1 V, 0.85 Ω Load.
 Upper: I_{OUT} , 2 A, 10 ms / div.
 Lower: V_{OUT} , 2 V / div.

12.2.4.2 9 V Output

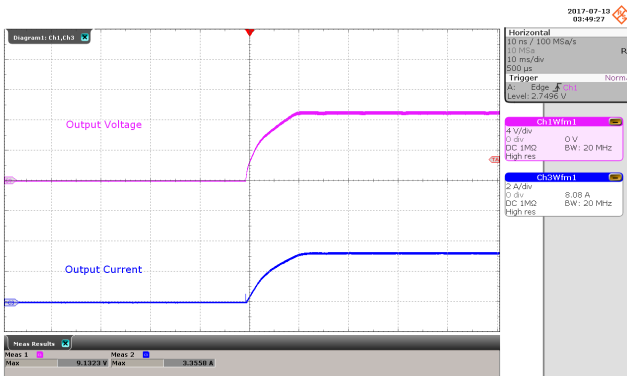


Figure 71 – Output Voltage and Current Waveforms.
 100 VAC Input, 9 V, 2.75 Ω Load .
 Upper: I_{OUT} , 1 A, 10 ms / div.
 Lower: V_{OUT} , 2 V / div.

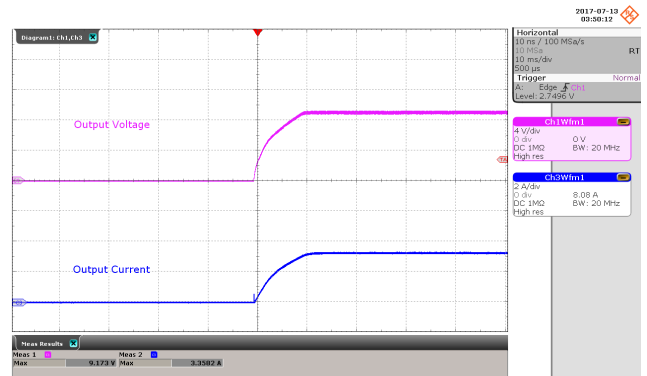


Figure 72 – Output Voltage and Current Waveforms.
 132 VAC Input, 9 V, 2.75 Ω Load.
 Upper: I_{OUT} , 1 A, 10 ms / div.
 Lower: V_{OUT} , 2 V / div.



12.2.4.3 15 V Output

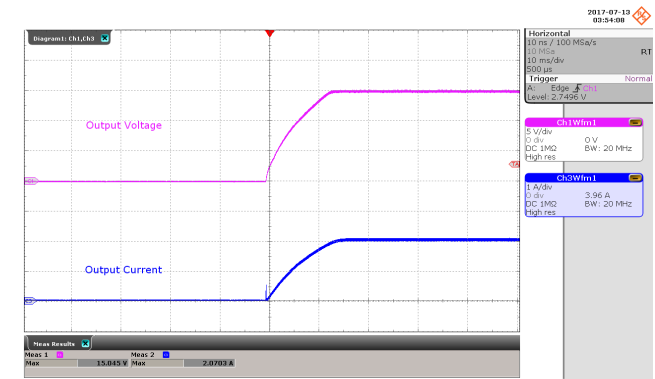
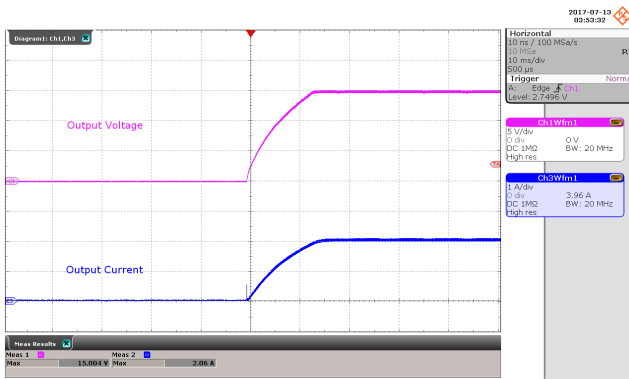


Figure 73 – Output Voltage and Current Waveforms.
 100 VAC Input, 15 V, 7.5 Ω Load .
 Upper: I_{OUT} , 1 A, 50 ms / div.
 Lower: V_{OUT} , 5 V / div.

Figure 74 – Output Voltage and Current Waveforms.
 132 VAC Input, 15 V, 7.5 Ω Load.
 Upper: I_{OUT} , 1 A, 50 ms / div.
 Lower: V_{OUT} , 5 V / div.

12.3 Output Ripple Measurements

12.3.1 Ripple Measurement Technique

For DC output ripple measurements, a modified oscilloscope test probe must be utilized in order to reduce spurious signals due to pick-up. Details of the probe modification are provided in the Figures below.

The 4987BA probe adapter is affixed with two capacitors tied in parallel across the probe tip. The capacitors include one (1) 0.1 $\mu\text{F}/50\text{ V}$ ceramic type and one (1) 47 $\mu\text{F}/50\text{ V}$ aluminum electrolytic. The aluminum electrolytic type capacitor is polarized, so proper polarity across DC outputs must be maintained (see below). Ripple measurement done at the end of a 100m Ω cable.

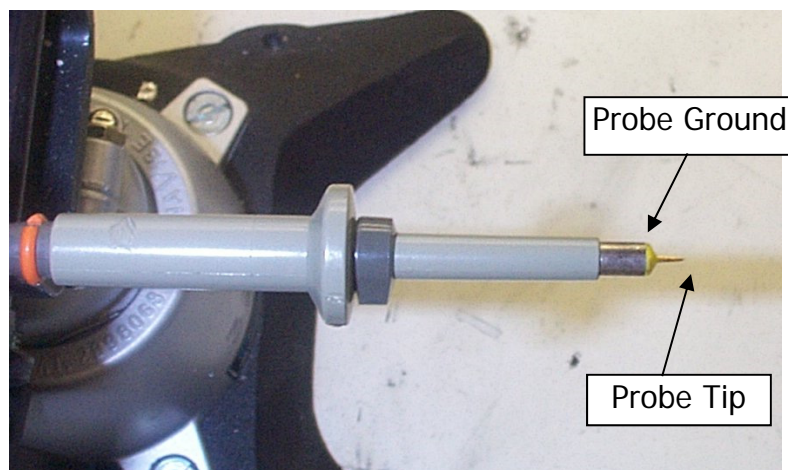


Figure 75 – Oscilloscope Probe Prepared for Ripple Measurement. (End Cap and Ground Lead Removed)

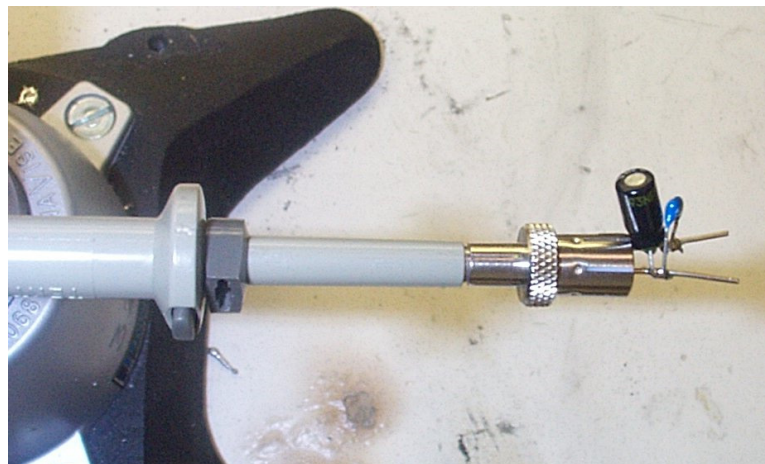


Figure 76 – Oscilloscope Probe with Probe Master (www.probemaster.com) 4987A BNC Adapter. (Modified with wires for ripple measurement, and two parallel decoupling capacitors added)

12.3.1.1 5 V Output

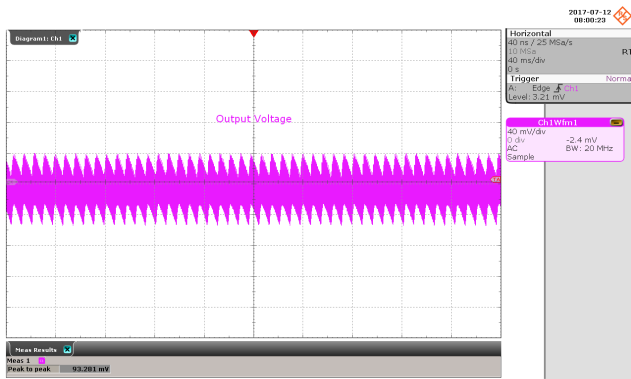


Figure 77 – Output Ripple.
 100 VAC Input 5.1 V, 6.0 A Load.
 V_{OUT} , 40 mV / div., 40 ms / div.

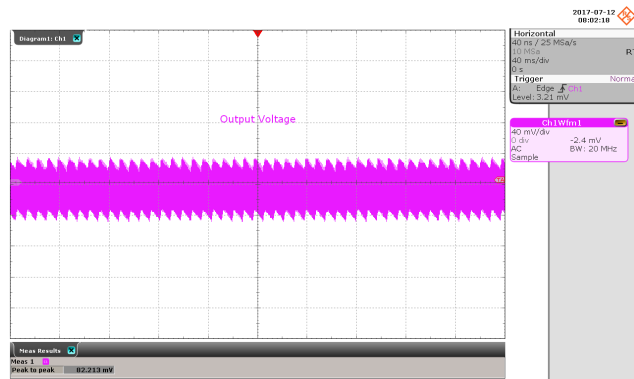


Figure 78 – Output Ripple.
 132 VAC Input 5.1 V, 6.0 A Load.
 V_{OUT} , 40 mV / div., 40 ms / div.

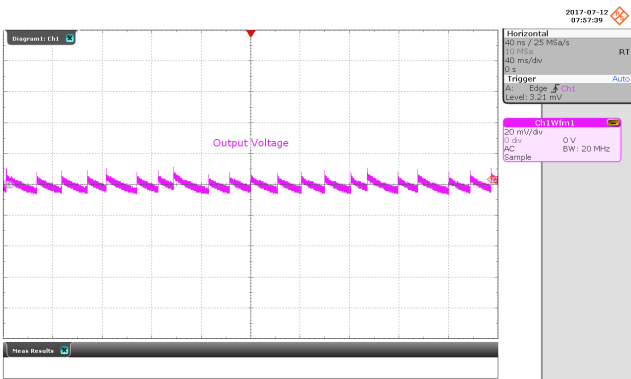


Figure 79 – Output Ripple.
 100 VAC Input 5.1 V, 0 A Load.
 V_{OUT} , 20 mV / div., 40 ms / div.

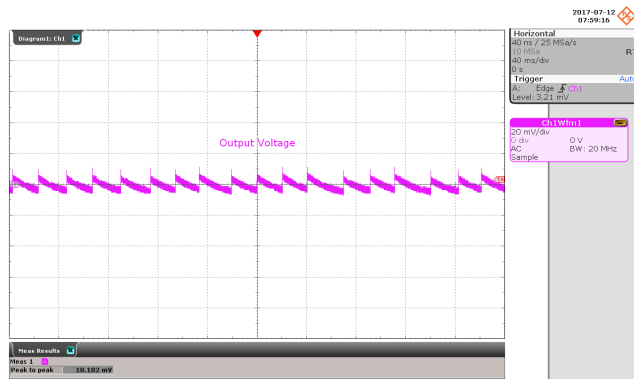


Figure 80 – Output Ripple.
 132 VAC Input 5.1 V, 0 A Load.
 V_{OUT} , 20 mV / div., 40 ms / div.

Input (VAC)	Full Load (mV)	No-Load (mV)
100	93.3	17.8
132	82.2	18.1

12.3.1.2 9 V Output

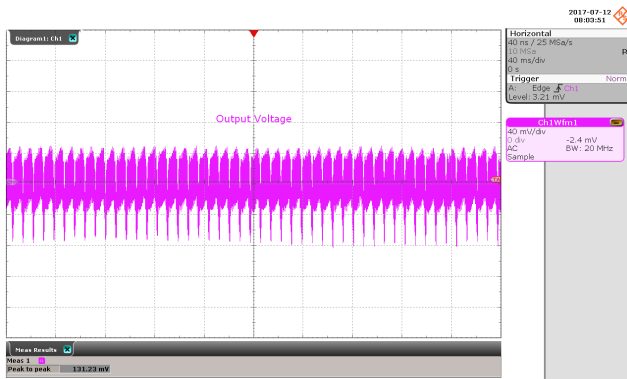


Figure 81 – Output Ripple.
 100 VAC Input, 9.0 V, 3.3 A Load.
 V_{OUT} , 40 mV / div., 40 ms / div.

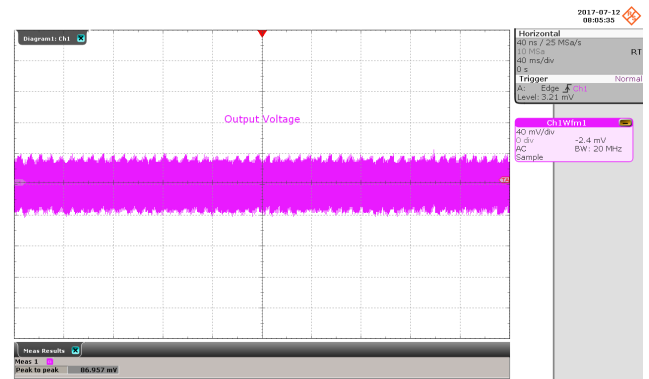


Figure 82 – Output Ripple.
 132 VAC Input 9.0 V, 3.3 A Load.
 V_{OUT} , 40 mV / div., 40 ms / div.

12.3.1.3 15 V Output

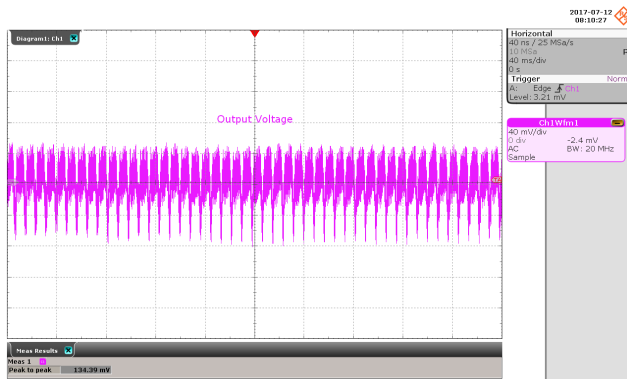


Figure 83 – Output Ripple.
 100 VAC Input, 15.0 V, 2.0 A Load.
 V_{OUT} , 40 mV / div., 40 ms / div.

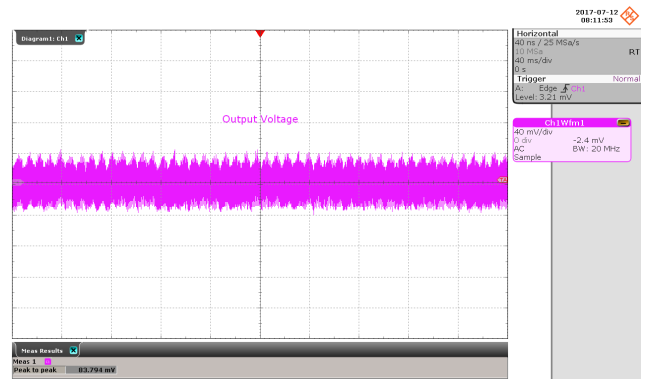


Figure 84 – Output Ripple.
 132 VAC Input 15.0 V, 2.0 A Load.
 V_{OUT} , 40 mV / div., 40 ms / div.

Input (VAC)	9V (mV)	15V (mV)
90	131.2	134.4
132	86.5	83.8



13 Conducted EMI

13.1 Test Set-up

13.1.1 Equipment and Load Used

1. Rohde and Schwarz ENV216 two line V-network.
2. Rohde and Schwarz ESRP EMI test receiver.
3. Hioki 3322 power hitester.
4. Chroma measurement test fixture, model A662003.
5. Resistor load with input voltage set at 115 VAC.

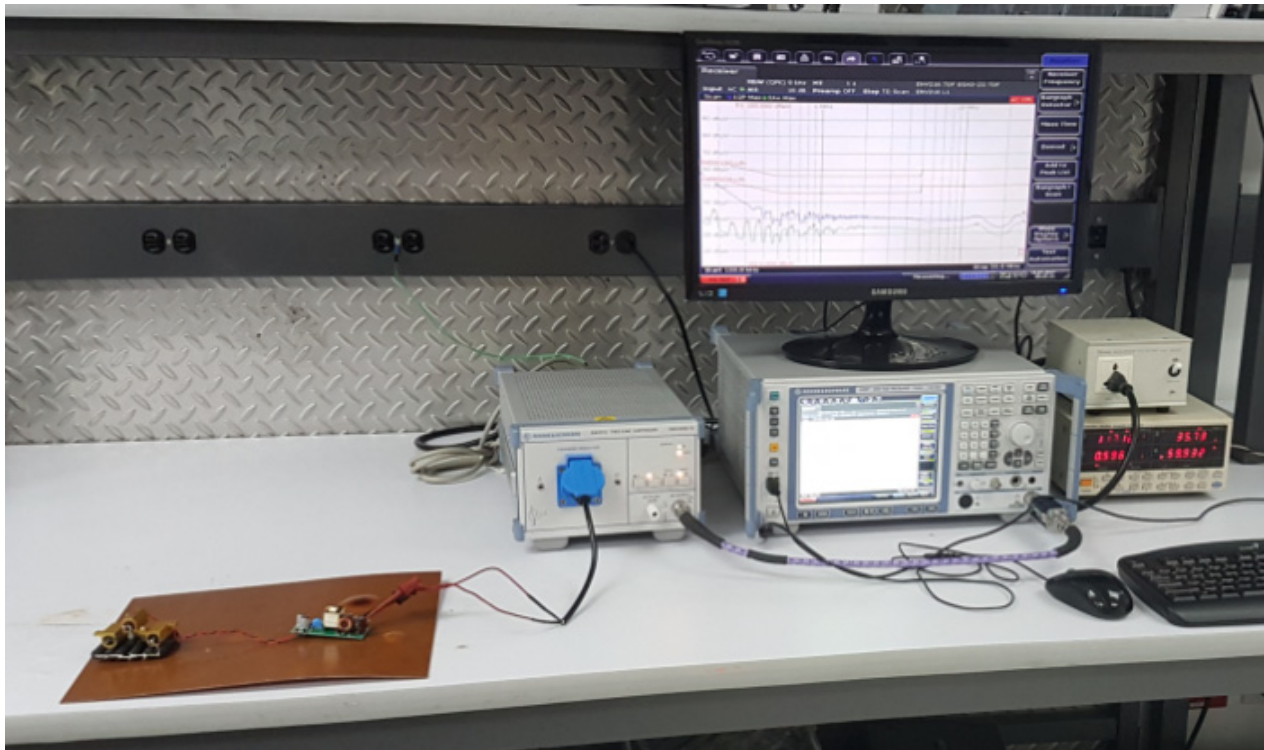


Figure 85 – Conducted EMI Test Set-up.

13.2 EMI Test Result

13.2.1 Floating Output

13.2.1.1 Output 5.1 V / 6 A

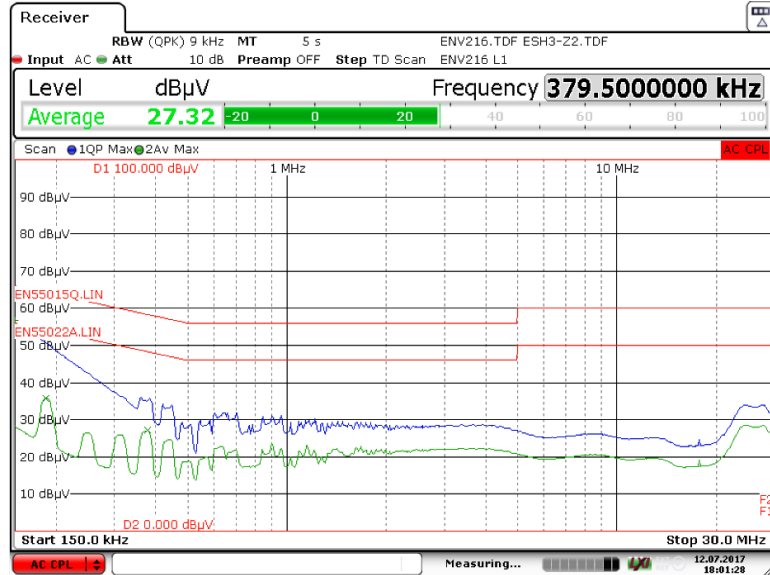


Figure 86 – Conducted EMI, 5.1 V / 6 A Load 115 VAC, 60 Hz, and EN55022 B Limits (Line).

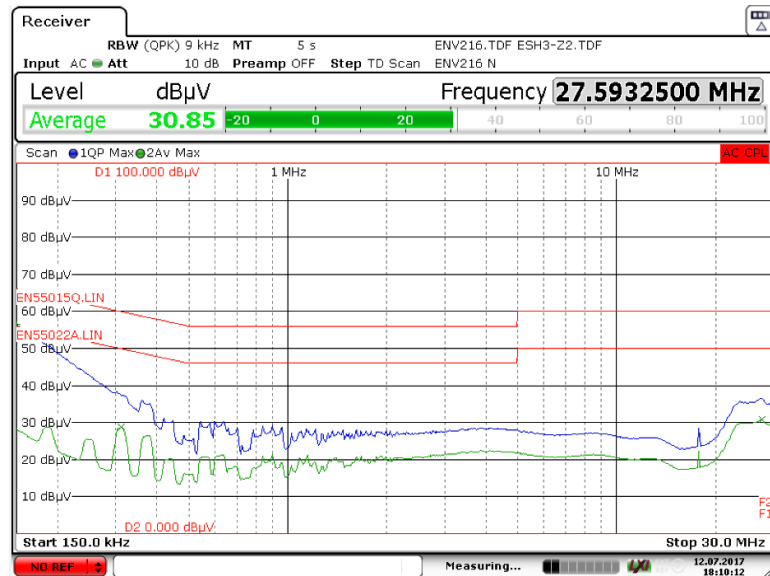


Figure 87 – Conducted EMI, 5.1 V / 6 A Load 115 VAC, 60 Hz, and EN55022 B Limits (Neutral).

13.2.1.2 Output 9 V / 3.3 A

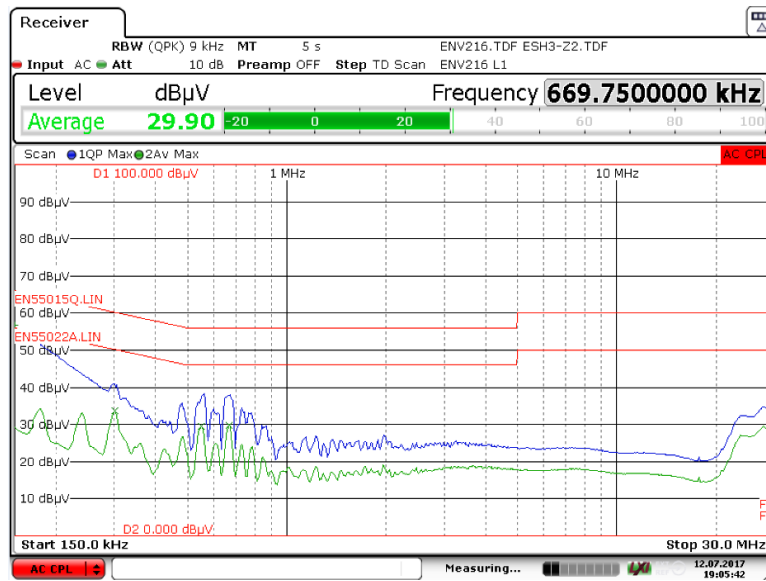


Figure 88 – Conducted EMI, 9 V / 3.3 A Load 115 VAC, 60 Hz, and EN55022 B Limits (Line).

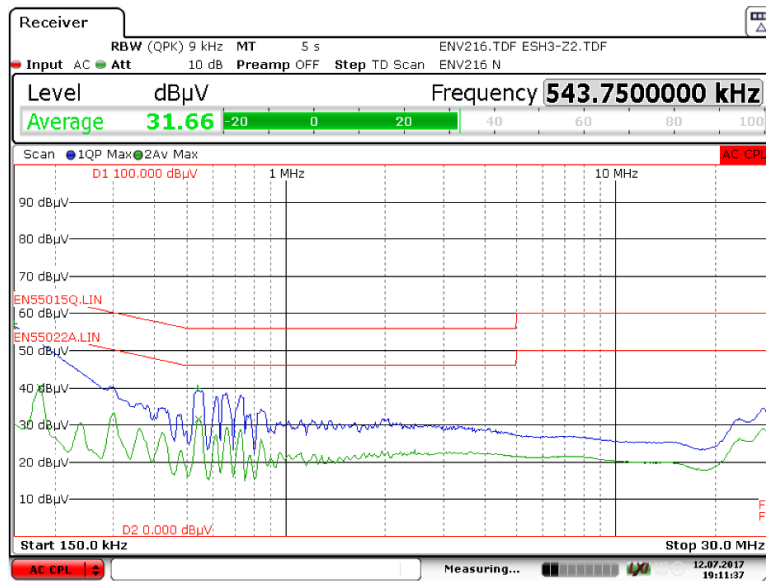


Figure 89 – Conducted EMI, 9 V / 3.3 A Load 115 VAC, 60 Hz, and EN55022 B Limits (Neutral).

13.2.1.3 Output 15 V / 2 A

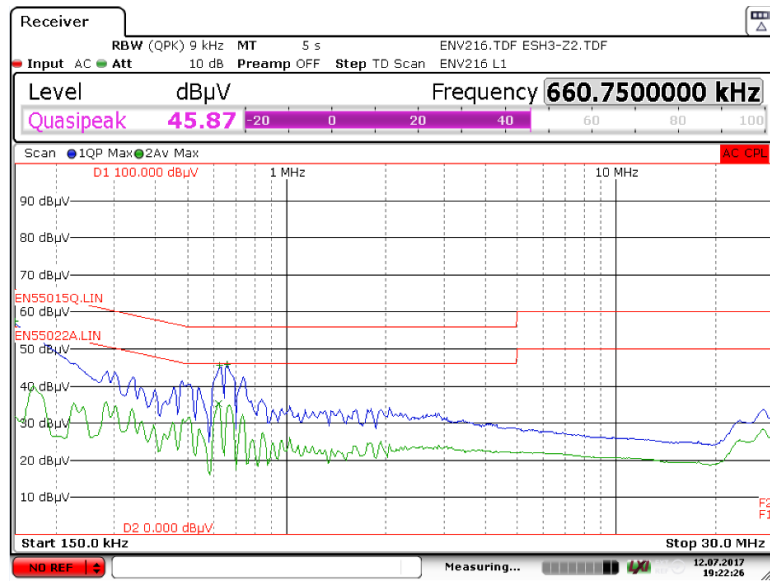


Figure 90 – Conducted EMI, 15 V / 2 A Load 115 VAC, 60 Hz, and EN55022 B Limits (Line).

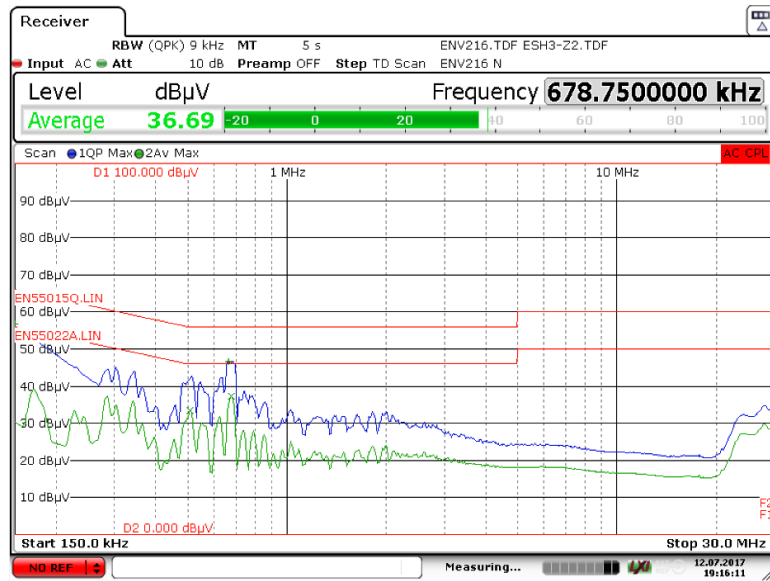


Figure 91 – Conducted EMI, 15 V / 2 A Load 115 VAC, 60 Hz, and EN55022 B Limits (Neutral).



13.2.2 Artificial Hand

13.2.2.1 Output 5.1 V / 6 A

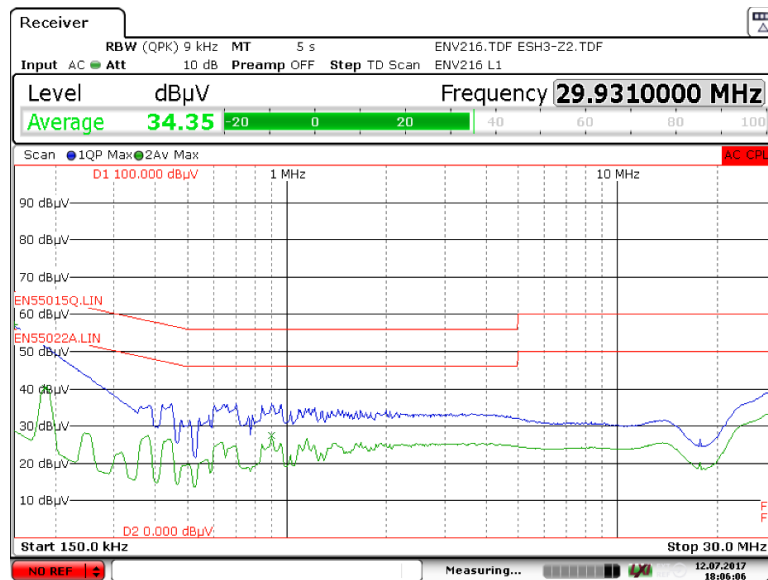


Figure 92 – Conducted EMI, 5.1 V / 6 A Load 115 VAC, 60 Hz, and EN55022 B Limits (Line).

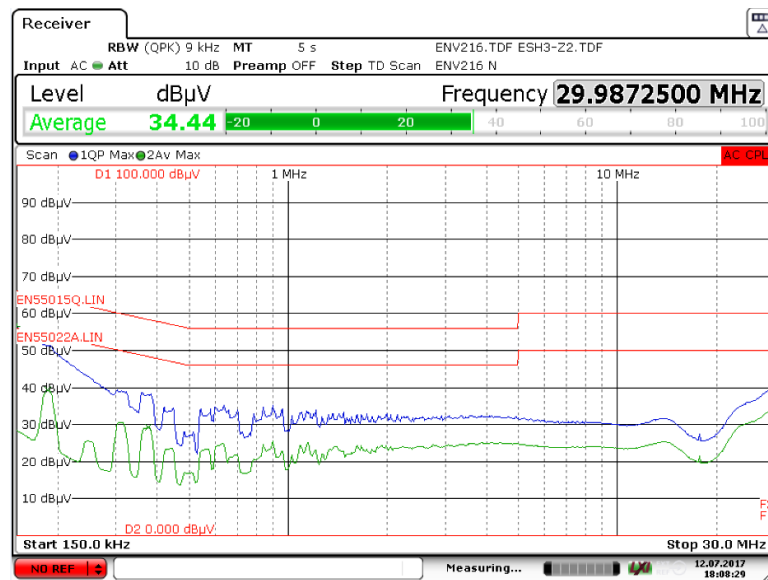


Figure 93 – Conducted EMI, 5.1 V / 6 A Load 115 VAC, 60 Hz, and EN55022 B Limits (Neutral).

13.2.2.2 Output 9 V / 3.3 A

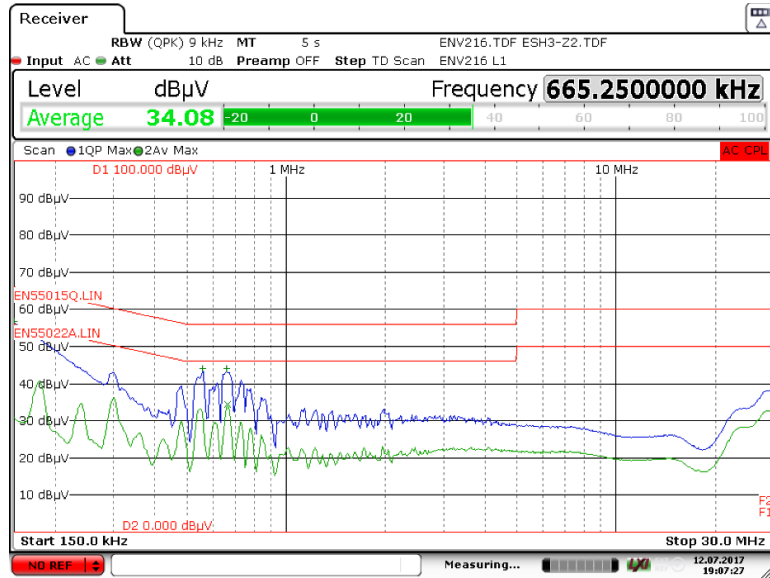


Figure 94 – Conducted EMI, 9 V / 3.3 A Load 115 VAC, 60 Hz, and EN55022 B Limits (Line).

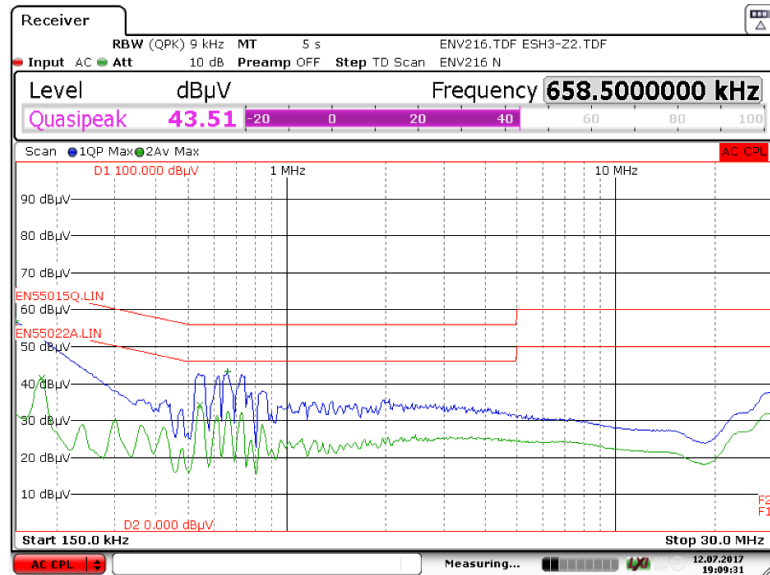


Figure 95 – Conducted EMI, 9 V / 3.3 A Load 115 VAC, 60 Hz, and EN55022 B Limits (Neutral).



13.2.2.3 Output 15 V / 2 A

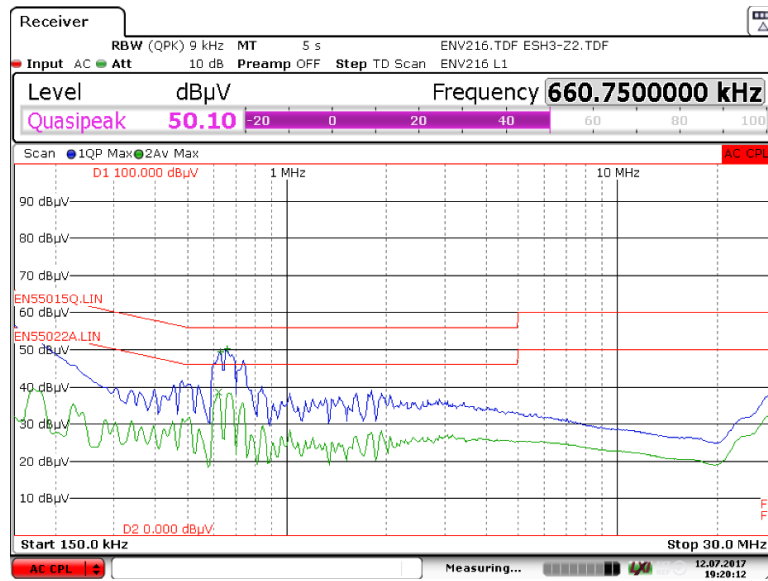


Figure 96 – Conducted EMI, 15 V / 2 A Load 115 VAC, 60 Hz, and EN55022 B Limits (Line).

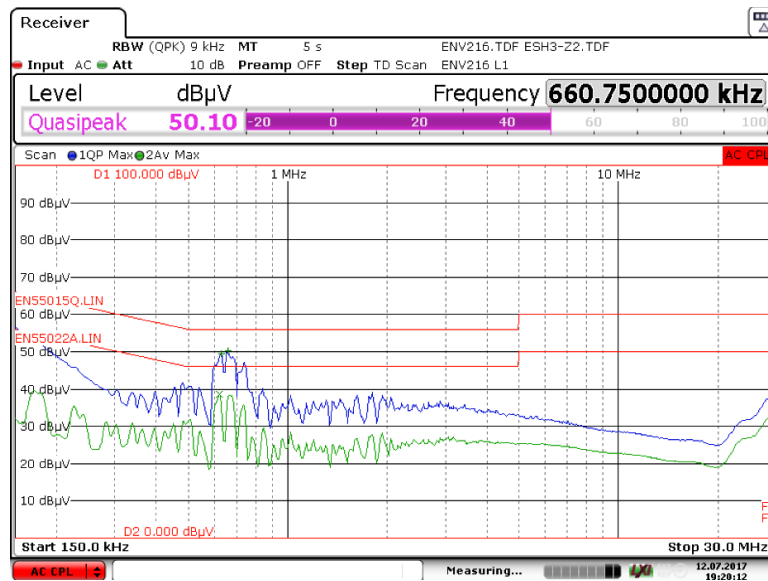


Figure 97 – Conducted EMI, 15 V / 2 A Load 115 VAC, 60 Hz, and EN55022 B Limits (Neutral).

14 Line Surge

The unit was subjected to ± 2000 V, common mode surge and ± 1000 V differential surge using 10 strikes at each condition. A test failure was defined as a non-recoverable interruption of output requiring repair or recycling of input voltage.

Surge Level (V)	Input Voltage (VAC)	Injection Location	Injection Phase (°)	Test Result (Pass/Fail)
+1000	115	L to N	0	Pass
-1000	115	L to N	0	Pass
+1000	115	L to N	90	Pass
-1000	115	L to N	90	Pass
+2000	115	L to PE	0	Pass
-2000	115	L to PE	0	Pass
+2000	115	L to PE	90	Pass
-2000	115	L to PE	90	Pass

Note: Output ground of output connected to PE.

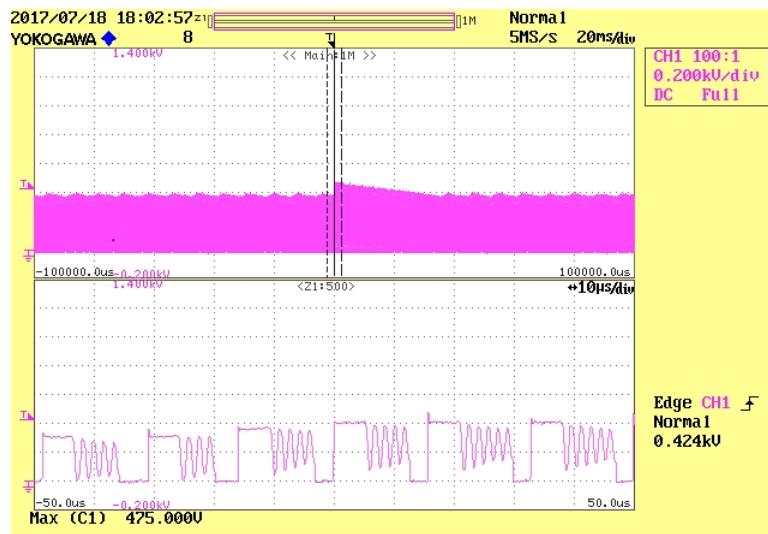


Figure 98 – U1 Drain to Source Voltage, 15 V / 2 A Load 115 VAC, 60 Hz, and Line Input Surge Test.



15 ESD Test

Passed ± 8 kV contact test.

Contact Voltage (kV)	Applied to	Number of Strikes	Test Result
8	5 V	10	PASS
-8	5 V	10	PASS
8	9 V	10	PASS
-8	9 V	10	PASS
8	15 V	10	PASS
-8	15 V	10	PASS

Passed ± 15 kV air test.

Differential Voltage (kV)	Applied to	Number of Strikes	Test Result
15	5 V	10	PASS
-15	5 V	10	PASS
15	9 V	10	PASS
-15	9 V	10	PASS
15	15 V	10	PASS
-15	15 V	10	PASS

16 Revision History

Date	Author	Revision	Description and Changes	Reviewed
12-Sep-17	IB	1.0	Initial Release	Apps & Mktg



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Power Integrations Worldwide Sales Support Locations**WORLD HEADQUARTERS**

5245 Hellyer Avenue
San Jose, CA 95138, USA.
Main: +1-408-414-9200
Customer Service:
Phone: +1-408-414-9665
Fax: +1-408-414-9765
e-mail: usasales@power.com

GERMANY

(IGBT Driver Sales)
HellwegForum 1
59469 Ense, Germany
Tel: +49-2938-64-39990
Email: igbt-driver.sales@power.com

KOREA

RM 602, 6FL
Korea City Air Terminal B/D,
159-6
Samsung-Dong, Kangnam-Gu,
Seoul, 135-728 Korea
Phone: +82-2-2016-6610
Fax: +82-2-2016-6630
e-mail: koreasales@power.com

CHINA (SHANGHAI)

Rm 2410, Charity Plaza, No. 88,
North Caoxi Road,
Shanghai, PRC 200030
Phone: +86-21-6354-6323
Fax: +86-21-6354-6325
e-mail:
chinasales@power.com

INDIA

#1, 14th Main Road
Vasanthanagar
Bangalore-560052
India
Phone: +91-80-4113-8020
Fax: +91-80-4113-8023
e-mail:
indiasales@power.com

SINGAPORE

51 Newton Road,
#19-01/05 Goldhill Plaza
Singapore, 308900
Phone: +65-6358-2160
Fax: +65-6358-2015
e-mail:
singaporesales@power.com

CHINA (SHENZHEN)

17/F, Hivac Building, No. 2, Keji
Nan 8th Road, Nanshan District,
Shenzhen, China, 518057
Phone: +86-755-8672-8689
Fax: +86-755-8672-8690
e-mail: chinasales@power.com

ITALY

Via Milanese 20, 3rd Fl.
20099 Sesto San Giovanni (MI)
Italy
Phone: +39-024-550-8701
Fax: +39-028-928-6009
e-mail: eurosales@power.com

TAIWAN

5F, No. 318, Nei Hu Rd.,
Sec. 1
Nei Hu District
Taipei 11493, Taiwan R.O.C.
Phone: +886-2-2659-4570
Fax: +886-2-2659-4550
e-mail: taiwansales@power.com

GERMANY

(AC-DC/LED Sales)
Lindwurmstrasse 114
80337, Munich
Germany
Phone: +49-895-527-39110
Fax: +49-895-527-39200
e-mail: eurosales@power.com

JAPAN

Kosei Dai-3 Building
2-12-11, Shin-Yokohama,
Kohoku-ku, Yokohama-shi,
Kanagawa 222-0033
Japan
Phone: +81-45-471-1021
Fax: +81-45-471-3717
e-mail: japansales@power.com

UK

Cambridge Semiconductor,
a Power Integrations company
Westbrook Centre, Block 5, 2nd
Floor
Milton Road
Cambridge CB4 1YG
Phone: +44 (0) 1223-446483
e-mail: eurosales@power.com

