Design Example Report

Title	*35 W Output Automotive Power Supply for 800 V Systems Using InnoSwitch™3-AQ INN3949CQ*
Specification	30 VDC – 1000 VDC Input; 15.0 V / 2.33 A Output
Application	Traction Inverter Gate and/or Emergency Power Supply
Author	Automotive Systems Engineering Department
Document Number	DER-948Q
Date	July 9, 2023
Revision	2.0

Summary and Features

- Ultra-compact design for 800 V_{DC} BEV automotive applications
- Low component count (only 66 components)[1] design with single 1700 V power switch
- Wide range start-up and operating input from 30 V_{DC} to 1000 V_{DC}[2]
- Reinforced 1000 V isolated transformer (IEC-60664-1 and IEC-60664-4 compliant)
- ≥85 % full load efficiency across input voltage range[3]
- Secondary-side regulated output
- Ambient operating temperature from -40 °C to 85 °C
- Fully fault protected including output current limit and short-circuit protection
- Uses automotive qualified AEC-Q surface mount (SMD) components[4]
- Low profile, 15 mm height

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[1] Excluding input and output terminal blocks.
[2] Output current rating derated to 1000 mA at 60 V and 500 mA at 30 V input.
[3] 83.7% minimum full load efficiency across input voltage range at -40 °C ambient temperature.
[4] AEC-Q200 transformer and input common mode choke qualification belongs to final design.

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Disclaimer:

1 Introduction

This engineering report describes a 35 W single output automotive power supply. It is intended for use in 800 V battery system electric vehicles supporting an ultra-wide input range of 30 V_{DC} to 1000 V_{DC}. This design uses the 1700 V rated INN3949CQ from the InnoSwitch3-AQ family of ICs in a flyback converter configuration.

The design provides reinforced isolation between the primary (high-voltage input) and secondary (output) sides by observing the creepage and clearance requirements as indicated in IEC-60664 parts 1 and 4.

The report contains the power supply specification, schematic diagram, printed circuit board (PCB) layout, bill of materials (BOM), magnetics specifications, and performance data.

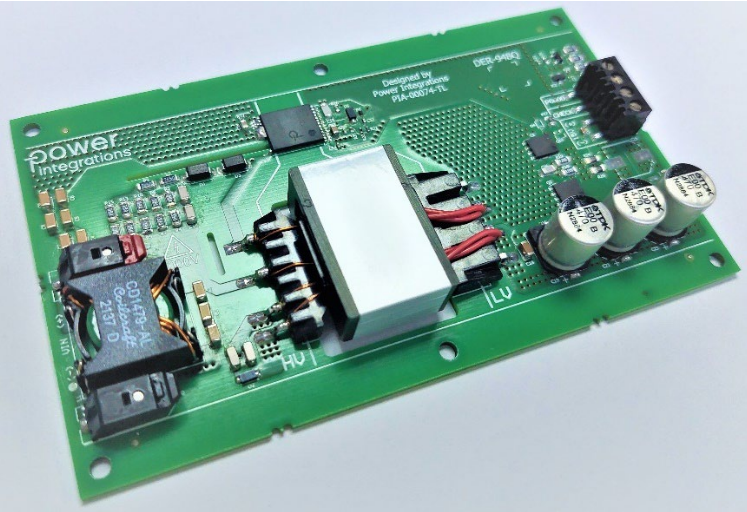

Figure 1 – Populated Circuit Board, Entire Assembly.

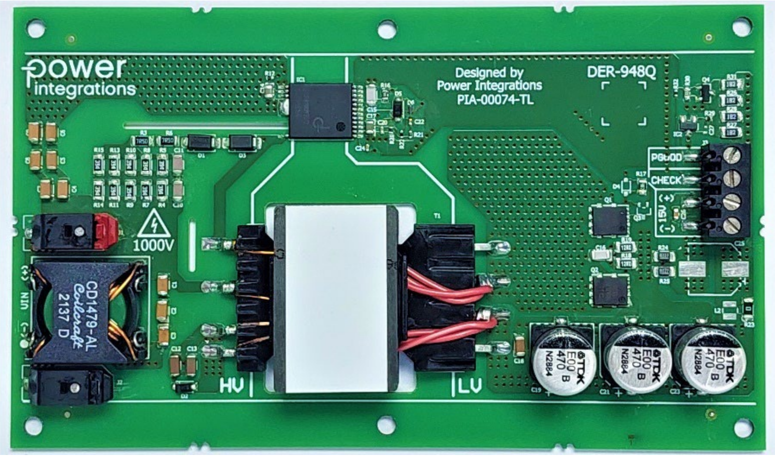

Figure 2 – Populated Circuit Board, Top.

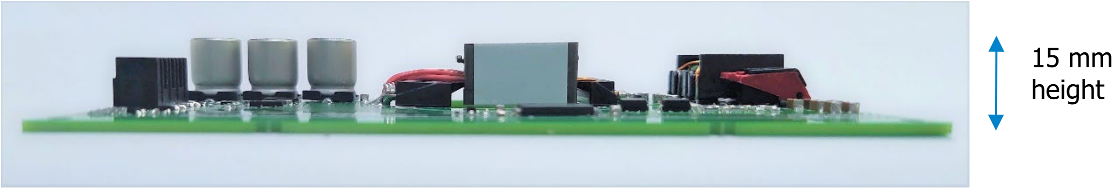

Figure 3 – Populated Circuit Board Photograph, Side.

The design can deliver the full 35 W output power at 85 °C ambient temperature from 80 V_{DC} to 1000 V_{DC} input voltage range. It is derated to 15 W with 60 V input and 7.5 W with 30 V input at 85 °C ambient temperature. The 15 V output is typically configured to provide a redundant supply should the vehicle 12 V system supplying the traction inverter fail. This is a common requirement to meet functional safety by continuously allowing the inverter to provide active short-circuit, active discharge and reporting functions.

The InnoSwitch3-AQ IC maintains necessary regulation by directly sensing the output voltage and providing fast, accurate feedback to the primary-side via FluxLink^{TM}. Secondary-side control also enables the use of synchronous rectification improving the overall efficiency compared to diode rectification thus saving cost and space by eliminating heat sinking.

2 Design Specification

The following tables below represent the minimum acceptable performance of the design. Actual performance is listed in the results section.

2.1 *Electrical Specifications*

Description	Symbol	Min.	Typ.	Max.	Units
Input Parameters					
Positive DC Link Input Voltage Referenced to HV-	**HV**	30	800	1000	V_{DC}
Operating Switching Frequency	**f_{SW}**	25		55.5	kHz
Output Parameters					
Output Voltage Parameters					
Regulated Output Voltage	**V_{OUT}**	14.25	15.0	15.75	V_{DC}
Output Voltage Load and Line Regulation	**V_{REG}**	-5		+5	%
Ripple Voltage Measured on Board	**V_{RIPPLE}**		500		mV
Output Current Parameters					
Output Current	**I_{OUT}**		2333		mA
Output Power Parameters	**P_{OUT}**				W
Continuous Output Power at:					
80 V_{DC} – 1000 V_{DC} Input				35	
60 V_{DC} Input				15	
30 V_{DC} Input				7.5	
Output Overshoot and Undershoot During Dynamic Load Condition	**ΔV_{OUT}**		5		%

Table 1 – Electrical Specifications.

2.2 *Isolation Coordination*

Description	Symbol	Min.	Typ.	Max.	Units
Maximum Blocking Voltage of INN3949CQ	BV_{DSS}			1700	V
System Voltage	V_{SYSTEM}			1202	V
Working Voltage	$V_{WORKING}$			1000	V
Pollution Degree	**PD**			2	
CTI for FR4	**CTI**	175		399	
Rated Impulse Voltage	$V_{IMPULSE}$			2.5	kV
Altitude Correction Factor for h_a	c_{ha}			1.59	
Technical Cleanliness Requirement				0.0	mm
Basic Clearance Distance Requirement	CLR_{BASIC}	2.4			mm
Reinforced Clearance Distance Requirement	$CLR_{REINFORCED}$	4.8			mm
Basic Creepage Distance Requirement for PCB	$CPG_{BASIC(PCB)}$	5.0			mm
Reinforced Creepage Distance Requirement for PCB	$CPG_{REINFORCED(PCB)}$	10.0			mm
Isolation Test Voltage Between Primary and Secondary-Side for 60s	V_{ISO}	5000			V_{PK}
Partial Discharge Test Voltage	V_{PD_TEST}	1803			V_{PK}

Table 2 – Isolation Coordination[5].

2.3 *Environmental Specifications*

Description	Symbol	Min.	Typ.	Max.	Units
Ambient Temperature	Ta	-40		85	°C
Altitude of Operation	ha			5500	m
Relative Humidity	Rh			85	%

Table 3 – Environmental Specifications.

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[5] Clearance and creepage distances are derived from IEC 60664-1 and IEC 60664-4.

3 Schematic

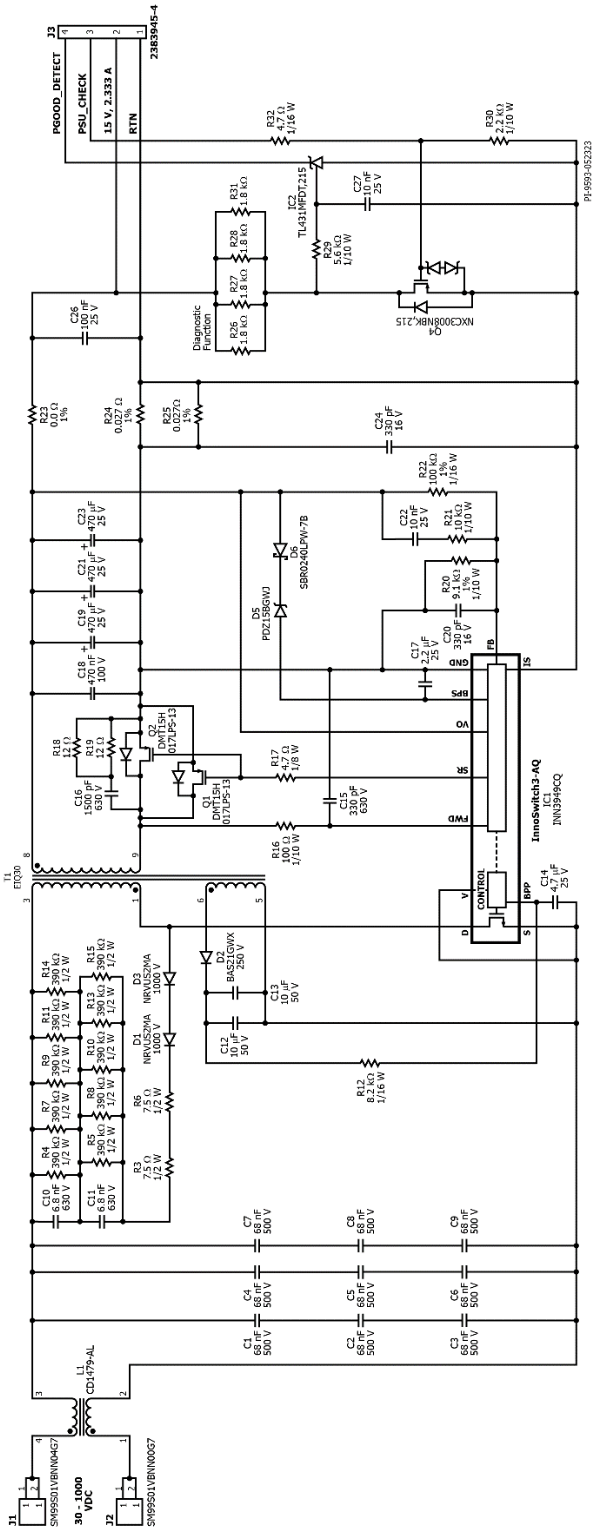

Figure 4 – DER-948Q Schematic.

4 Circuit Description

4.1 *Input Filter*

The automotive inverter environment is harsh, characterized by high dv/dt and di/dt from the switching action of the power modules. Large common mode currents are generated across the isolation barrier of the power supply which can interfere with the power supply operation, other inverter blocks and signal measurement integrity. The input common mode choke L1 together with the bypass capacitors C1 to C9 helps filter unwanted noise as prevention from affecting the overall performance of the design.

Common mode inductor L1 was selected such that the reference board would be able to withstand the Power Integrations' internal "Resistance to ripple on high voltage network" test. The test injects high frequency ripple on the high-voltage input to simulate the actual DC link capacitor ripple in a traction inverter. The final value of L1 will depend on the final design or application requirement. The higher the noise, the higher the inductance of L1 should be. However, consideration should be given between inductance value and the DC resistance (DCR) which has an impact on the overall efficiency of the design.

Bypass capacitors C1 to C9 were selected so as not to exceed 65% of their voltage rating as well as to maintain enough pad-to-pad distance to meet creepage and clearance requirements.

4.2 *High-Voltage Side Circuit*

The circuit design uses a flyback converter topology to provide an isolated low-voltage output from the high-voltage input. The flyback transformer T1 primary winding is connected across the high-voltage DC input and the drain terminal of the 1700 V SiC power MOSFET switch internal to INN3949CQ IC1.

An RCD type snubber circuit is placed across the primary side winding, to clip the drain-source voltage peaking of the internal SiC MOSFET switch during turn-off instance. Two super-fast (or better), surface mount type, AEC-Q qualified diodes D1 and D3 were placed in series to meet creepage and clearance requirements and ensure that the voltage across the diodes would not exceed 70% rating. Capacitors C10 and C11 catches the energy from the leakage inductance of transformer T1, the capacitor values were selected to minimize the voltage ripple across the snubber resistor network and maintain near constant power dissipation throughout the switching period. Resistors R4, R5, R7, R8, R9, R10, R11, R13, R14 and R15 dissipate the energy stored inside the snubber capacitors, the resistor values were selected such that their average voltage will not exceed 80% rating and maintain below 50% power dissipation. Cooling area for the snubber resistors were also considered to ensure operating temperature would be at acceptable level.

IC1 is self-starting, using an internal high-voltage current source to charge BPP capacitor C14. INN3949CQ is guaranteed to start-up at 30 V but will typically start below this level.

Transformer T1 auxiliary winding powers up the primary-side block during normal operation, this minimizes the power derived from the internal high-voltage current source to optimize the overall converter efficiency and lessens heating inside IC1. The output of the auxiliary winding is rectified and DC filtered using diode D2 and capacitors C12 and C13. The DC filtered voltage is fed to the BPP pin through resistor R12, where the resistor value is chosen to allow enough current for normal switching operation of IC1.

In this design, the input under and overvoltage features were disabled by shorting the V pin to SOURCE pin. This approach does not require the voltage sensing resistor chain for setting the under or overvoltage trigger of IC1 thus saving cost and space however, output voltage regulation at high load may fail at voltages < 80 V_{DC}.[6] If the output voltage fails to reach 90% regulation within 60 ms ($t_{SS(RAMP)}$ + $t_{FB(AR)}$) during start-up, the auto-restart fault is triggered followed by a 2 s off time. This will result in a power supply hiccup where the output rises but fails to reach regulation.

If hiccup is not acceptable on the target design or application, then the undervoltage feature can be implemented. Please refer to the data sheet for the recommended undervoltage lockout circuit and design guide.

4.3 *Low-Voltage Side Circuit*

The secondary side of the INN3949CQ provides output voltage sensing, output current sensing and gate drive for the MOSFET providing synchronous rectification (SR). The voltage across the secondary winding of the transformer T1 is rectified by the synchronous rectifier MOSFETs Q1 and Q2 then DC filtered by capacitors C18, C19, C21 and C23. High frequency ringing during switching is reduced by the RC type snubber formed by resistors R18, R19 and capacitor C16.

Switching of Q1 and Q2 is controlled by the secondary-side controller inside IC1. Control timing is based on the negative edge voltage transition sensed from the FWD pin via resistor R16. Capacitor C10 and R16 form a low pass filter that reduces voltage spike seen by the FWD pin and ensure that the maximum rating of 150 V will not be exceeded.

In continuous conduction mode operation, the primary-side power MOSFET is turned off just prior to the secondary-side controller commanding a new switching cycle from the primary. In discontinuous mode the SR MOSFET is turned off when the voltage drop across it falls below a certain threshold of approximately $V_{SR(TH)}$. Secondary-side control of the primary-side power MOSFET avoids any possibility of cross conduction of the two switches and ensures reliable synchronous rectifier operation.

The secondary side of the IC is self-powered from either the secondary winding forward voltage (thru R16 and the FWD pin) or by the output voltage (thru the VOUT pin). In both cases, energy is used to charge the decoupling capacitor C17 via an internal regulator.

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[6] Output current is derated at voltages less than 80 V.

Resistors R22 and R20 form a voltage divider network that senses the output voltage. The INN3949CQ IC has an FB pin internal reference of 1.265 V. Capacitor C20 provides decoupling from high frequency noise affecting power supply operation. Capacitor C22 and R21 form a feedforward network to speed up the feedback response time and lower the output ripple.

Output current is sensed by monitoring the voltage drop across parallel configured resistors R24 and R25. The resulting current measurement is filtered with decoupling capacitor C12 and monitored across the IS and SECONDARY GROUND pins. An internal current sense threshold of around 35 mV is used to reduce losses. Once the threshold is exceeded, the INN3949CQ IC1 will adjust the number of pulses to maintain fixed current limit. The IC will enter auto-restart (AR) operation when the output voltage feedback is below 90% and will recover when the load current is reduced below threshold.

4.4 *Diagnostic Circuit*

As the power supply unit will be used as an emergency backup, it is mainly kept unloaded but must be ready to be used anytime. A diagnostic circuit is provided as a way for the system to perform self-test to check if it is functional or not.

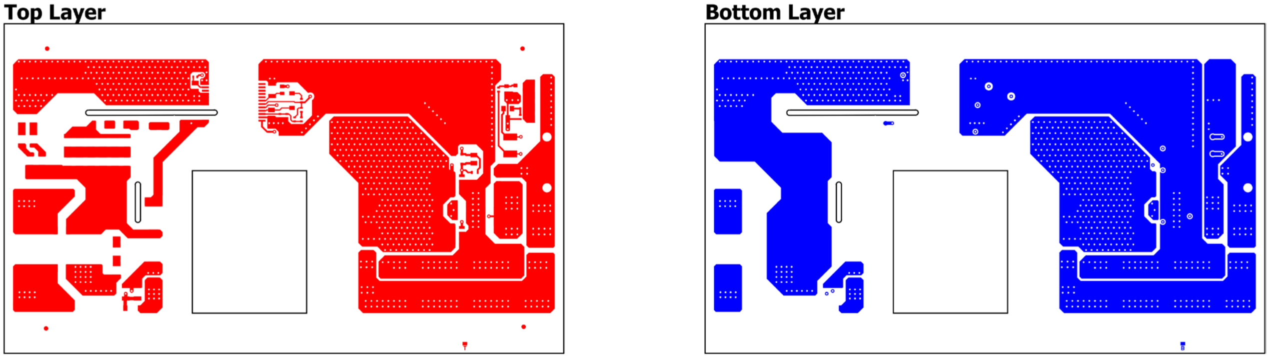
An additional interface for diagnostic checking was added, namely: PGOOD_DETECT and PSU_CHECK.

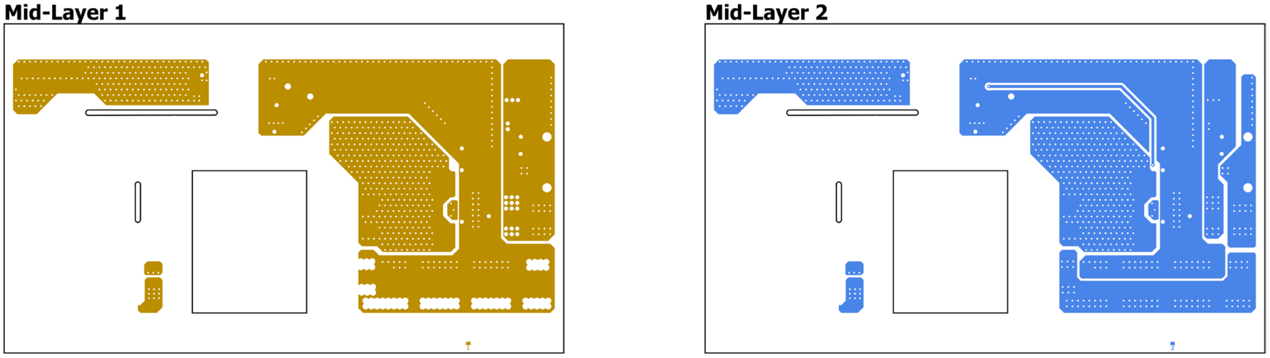
PSU_CHECK is an input signal (3.3 V to 5 V, maximum of 8 V) from the system's microcontroller, used to query if the unit is functional. When PSU_CHECK is HIGH, Q4 is turned ON via resistors R32 and R30, Q4 conducts and TL431 IC2's REF pin is pulled low. A maximum of 0.5 W is loaded to the output via the parallel resistors R26, R27, R28 and R31. When PSU_CHECK is LOW, IC2's REF pin is pulled HIGH to 15.0 V output voltage. R29 and C21 filter the signal to IC2's REF pin.

PGOOD_DETECT is an open collector output which must be pulled up externally (maximum of 36 V). When IC2's REF pin is pulled HIGH, PGOOD_DETECT is pulled low to approximately 2 V. A pull up resistor should be selected to provide at least 1 mA. When the IC2's REF pin is pulled LOW, IC2 does not conduct and PGOOD_DETECT is pulled up to the external voltage provided. In summary, a PGOOD_DETECT LOW signal indicates that the unit is functional and ready to use while a HIGH signal indicates that the unit is not serviceable.

5 PCB Layout

Layers:	Six (6) (typical for traction inverter control board)
Board Material:	FR4
Board Thickness:	1.6 mm
Copper Weight:	2 oz


Top Layer
Bottom Layer


Mid-Layer 1
Mid-Layer 2

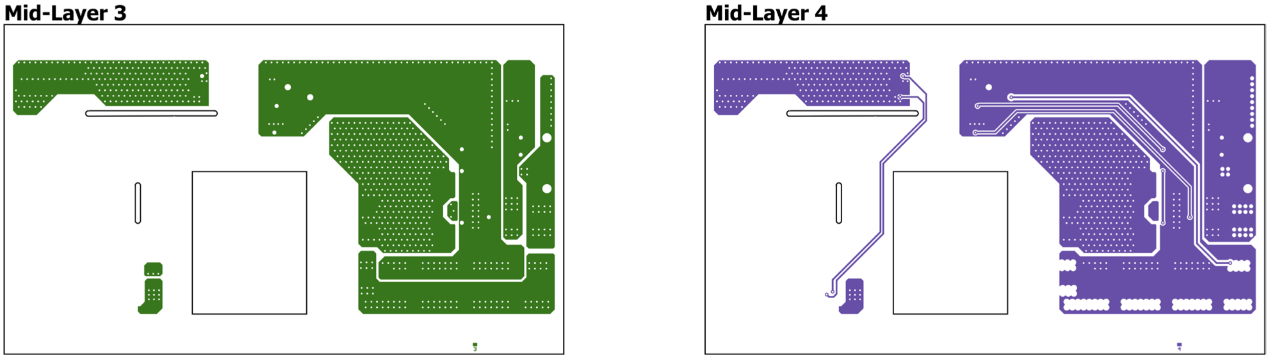

Mid-Layer 3
Mid-Layer 4

Figure 5 – DER-948Q PCB Layout.

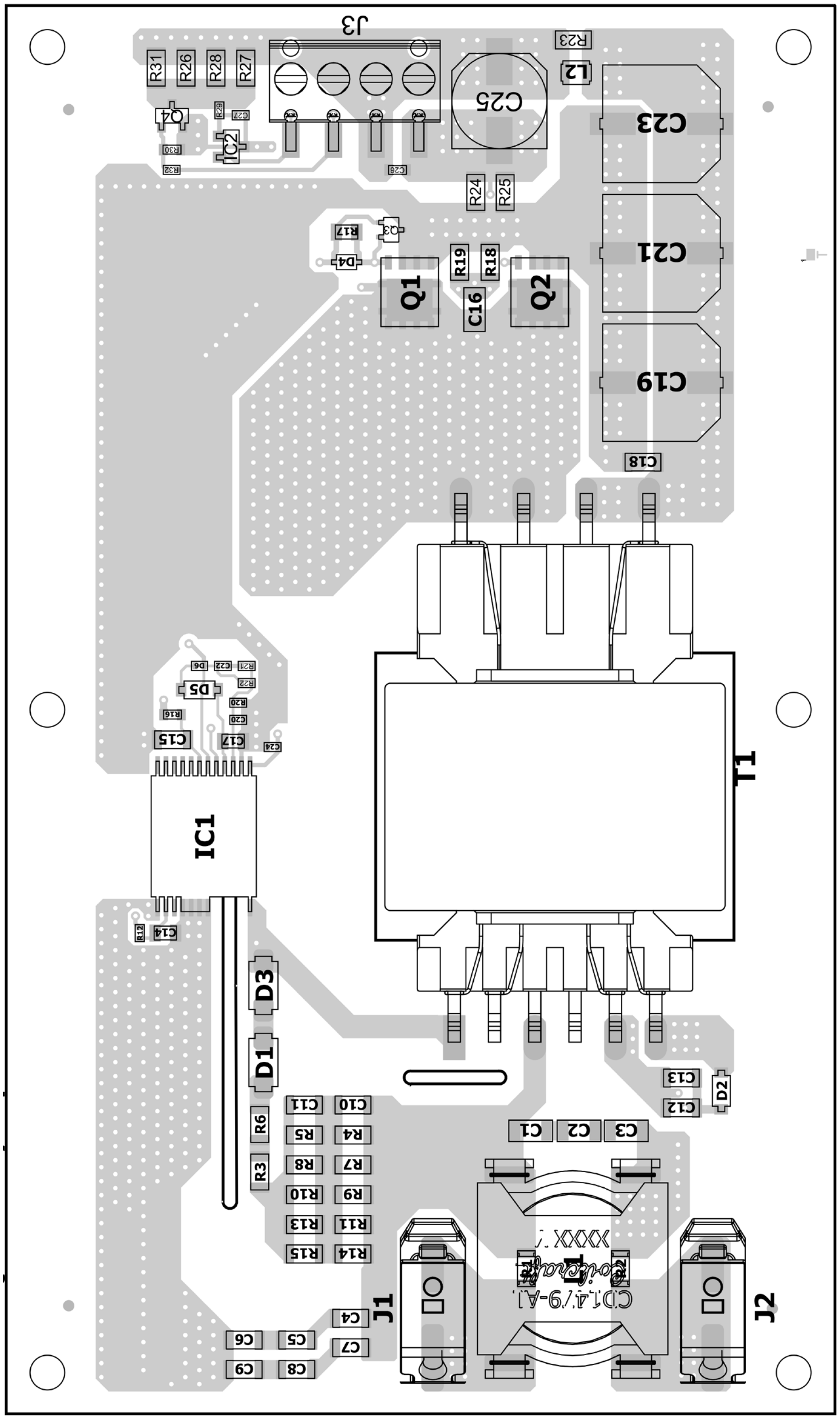


Figure 6 – DER-948Q PCB Assembly (Top).

6 Bill of Materials

Item	Qty	Designator	Description	MFR Part Number	Manufacturer
1	9	C1, C2, C3, C4, C5, C6, C7, C8, C9	Multilayer Ceramic Capacitors MLCC - SMD/SMT 68n X7R 500 V 10%1206 AEC-Q200	C1206C683KCRACAUTO	KEMET
2	2	C10, C11	Multilayer Ceramic Capacitors MLCC - SMD/SMT 6n8 C0G 630 V 5%1206 AEC-Q200	CGA5H4C0G2J682J115AE	TDK
3	2	C12, C13	Multilayer Ceramic Capacitors MLCC - SMD/SMT 10u X7R 50 V 10%1206 AEC-Q200	CGA5L1X7R1H106K160AE	TDK
4	1	C14	Multilayer Ceramic Capacitors MLCC - SMD/SMT 4u7 X7R 25 V 20%805 AEC-Q200	CGA4J1X7R1E475M125AC	TDK
5	1	C15	Multilayer Ceramic Capacitors MLCC - SMD/SMT 330p C0G 630 V 5%1206 AEC-Q200	CGA5C4C0G2J331J060AA	TDK
6	1	C16	Multilayer Ceramic Capacitors MLCC - SMD/SMT 1500p C0G 630 V 5%1206 AEC-Q200	CGA5H4C0G2J152J115AA	TDK
7	1	C17	Multilayer Ceramic Capacitors MLCC - SMD/SMT 2u2 X7R 25V 10%805 AEC-Q200	C0805C225K3RACAUTO	KEMET
8	1	C18	Multilayer Ceramic Capacitors MLCC - SMD/SMT 470n X7R 100 V 10%1206 AEC-Q200	HMK316B7474KLHT	Taiyo Yuden
9	3	C19, C21, C23	Polymer Aluminum Capacitor 470u AL 25V 20%10x12.5mm AEC-Q200	B40900B5477M000	TDK
10	2	C20, C24	Multilayer Ceramic Capacitors MLCC - SMD/SMT 330p X7R 16 V 10%402 AEC-Q200	VJ0402Y331KLJAJ32	Vishay
11	2	C22, C27	Multilayer Ceramic Capacitors MLCC - SMD/SMT 10n X7R 25 V 10%402 AEC-Q200	CGA2B2X7R1E103K050BA	TDK
12	1	C26	Multilayer Ceramic Capacitors MLCC - SMD/SMT 100n X7R 25 V 10%603 AEC-Q200	CGA3E2X7R1E104K080AA	TDK
13	2	D1, D3	Diode Standard 1000 V 1.5A SMT DO-214AC AEC-Q101	NRVUS2MA	On Semi
14	1	D2	Diode Standard 200 V 225mA SMT SOD-123 AEC-Q101	BAS21GWX	Nexperia
15	1	D5	Diode Zener 15 V 365 mW SMT SOD-123 AEC-Q101	PDZ15BGWJ	Nexperia
16	1	D6	Diode Standard 40 V 200mA SMT X1-DFN1006-2 AEC-Q	SBR0240LPW-7B	Diodes, Inc.
17	1	IC1	CV/CC QR Flyback Switcher IC with Integrated 1700 V Switch and FluxLink Feedback for Automotive Applications	INN3949CQ	Power Integrations
18	1	IC2	Voltage References 2.495 VIN ADJ Shunt AEC-Q100	TL431MFDT,215	Nexperia
19	1	J1	TERM BLOCK 1POS SIDE ENTRY SMD RED	SM99S01VBNN04G7	METZ CONNECT
20	1	J2	TERM BLOCK 1POS SIDE ENTRY SMD BLACK	SM99S01VBNN00G7	METZ CONNECT
21	1	J3	TERMI-BLOCK SMD MOUNT 180_4P_3.81	2383945-4	TE Connectivity
22	1	L1	Input Common Mode Choke	CD1479-AL	Coilcraft
23	1	Q1, Q2	N-Channel MOSFET: 150 V 9.4 A PowerDI5060-8	DMT15H017LPS-13[7]	Diodes, Inc.

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[7] DMT15H017LPS-13 is qualified for AEC-Q101 reliability test only but not fully qualified for all AEC-Q criteria.

24	1	Q3	N-Channel MOSFET: 30 V 400 mA SOT-23	NX3008NBK,215	Nexperia
25	2	R3, R6	Thick Film Resistors - SMD 1206 7R5 5% 0.5W 200 V AEC-Q200	ESR18EZPJ7R5	ROHM Semi
26	10	R4, R5, R7, R8, R9, R10, R11, R13, R14, R15	Thick Film Resistors - SMD 1206 390K 5% 0.5W 200 V AEC-Q200	ESR18EZPJ394	ROHM Semi
27	1	R12	Thick Film Resistors - SMD 0402 8K2 5% 0.0625W 50 V AEC-Q200	CR0402AJW-822GLF	Bourns
28	1	R16	Thick Film Resistors - SMD 0603 100R 5% 0.1W AEC-Q200	RMCF0603JT100R	Stackpole
29	1	R17	Thick Film Resistors - SMD 0805 4R7 5% 0.125W 150 V AEC-Q200	AC0805JR-074R7L	YAGEO
30	2	R18, R19	Thick Film Resistors - SMD 1206 12R 5% 0.25W 200 V AEC-Q200	AC1206JR-0712RL	YAGEO
31	1	R20	Thick Film Resistors - SMD 0402 9K1 1% 0.1W 50 V AEC-Q200	ERJ-2RKF9101X	Panasonic
32	1	R21	Thick Film Resistors - SMD 0402 10K 5% 0.1W 50 V AEC-Q200	ERJ-U02J103X	Panasonic
33	1	R22	Thick Film Resistors - SMD 0402 100K 1% 0.0625W AEC-Q200	RMCF0402FT100K	Stackpole
34	1	R23	Thick Film Resistors - SMD 1206 0R 1% 0.25W 200 V AEC-Q200	AF1206JR-070RL	YAGEO
35	2	R24, R25	Thick Film Resistors - SMD 1206 0R027 1% 0.25W AEC-Q200	WSL1206R0270FEA	Vishay
36	4	R26, R27, R28, R31	Thick Film Resistors - SMD 1206 1K8 5% 0.25W AEC-Q200	ERJ-8GEYJ182V	Panasonic
37	1	R29	Thick Film Resistors - SMD 0402 5K6 5% 0.1W 50V AEC-Q200	ERJ-2GEJ562X	Panasonic
38	1	R30	Thick Film Resistors - SMD 0603 2K2 5% 0.1W 75V AEC-Q200	AC0603JR-072K2L	YAGEO
39	1	R32	Thick Film Resistors - SMD 0402 4R7 5% 0.063W 50V AEC-Q200	AC0402JR-074R7L	YAGEO
40	1	T1	35 W Power Transformer	EFD25	Power Integrations
41	1	T1-Core	3C96 Ferrite Core	EQ30 – 3C96	Ferroxcube
42	1	T1-Core	3C96 Ferrite Core	PLT30/20/3 – 3C96	Ferroxcube
43	1	T1-Bobbin	Customized bobbin	MCT-EIQ3001 V4+6P	Power Integrations
44	1	Z1	Printed circuit board	PIA-00074-TL	Power Integrations

Table 4 – DER-948Q Bill of Materials[8].

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[8] All components are AEC-Q qualified except connectors, T1 and L1.

7 Transformer Specification (T1)

7.1 *Electrical Diagram*

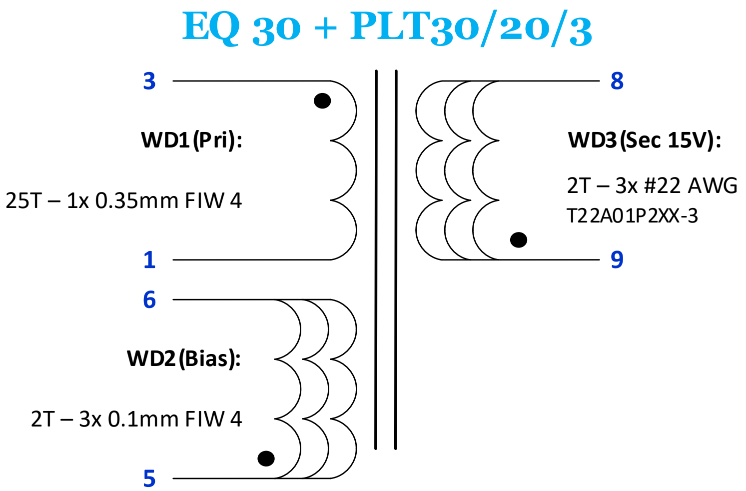


Figure 7 – Transformer Electrical Diagram.

7.2 *Electrical Specifications*

Parameter	Conditions	Min.	Typ.	Max.	Unit
Power	Output power secondary-side			35	W
Input voltage Vdc	Flyback topology	30	800	1000	V
Switching frequency	Flyback topology			55.5	kHz
Duty cycle	Flyback topology	3.8		52.8	%
Np:Ns			12.5		
Rdc	Primary side		240		mΩ
Rdc	Secondary side		2.8		mΩ
Coupling capacitance	Primary-side to secondary-side Measured at 1 V_{PK-PK}, 100 kHz frequency, with pins 1-3 shorted, pins 5-6 shorted and pins 8-9 shorted at 25 °C			21.39	pF
Primary inductance	Measured at 1 V_{PK-PK}, 100 kHz frequency, between pin 1-3, with all other windings open at 25 °C		422.6		µH
Part to part tolerance	Tolerance of Primary Inductance	-3.0		3.0	%
Primary leakage inductance	Measured between pin 1 to pin 3, with all other windings shorted.			6.5	µH

Table 5 – Transformer (T1) Electrical Specifications.

7.3 *Transformer Build Diagram*

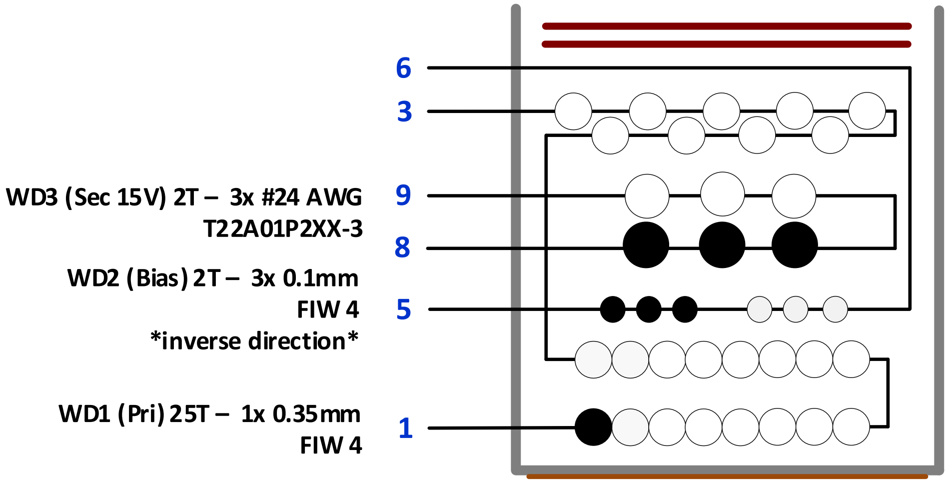


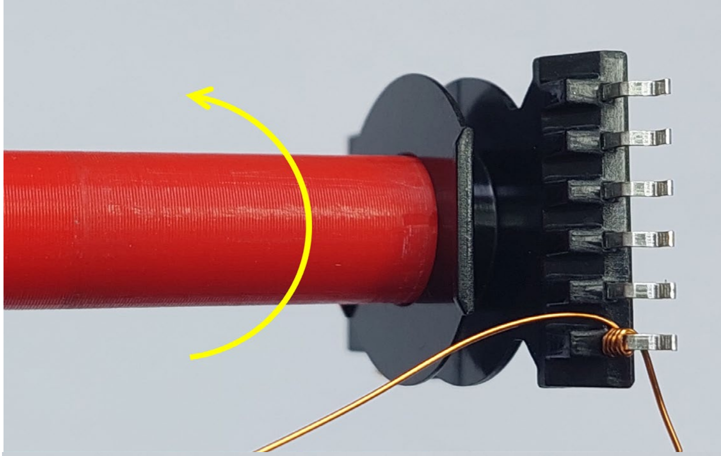
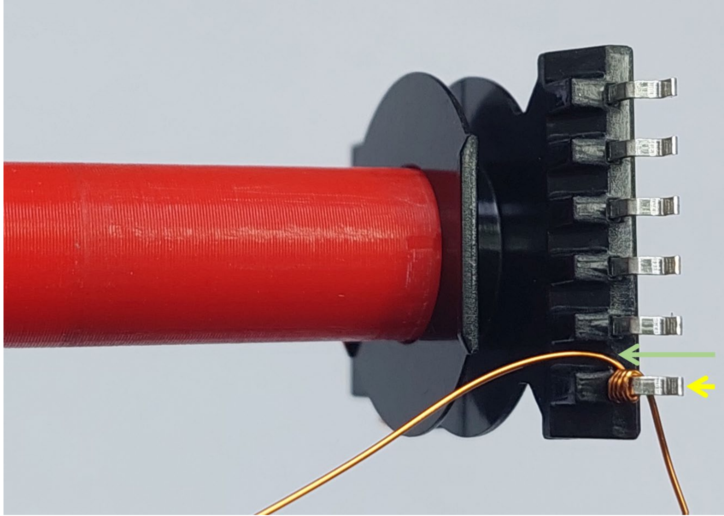
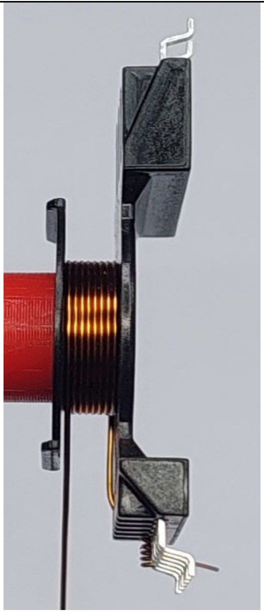
Figure 8 – Transformer Build Diagram.

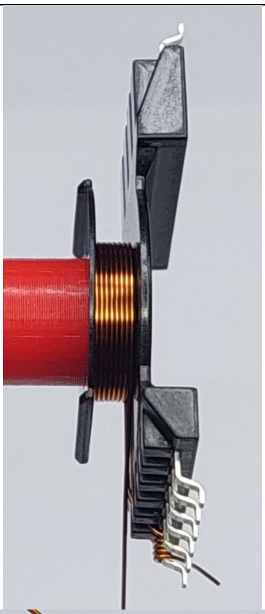
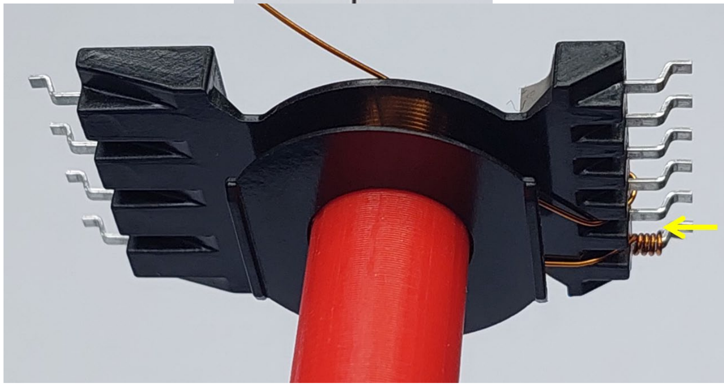
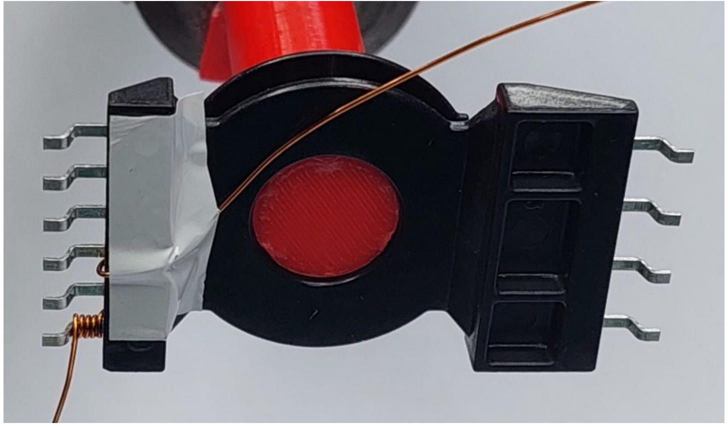
7.4 *Material List*

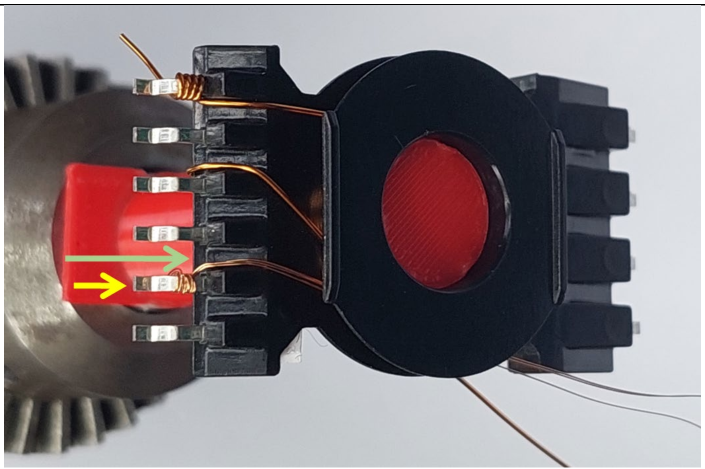
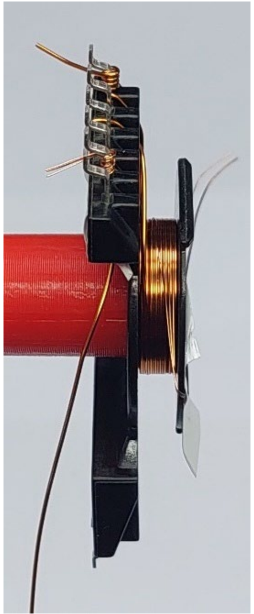
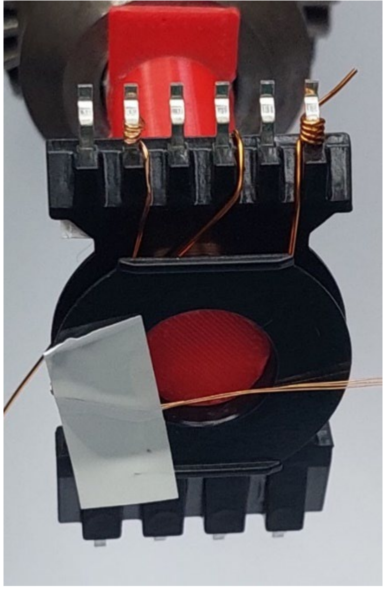
Item	Description	Qty	UOM	Material	Manufacturer
[1]	Bobbin: MCT-EIQ3001 V4+6P	1	PC	Phenolic	MyCoilTech
[2]	Core: EQ30	1	PC	3C96 (or equivalent)	Ferroxcube
[3]	Core: PLT30/20/3	1	PC	3C96 (or equivalent)	Ferroxcube
[4]	WD1 (Pri): 0.35 mm FIW 4, Class F		mm	Copper Wire	Elektrisola
[5]	WD2 (Bias): 0.1 mm FIW 4, Class F		mm		Elektrisola
[6]	WD3a (Sec): T22A01P2XX-3, AWG 22 PFA.003”		mm		Rubadue
[7]	Polyimide Amber: 0.125 in (3.18 mm)		mm	315-CQT1-0.125	Chip Quik Inc.

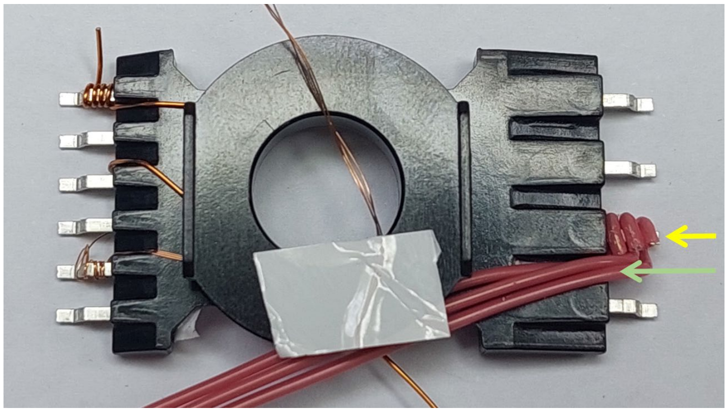
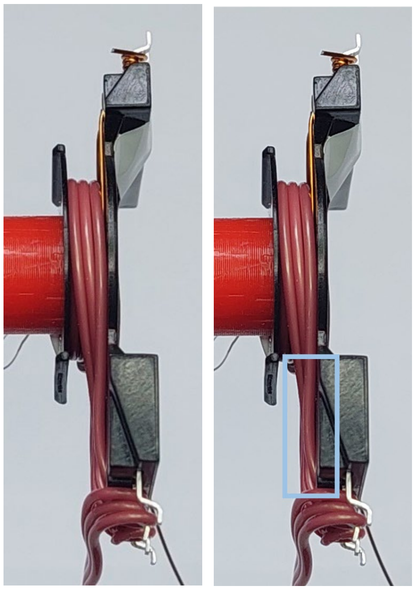
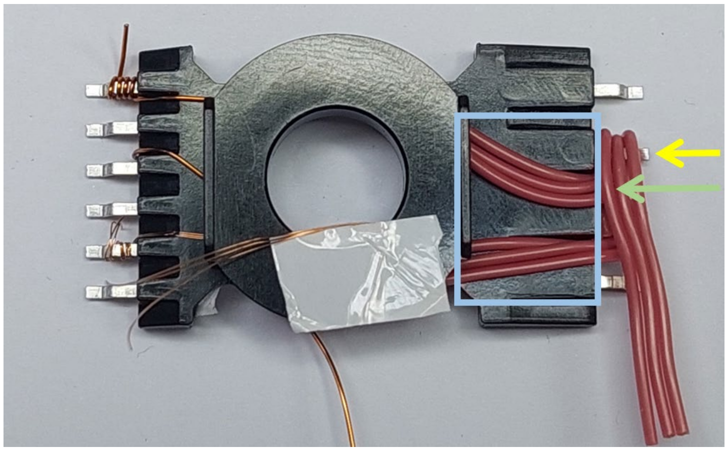
Table 6 – Transformer (T1) Material List.

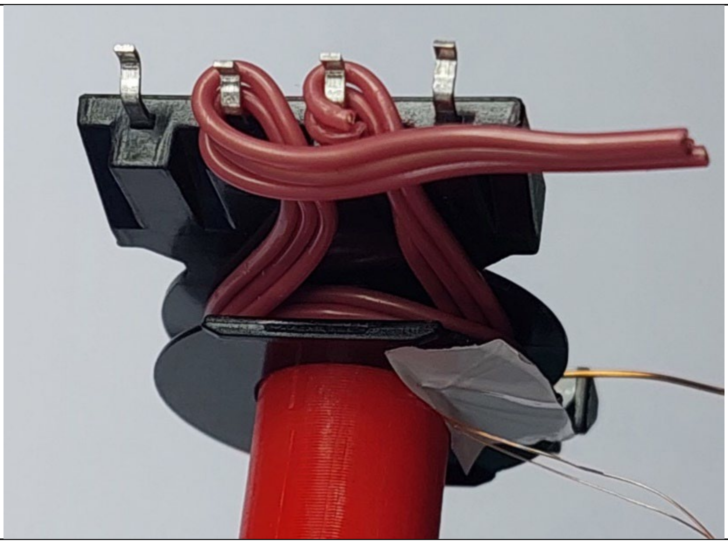
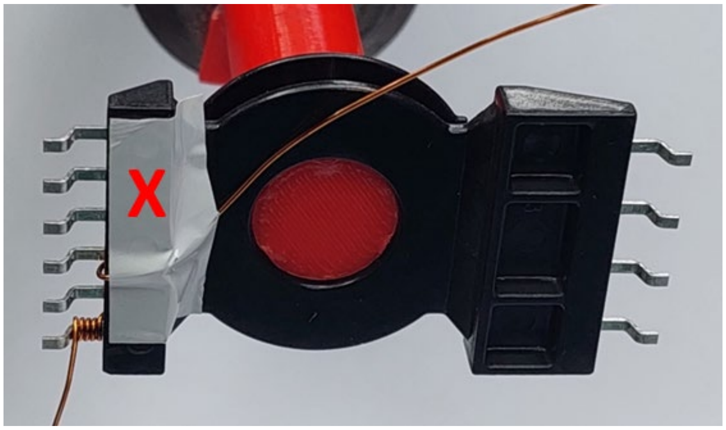
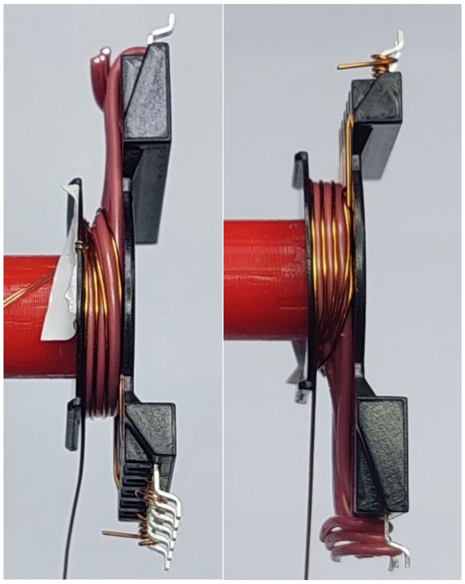
7.5 *Winding Instructions*

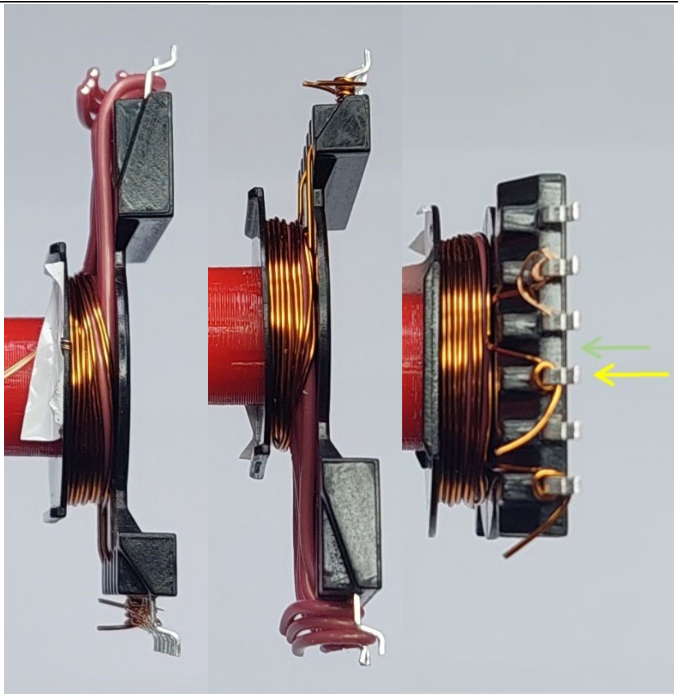
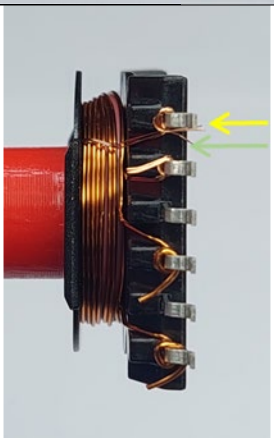
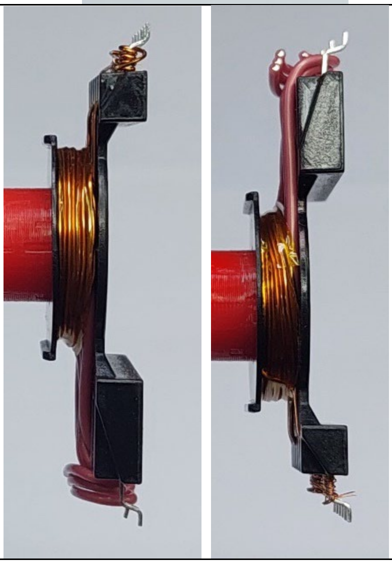
WD1: Primary	 	Position the bobbin on the mandrel such that the bobbin pins are on the right side. Refer to the arrow for the winding direction. Using .35 mm FIW4, route the start lead from 1st pin(yellow) going to the 2nd lead guide(green) of the bobbin.
WD1: Primary		Wind the primary winding's first layer, 8 turns from right to left with tight tension. Spread the winding evenly along the bobbin's width.

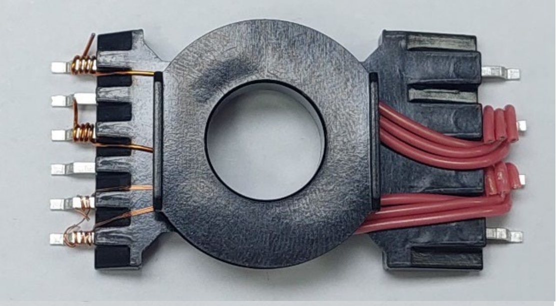
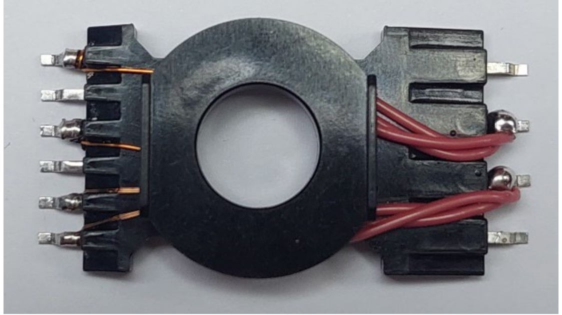
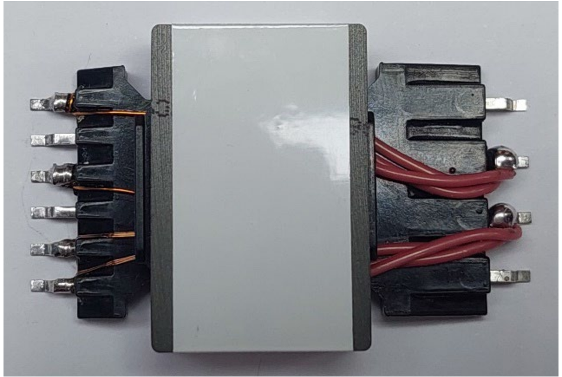
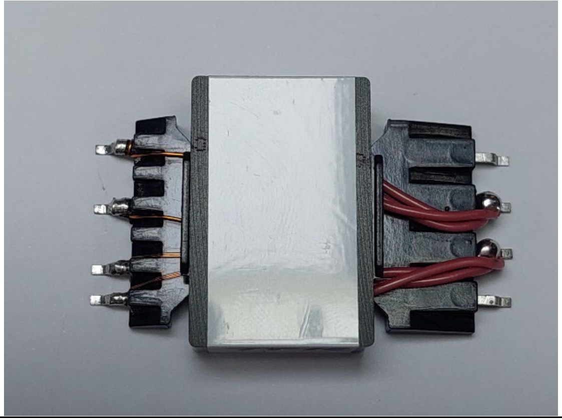
	  	Wind the primary winding's second layer, 8 turns from left to right with tight tension. Spread the winding evenly along the bobbin's width. Temporarily route the primary winding to the 3rd lead guide and attach it to the bottom of the bobbin using tape.

WD2: Bias	  	Flip the bobbin, such that the pins are on the left side, to invert the winding. Using 3x .1 mm FIW4, route the start lead from 5th pin(yellow) going to the 5th lead guide(green) of the bobbin. Wind the bias winding, 2 turns from left to right with tight tension. Spread the winding evenly along the bobbin's width. Try to fit in the bias winding wires between the spaces of the primary winding. The previous layer of primary winding has 8 turns, giving 7 spaces available for the bias winding. Temporarily attach the bias winding wires on the top of the bobbin using tape.

WD3: 15V		Using 3xAWG 22 PFA .003” Triple Insulated Wire, route the start lead from 8th pin(yellow) going to the 9th lead guide(green) of the bobbin.
		Wind all wires together with tight tension, 2 turns with 1 turn per layer. For the portion inside the blue box, lay it flat on the surface of the bobbin in preparation for the next layer of the primary.
		Terminate the secondary winding at the 9th pin(yellow) thru the 10th lead (green) guide,

		
WD1: Primary	 	This is the continuation of the primary winding. Remove the tape that attaches the primary winding at the bottom of the bobbin. Wind 4 turns of the primary in the spaces between the secondary windings

		Wind another 5 turns of the primary in the remaining space to complete 9 turns of the primary's 3rd layer. Terminate the primary winding at the 3rd pin (yellow) through the 4th lead guide (green).
WD2: Bias		Terminate the bias winding at the 6th pin (yellow) through the 6th lead guide (green).
Finishing		Place 2 layers of tape to hold the winding in place.

	   	Cut and solder the wires. Mount the gapped core using glue (a 16 mm polymer tape can be used as alternative Remove Pins 2 and 4

8 Transformer Design Spreadsheet

1	**DCDC_InnoSwitch3AQ_Flyback_060622; Rev.3.4; Copyright Power Integrations 2022**	**INPUT**	**INFO**	**OUTPUT**	**UNITS**	**InnoSwitch3-AQ Flyback Design Spreadsheet**
2	**APPLICATION VARIABLES**					
3	VOUT	15.00		15.00	V	Output Voltage
4	**OPERATING CONDITION 1**					
5	VINDC1	1000.00		1000.00	V	Input DC voltage 1
6	IOUT1	2.333		2.333	A	Output current 1
7	POUT1			35.00	W	Output power 1
8	EFFICIENCY1			0.85		Converter efficiency for output 1
9	Z_FACTOR1			0.50		Z-factor for output 1
11	**OPERATING CONDITION 2**					
12	VINDC2	80.00		80.00	V	Input DC voltage 2
13	IOUT2	2.333		2.333	A	Output current 2
14	POUT2			35.00	W	Output power 2
15	EFFICIENCY2			0.85		Converter efficiency for output 2
16	Z_FACTOR2			0.50		Z-factor for output 2
69	**PRIMARY CONTROLLER SELECTION**					
70	ILIMIT_MODE	INCREASED		INCREASED		Device current limit mode
71	VDRAIN_BREAKDOWN			1700	V	Device breakdown voltage
72	DEVICE_GENERIC			INN39X9		Device selection
73	DEVICE_CODE	INN3949CQ		INN3949CQ		Device code
74	PDEVICE_MAX			70	W	Device maximum power capability
75	RDSON_25DEG			0.62	Ω	Primary switch on-time resistance at 25°C
76	RDSON_125DEG			1.10	Ω	Primary switch on-time resistance at 125°C
77	ILIMIT_MIN			1.981	A	Primary switch minimum current limit
78	ILIMIT_TYP			2.130	A	Primary switch typical current limit
79	ILIMIT_MAX			2.279	A	Primary switch maximum current limit
80	VDRAIN_ON_PRSW			0.53	V	Primary switch on-time voltage drop
81	VDRAIN_OFF_PRSW			1217.5	V	Peak drain voltage on the primary switch during turn-off
85	**WORST CASE ELECTRICAL PARAMETERS**					
86	FSWITCHING_MAX	55500		55500	Hz	Maximum switching frequency at full load and the valley of the minimum input AC voltage
87	VOR	187.5		187.5	V	Voltage reflected to the primary winding (corresponding to set-point 1) when the primary switch turns off
88	KP			2.107		Measure of continuous/discontinuous mode of operation
89	MODE_OPERATION			DCM		Mode of operation
90	DUTYCYCLE			0.528		Primary switch duty cycle
91	TIME_ON_MIN			0.75	us	Minimum primary switch on-time
92	TIME_ON_MAX			10.95	us	Maximum primary switch on-time
93	TIME_OFF			8.58	us	Primary switch off-time
94	LPRIMARY_MIN			410.0	uH	Minimum primary magnetizing inductance
95	LPRIMARY_TYP			422.6	uH	Typical primary magnetizing inductance
96	LPRIMARY_TOL	3.0		3.0	%	Primary magnetizing inductance tolerance
97	LPRIMARY_MAX			435.3	uH	Maximum primary magnetizing inductance
99	**PRIMARY CURRENT**					
100	IAVG_PRIMARY			2.019	A	Primary switch average current
101	IPEAK_PRIMARY			2.019	A	Primary switch peak current
102	IPEDESTAL_PRIMARY			0.479	A	Primary switch current pedestal
103	IRIPPLE_PRIMARY			2.019	A	Primary switch ripple current
104	IRMS_PRIMARY			0.803	A	Primary switch RMS current

108	**TRANSFORMER CONSTRUCTION PARAMETERS**					
109	**CORE SELECTION**					
110	CORE	CUSTOM		CUSTOM		Core selection
111	CORE NAME	EIQ30-3C96		EIQ30-3C96		Core code
112	AE	108.0		108.0	mm^2	Core cross sectional area
113	LE	36.2		36.2	mm	Core magnetic path length
114	AL	6000		6000	nH	Ungapped core effective inductance per turns squared
115	VE	3910		3910	mm^3	Core volume
116	BOBBIN NAME	MCT-EIQ3001 V4+6P		MCT-EIQ3001 V4+6P		Bobbin name
117	AW	22.3		22.3	mm^2	Bobbin window area
118	BW	3.60		3.60	mm	Bobbin width
119	MARGIN			0.0	mm	Bobbin safety margin
121	**PRIMARY WINDING**					
122	NPRIMARY			25		Primary winding number of turns
123	BPEAK			3761	Gauss	Peak flux density
124	BMAX			3224	Gauss	Maximum flux density
125	BAC			1612	Gauss	AC flux density (0.5 x Peak to Peak)
126	ALG			676	nH	Typical gapped core effective inductance per turns squared
127	LG			0.178	mm	Core gap length
129	**SECONDARY WINDING**					
130	NSECONDARY	2		2		Secondary winding number of turns
132	**BIAS WINDING**					
133	NBIAS			2		Bias winding number of turns
137	**PRIMARY COMPONENTS SELECTION**					
138	**LINE UNDERVOLTAGE/OVERVOLTAGE**					
139	UVOV Type	UV Only		UV Only		Input Undervoltage/Overvoltage protection type
140	**UNDERVOLTAGE PARAMETERS**					
141	BROWN-IN REQUIRED	30.00		30.00	V	Required DC bus brown-in voltage threshold
142	UNDERVOLTAGE ZENER DIODE	BZM55C9V1		BZM55C9V1		Undervoltage protection zener diode
143	VZ			9.10	V	Zener diode reverse voltage
144	VR			6.80	V	Zener diode reverse voltage at the maximum reverse leakage current
145	ILKG			2.00	uA	Zener diode maximum reverse leakage current
146	BROWN-IN ACTUAL			22.99 - 29.55	V	Actual brown-in voltage range using standard resistors
147	BROWN-OUT ACTUAL			19.76 - 26.44	V	Actual brown-out voltage range using standard resistors
148	**OVERVOLTAGE PARAMETERS**					
149	OVERVOLTAGE REQUIRED		Info		V	For UV Only design, overvoltage feature is disabled
150	OVERVOLTAGE DIODE		Info			OV diode is used only for the overvoltage protection circuit
151	VF				V	OV diode forward voltage
152	VRRM				V	OV diode reverse voltage
153	PIV				V	OV diode peak inverse voltage
154	LINE_OVERVOLTAGE				V	For UV Only design, line overvoltage feature is disabled
155	**DC BUS SENSE RESISTORS**					
156	RLS_H			0.70	MΩ	Connect five 140 kOhm DC bus upper sense resistors to the V-pin for the required UV/OV threshold
157	RLS_L			261	kΩ	DC bus lower sense resistor to the V-pin for the required UV/OV threshold
160	**BIAS WINDING**					

161	VBIAS			9.00	V	Rectified bias voltage
162	VF_BIAS	1.00		1.00	V	Bias winding diode forward drop
163	VREVERSE_BIASDIODE			89.00	V	Bias diode reverse voltage (not accounting parasitic voltage ring)
164	CBIAS			22	uF	Bias winding rectification capacitor
165	CBPP			4.70	uF	BPP pin capacitor
169	**SECONDARY COMPONENTS SELECTION**					
170	**FEEDBACK COMPONENTS**					
171	RFB_UPPER			100.00	kΩ	Upper feedback resistor (connected to the output terminal)
172	RFB_LOWER			9.31	kΩ	Lower feedback resistor
173	CFB_LOWER			330	pF	Lower feedback resistor decoupling capacitor
177	**MULTIPLE OUTPUT PARAMETERS**					
178	**OUTPUT 1**					
179	VOUT1			15.00	V	Output 1 voltage
180	IOUT1	2.333		2.333	A	Output 1 current
181	POUT1			35.00	W	Output 1 power
182	IRMS_SECONDARY1			6.536	A	Root mean squared value of the secondary current for output 1
183	IRIPPLE_CAP_OUTPUT1			6.106	A	Current ripple on the secondary waveform for output 1
184	NSECONDARY1			2		Number of turns for output 1
185	VREVERSE_RECTIFIER1			95.00	V	SRFET reverse voltage (not accounting parasitic voltage ring) for output 1
186	SRFET1	DMT15H017LPS-13		DMT15H017LPS-13		Secondary rectifier (Logic MOSFET) for output 1
187	VF_SRFET1			0.80	V	SRFET on-time drain voltage for output 1
188	VBREAKDOWN_SRFET1			150	V	SRFET breakdown voltage for output 1
189	RDSON_SRFET1			26	mΩ	SRFET on-time drain resistance at 25degC and VGS=4.4V for output 1
217	PO_TOTAL			35.00	W	Total power of all outputs

Table 7 – DER-948Q PIXls Spreadsheet.

9 Performance data

Note: 1. Measurements were taken with the unit under test set-up inside a thermal chamber placed inside a High Voltage (HV) room.

Figure 9 – High Voltage Test Set-up.

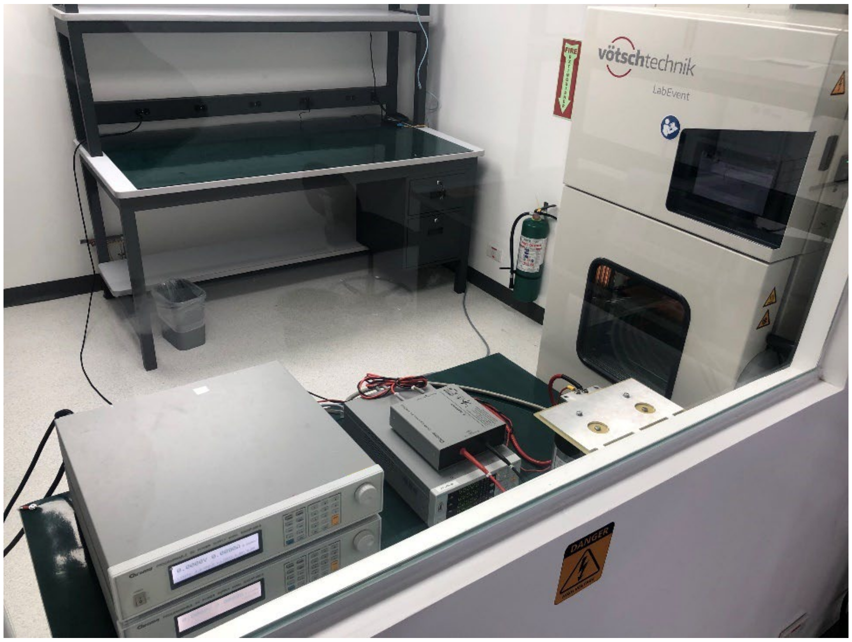


Figure 10 – Test Set-up Inside the High Voltage Room.

2. Unit under test was placed under a box while inside the thermal chamber to eliminate the effect of any airflow.

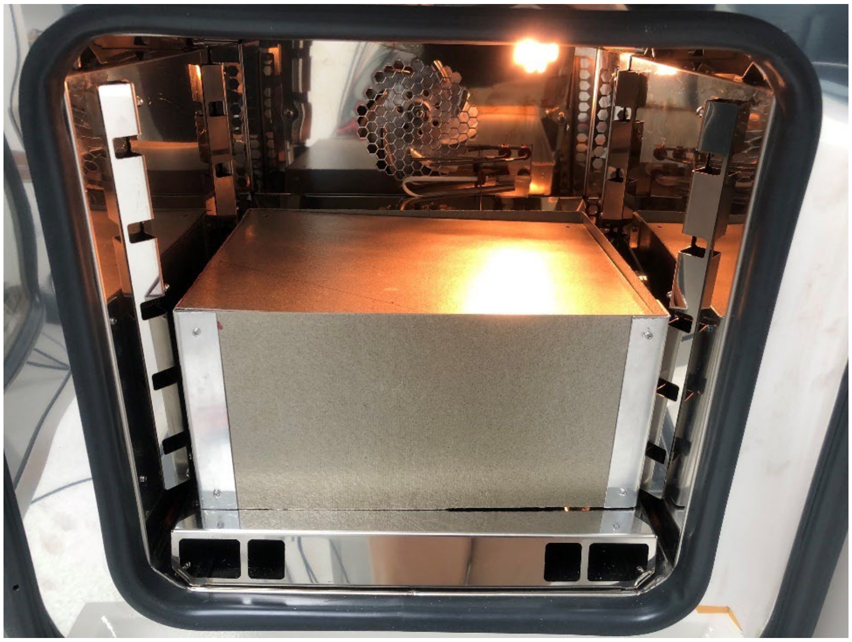


Figure 11 – Unit under test placed under a box to eliminate the effect of airflow.

4. Unit under test was soaked for 5 minutes at full load condition with every change in the input voltage during the start of every test sequence. Also, for every loading condition, unit under test was soaked for at least 20 s before measurements were taken.

9.1 *No-Load Input Power*

Figure 12 shows the test set up diagram for no load input current acquisition. The voltage metering point is placed before the ammeter; this is done to prevent the voltage sensing bias current from affecting the input current measurement. The ammeter used was Tektronix DMM 4050 6-1/2 Digit Precision Multimeter.

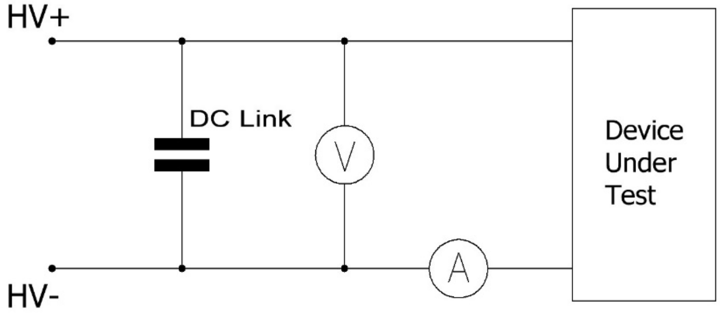


Figure 12 – No-Load Input Power Measurement Diagram.

The unit was soaked for ten minutes before starting data averaging of fifty thousand samples over a period of one minute. Analog filtering is also enabled to improve measurement accuracy.

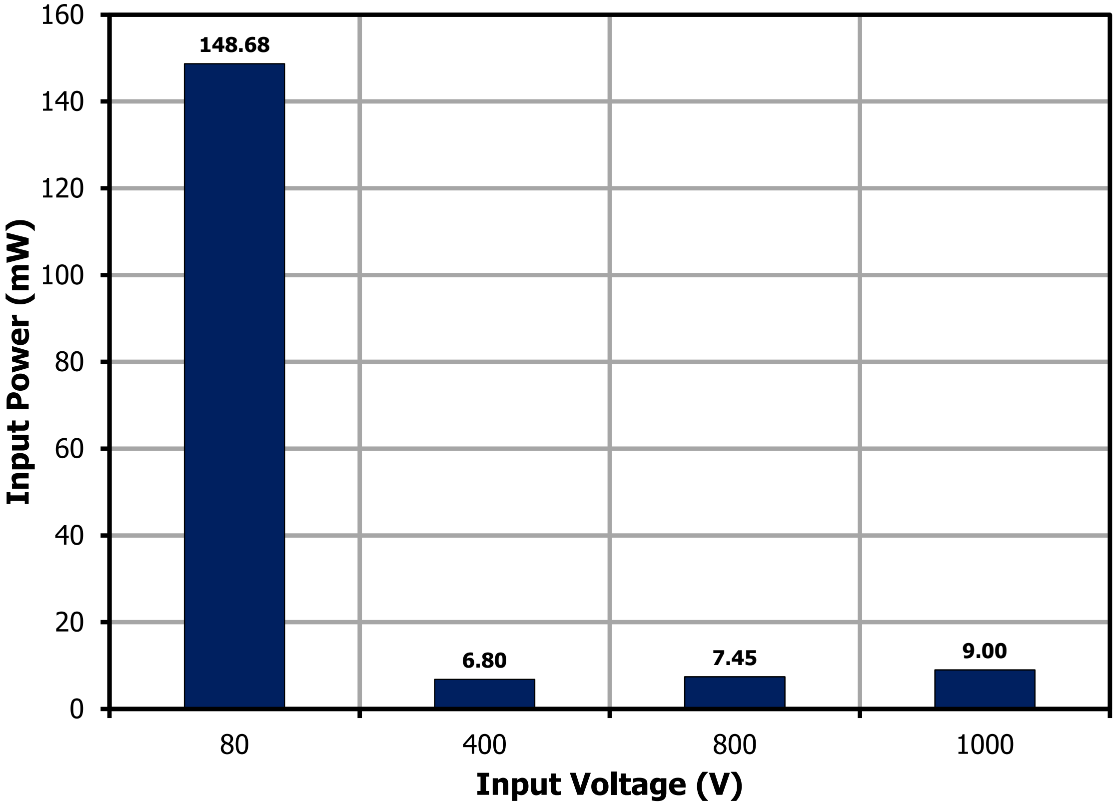


Figure 13 – No-Load Input Power vs. Input Voltage (25 °C Ambient).

9.2 *Efficiency*

9.2.1 Line Efficiency

Line efficiency describes how the change in input voltage affects the overall efficiency of the unit.

9.2.1.1 Line Efficiency at 85 °C Ambient Temperature

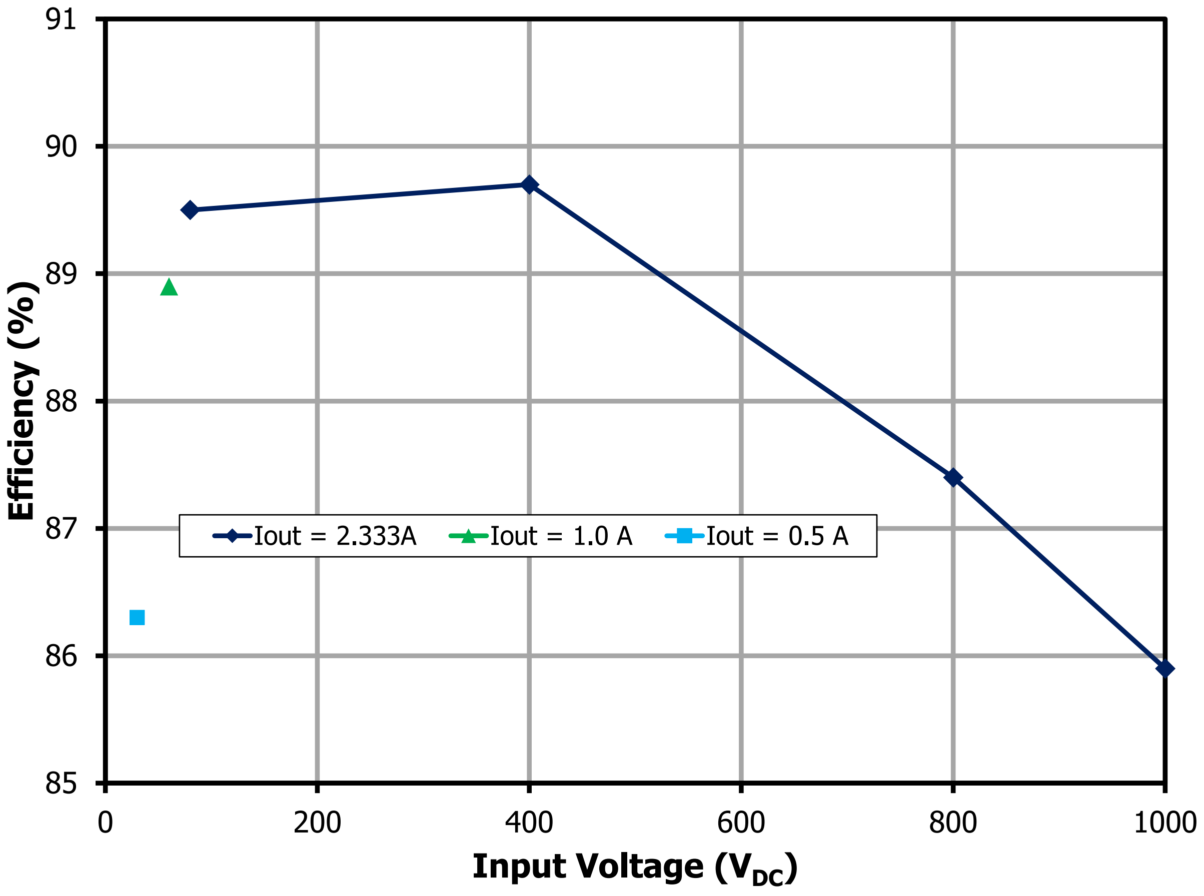


Figure 14 – Full Load Efficiency vs. Input Line Voltage (85 °C Ambient).[9]

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[9] 100% load for 60 V and 30 V input are 1000 mA and 500 mA, respectively.

9.2.1.2 Line Efficiency at 25 °C Ambient Temperature

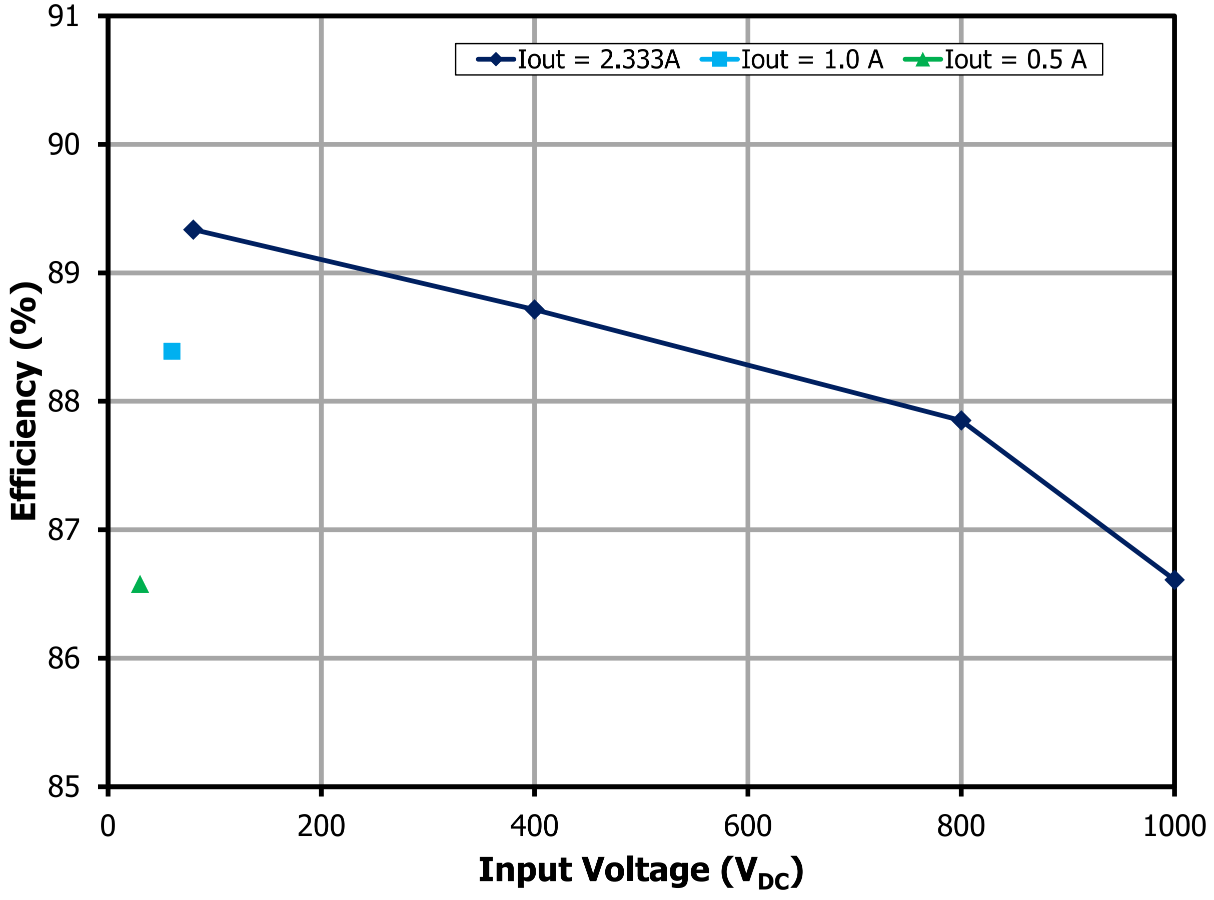

Figure 15 – Full Load Efficiency vs. Input Line Voltage (25 °C Ambient).[10]

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[10] 100% load for 60 V and 30 V input are 1000 mA and 500 mA, respectively.

9.2.1.3 Line Efficiency at -40 °C Ambient Temperature

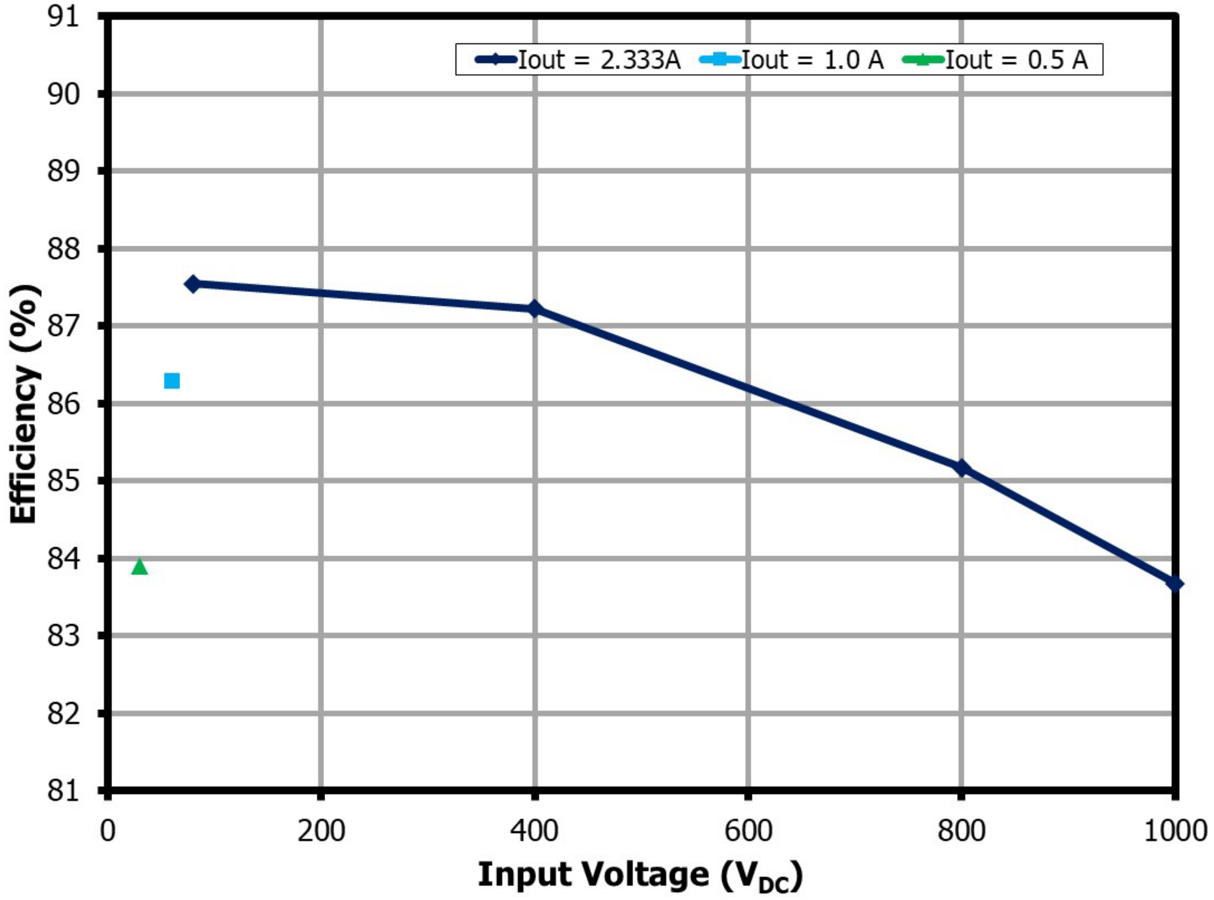

Figure 16 – Full Load Efficiency vs. Input Line Voltage (-40 °C Ambient).[11]

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[11] 100% load for 60 V and 30 V input are 1000 mA and 500 mA, respectively.

9.2.2 Load Efficiency

Load efficiency describes how the change in output loading conditions affects the overall efficiency of the unit.

9.2.2.1 Load Efficiency at 85 °C Ambient

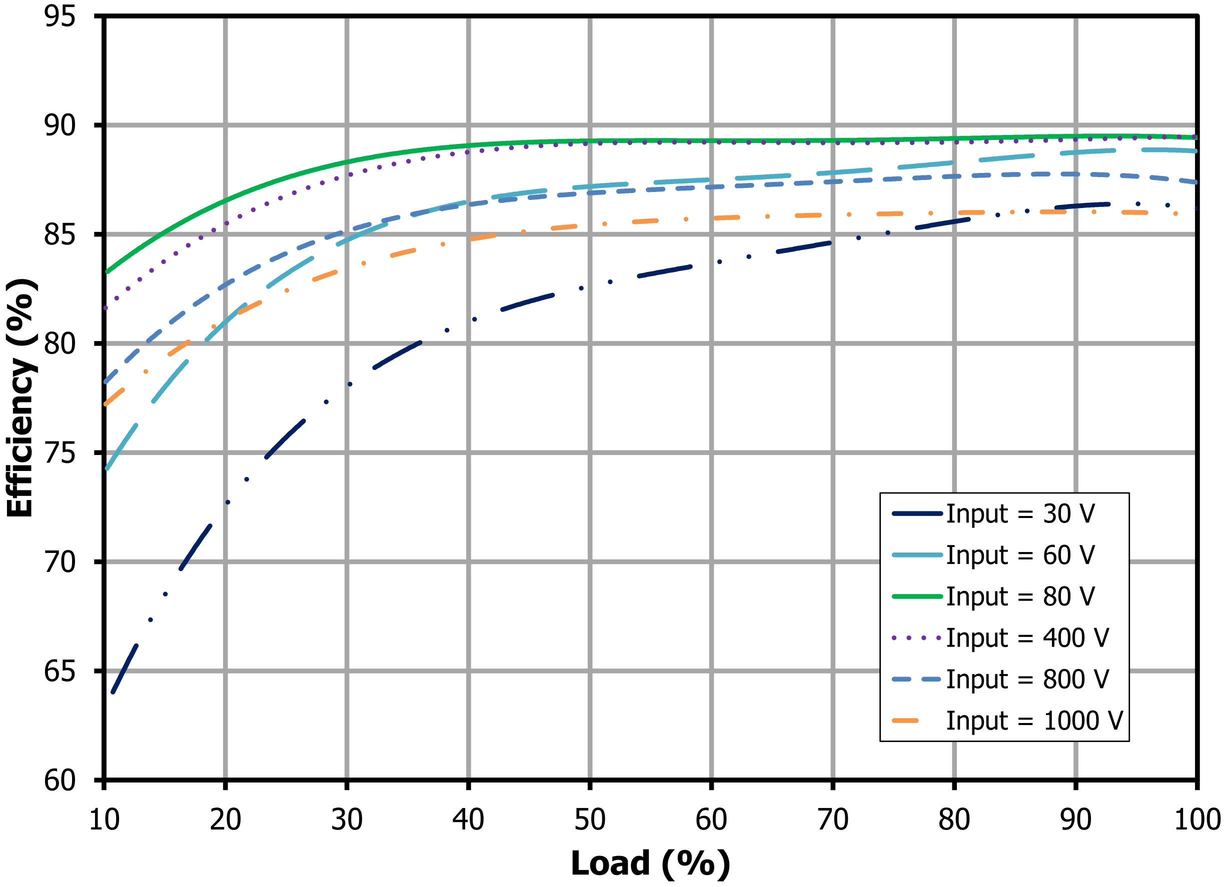

Figure 17 – Efficiency vs. Load at Different Input Voltages (85 °C Ambient).[12]

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[12] 100% load for 60 V and 30 V input are 1000 mA and 500 mA, respectively.

9.2.2.2 Load Efficiency at 25 °C Ambient

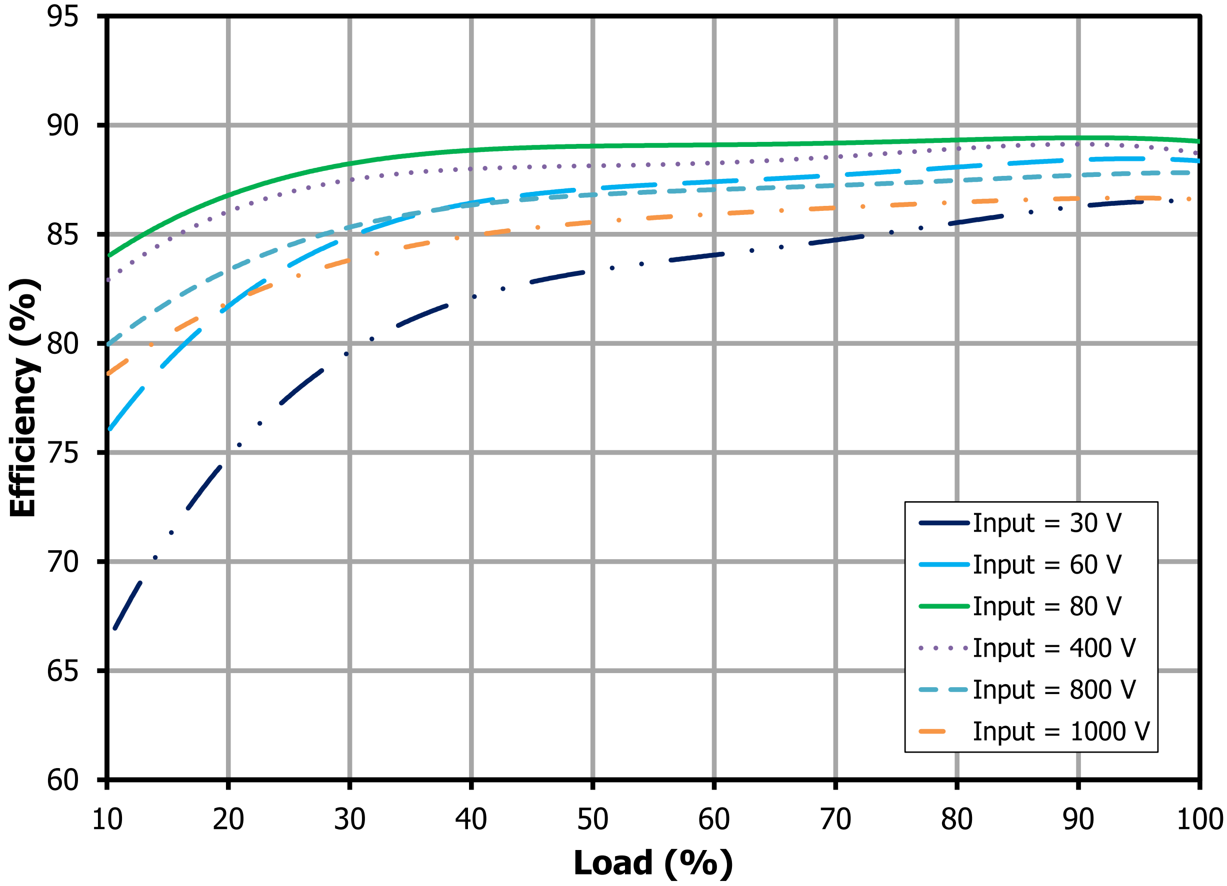

Figure 18 – Efficiency vs. Load at Different Input Voltages (25 °C Ambient).[13]

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[13] 100% load for 60 V and 30 V input are 1000 mA and 500 mA, respectively.

9.2.2.3 Load Efficiency at -40 °C Ambient

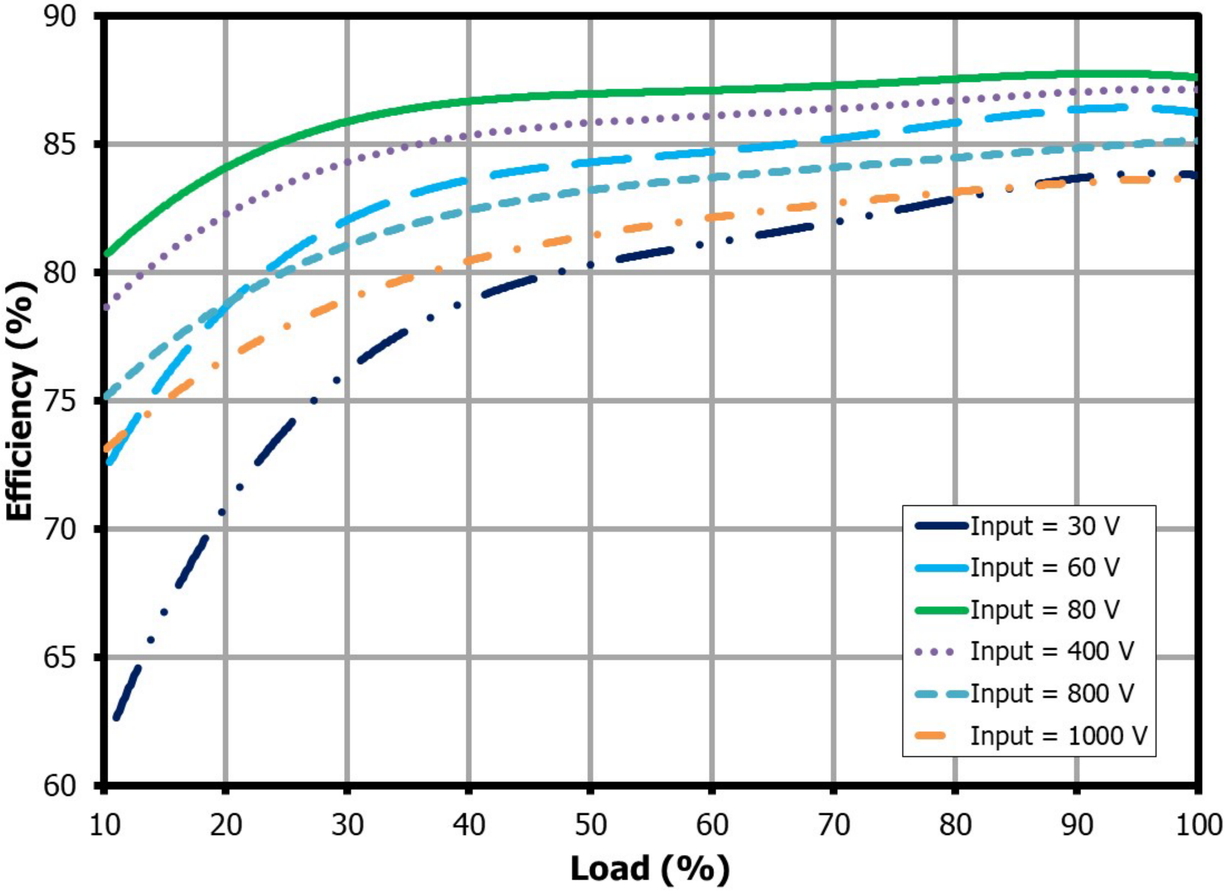

Figure 19 – Efficiency vs. Load at Different Input Voltages (-40 °C Ambient).[14]

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[14] 100% load for 60 V and 30 V input are 1000 mA and 500 mA, respectively.

9.3 *Output Line and Load Regulation*

9.3.1 Load Regulation

Load Regulation describes how the change in output loading conditions affects the average output voltage of the unit.

9.3.1.1 Load Regulation at 85 °C Ambient

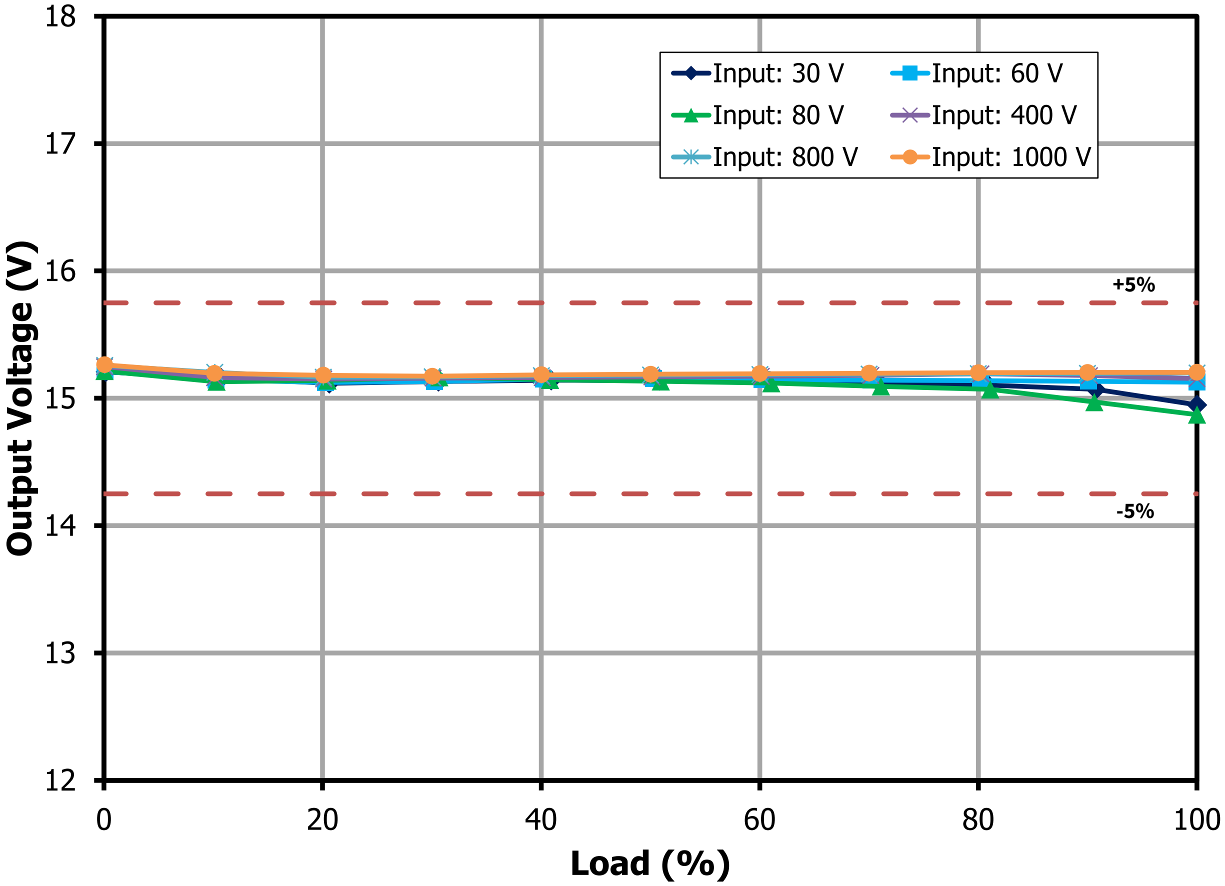

Figure 20 – Output Regulation vs. Load at Different Input Voltages (85 °C Ambient).[15]

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[15] 100% load for 60 V and 30 V input are 1000 mA and 500 mA, respectively.

9.3.1.2 Load Regulation at 25 °C Ambient

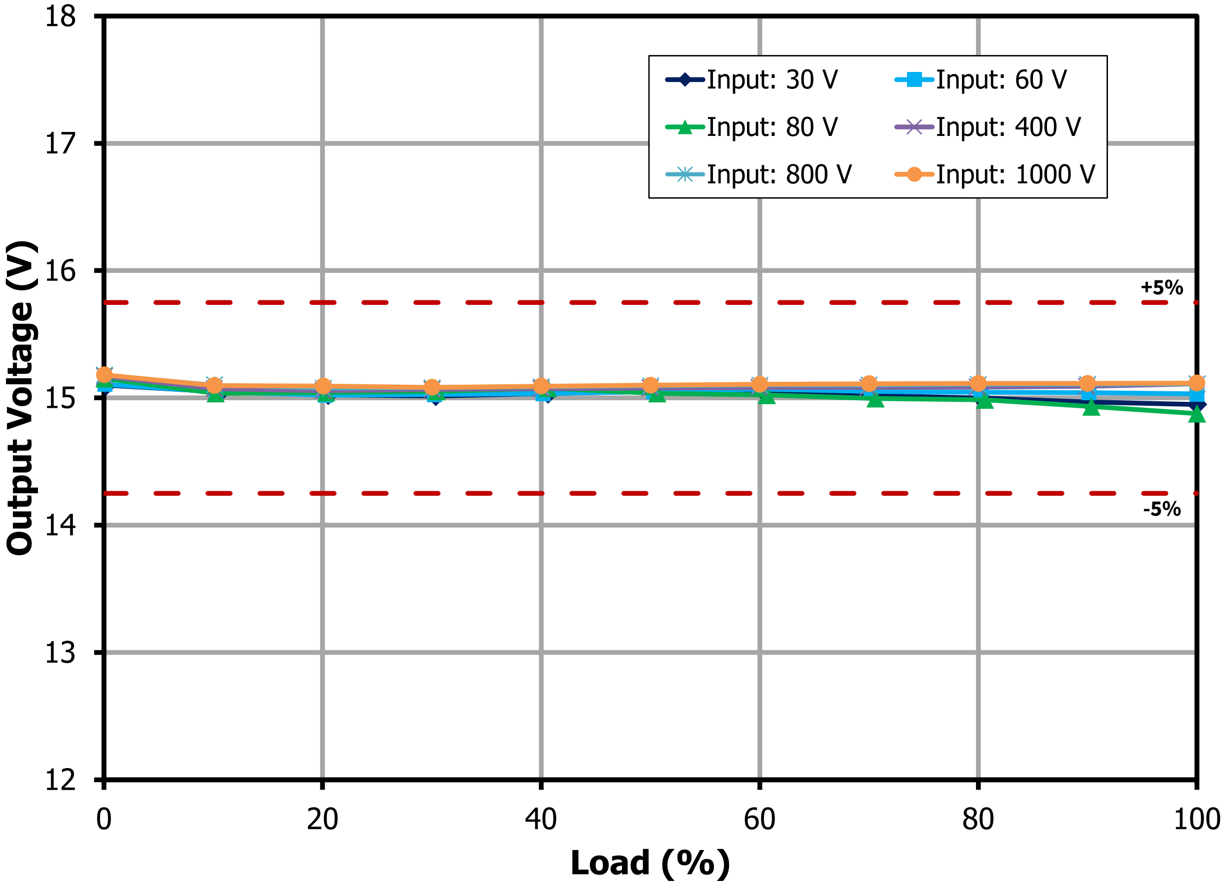

Figure 21 – Output Regulation vs. Load at Different Input Voltages (25 °C Ambient).[16]

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[16] 100% load for 60 V and 30 V input are 1000 mA and 500 mA, respectively.

9.3.1.3 Load Regulation at -40 °C Ambient

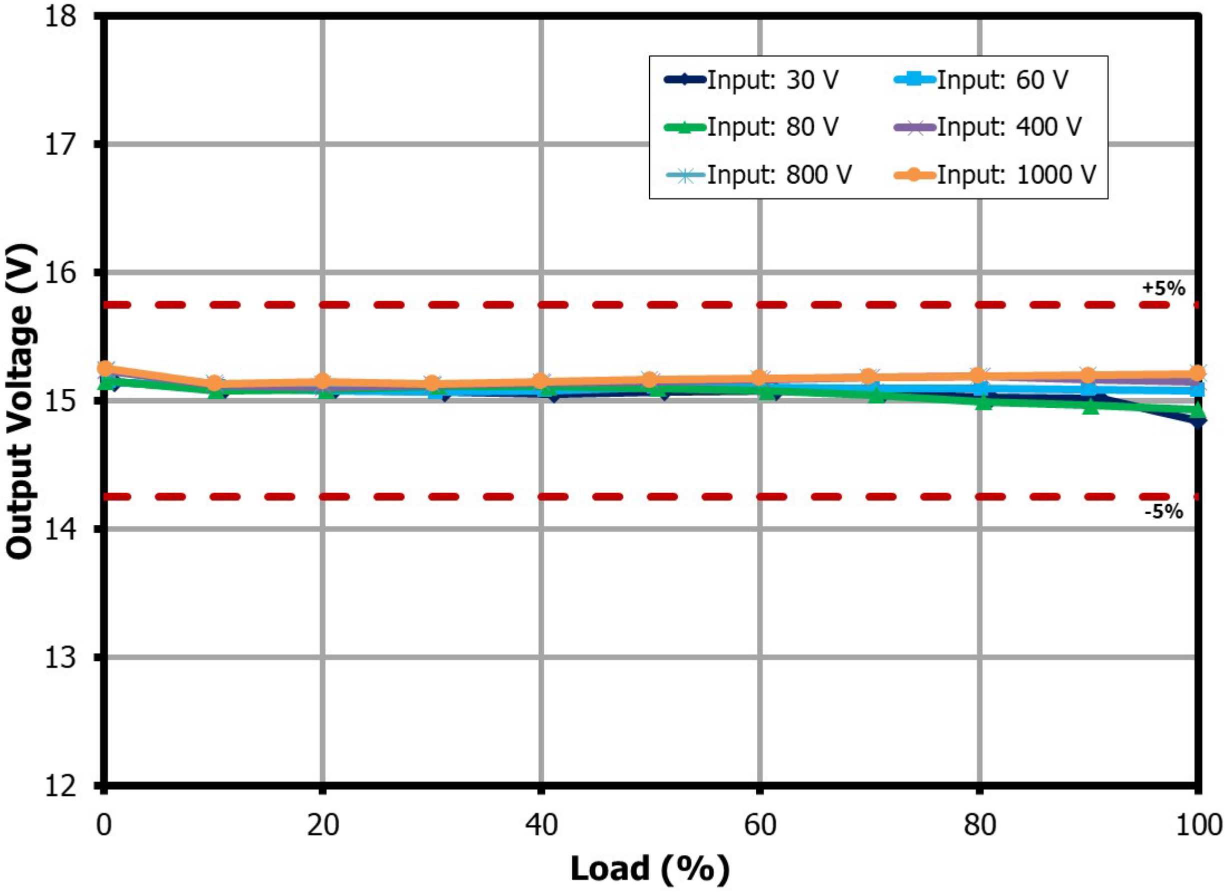

Figure 22 – Output Regulation vs. Load at Different Input Voltages (-40 °C Ambient).[17]

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[17] 100% load for 60 V and 30 V input are 1000 mA and 500 mA, respectively.

9.3.2 Line Regulation

Line Regulation describes how the change in input voltage conditions affects the average output voltage of the unit. The points in the following graphs are only taken from 100% load conditions.

9.3.2.1 Line Regulation at 85 °C Ambient

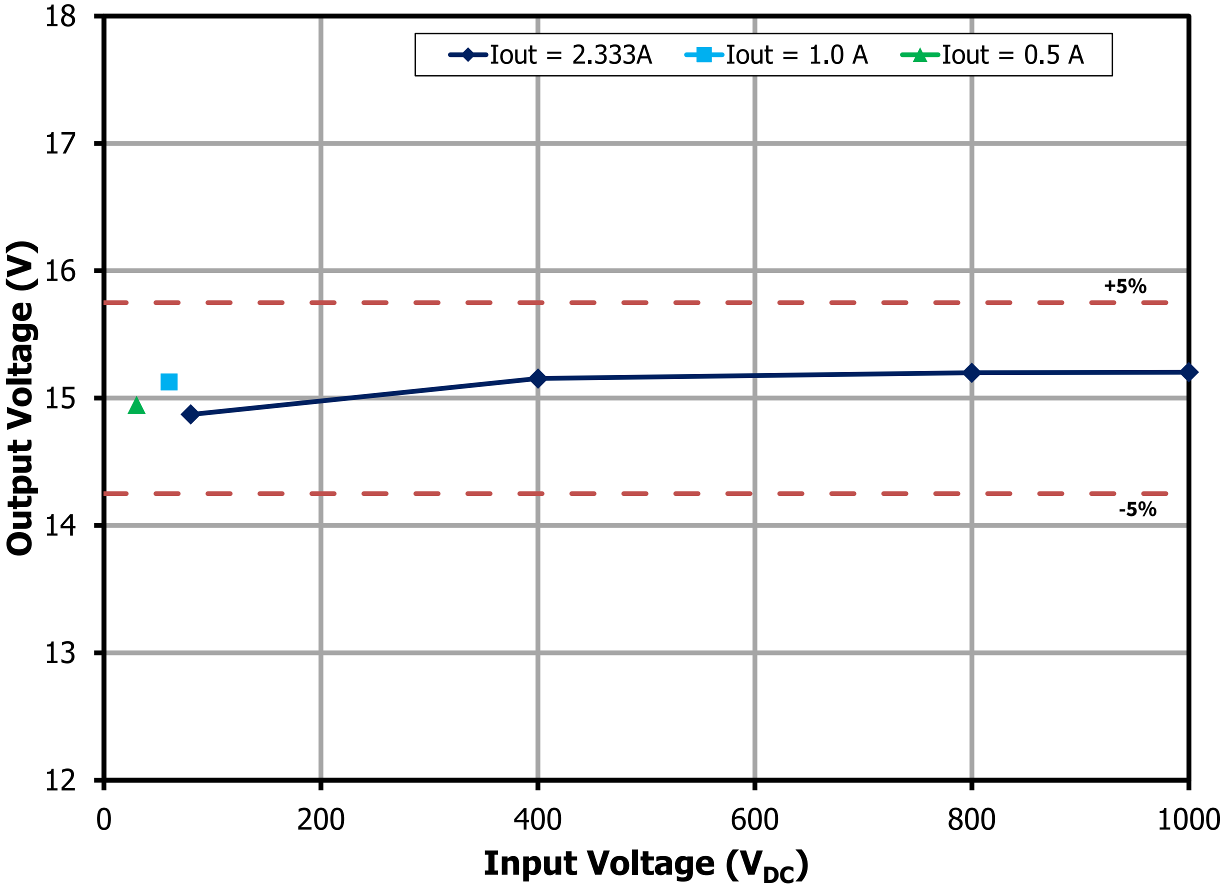

Figure 23 – Output Voltage vs Input Voltage at Full Load (85 °C Ambient)[18]

---

[18] 100% load for 60 V and 30 V input are 1000 mA and 500 mA, respectively.

9.3.2.2 Line Regulation at 25 °C Ambient

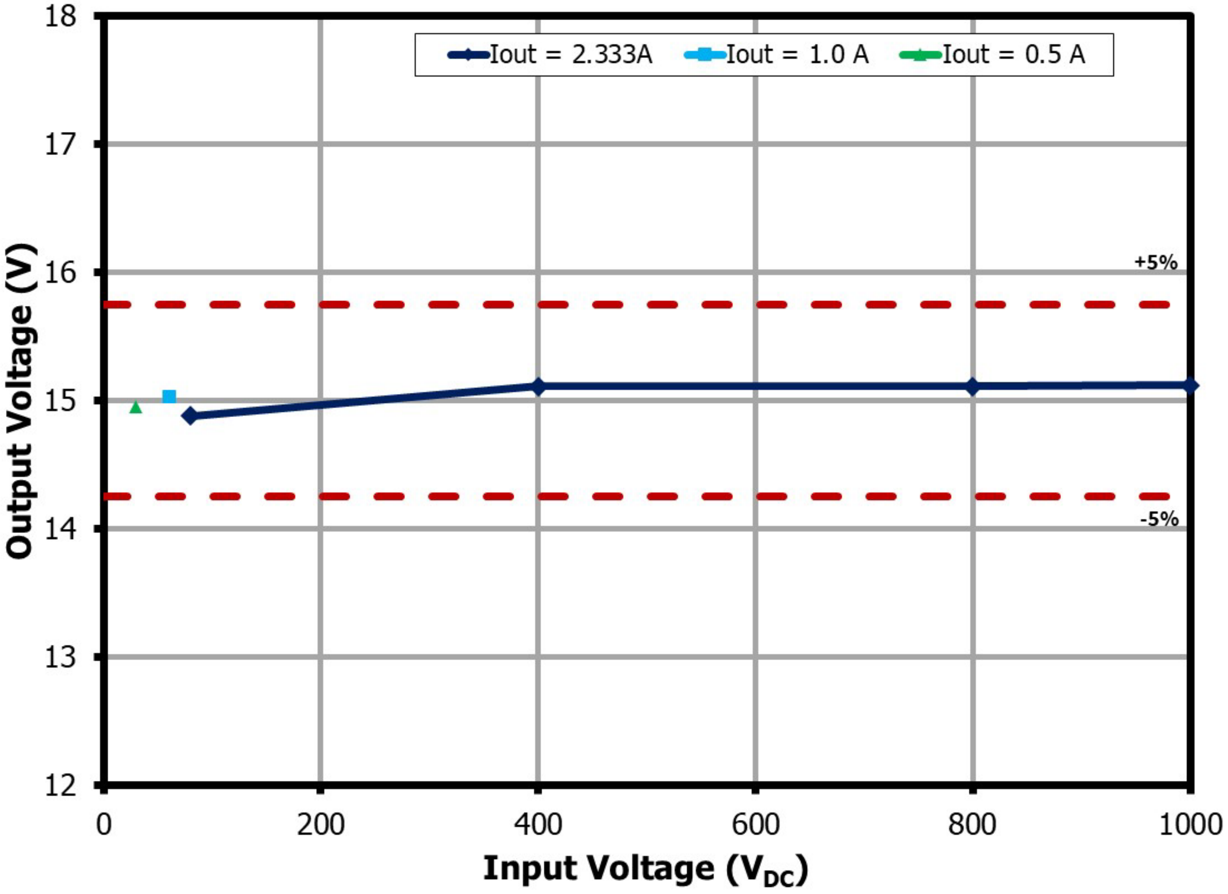

Figure 24 – Output Regulation vs Input Voltage at Full Load (25 °C Ambient).[19]

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[19] 100% load for 60 V and 30 V input are 1000 mA and 500 mA, respectively.

9.3.2.3 Line Regulation at -40 °C Ambient

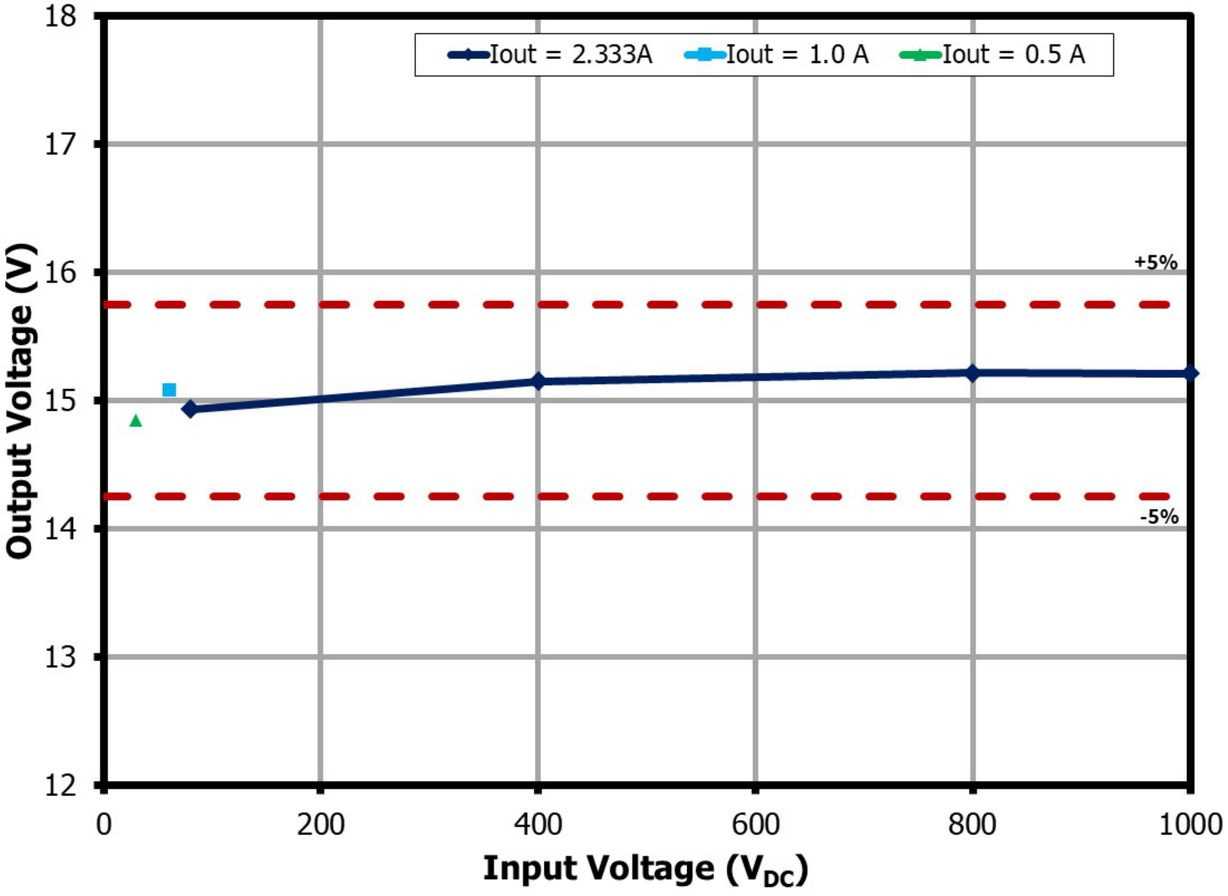

Figure 25 – Output Regulation vs Input Voltage at Full Load (-40 °C Ambient).[20]

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[20] 100% load for 60 V and 30 V input are 1000 mA and 500 mA, respectively.

10 Thermal Performance

10.1 *Thermal Data at 85 °C Ambient Temperature*

The unit was placed inside a thermal chamber and soaked for at least 1 hour to allow component temperatures to settle. Figure 11 shows the set-up for thermal measurement.

Critical Components	**Input Voltage**			
	80	**400**	**800**	**1000**
Output Capacitor (C19)	98.66	100.02	102.38	104.53
Secondary Snubber Resistor (R18)	101.26	105.01	111.81	116.85
SR MOSFET (Q1)	101.95	103.79	107.28	110.55
SR MOSFET (Q2)	104.21	106	109.6	113.1
Transformer Winding	107.54	110.47	120.09	128.86
Transformer Core	104.43	108.76	119.07	126.65
InnoSwitch3-AQ	112.7	105	115.66	126.92
Primary Snubber (R3)	110.9	106.09	109.88	124.06
Primary Snubber (R15)	109.2	105.93	108.23	116.71
Common Mode Choke Core	105.14	105.15	107.37	113.98
Common Mode Choke Winding	102.14	102.24	103.81	109.24

Table 8 – Thermal Data at 85 °C at Different Input Voltages.

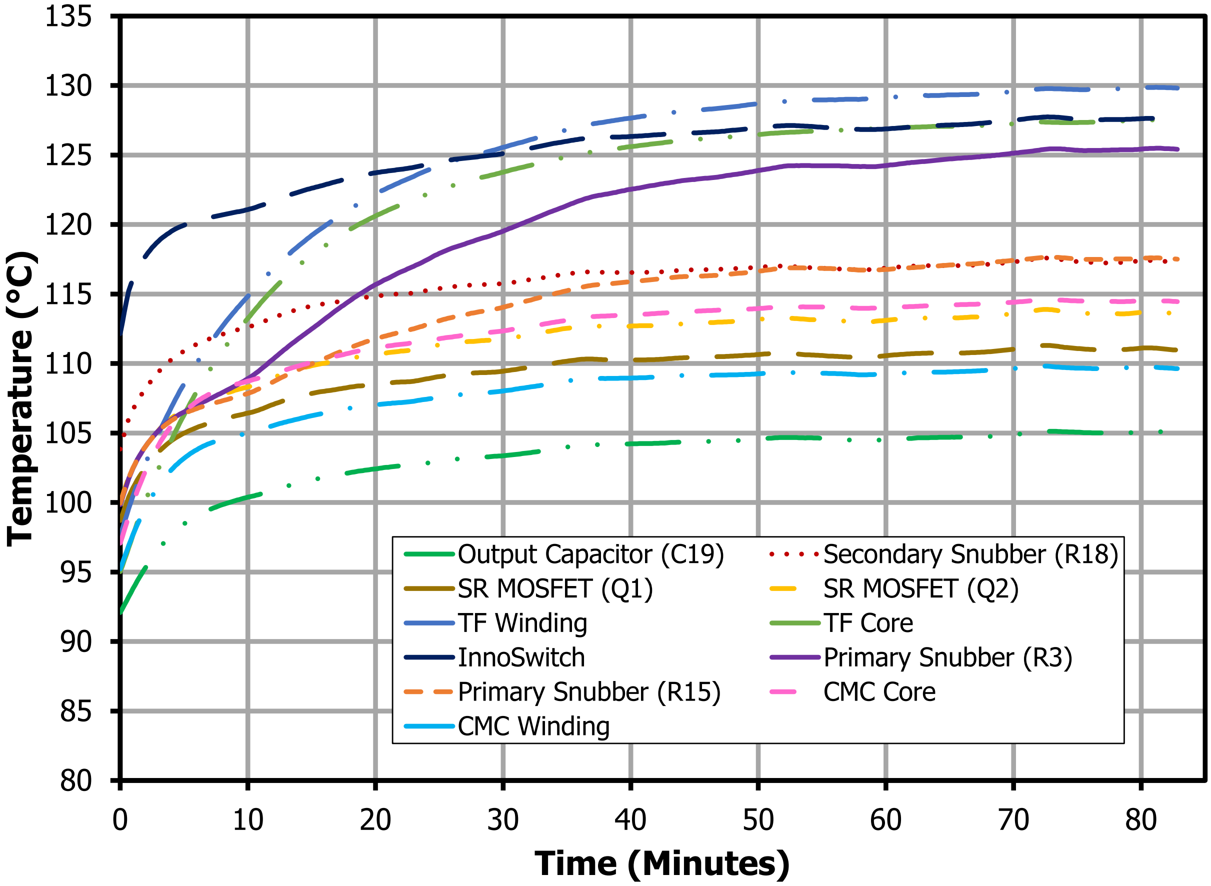


Figure 26 – Component Temperatures at 85 °C Ambient, 1000 V Input.

10.2 *Thermal Image Data at 25 °C Ambient Temperature*

The following thermal scans are captured using a Fluke thermal imager after soaking for at least 1 hour in an enclosure to minimize the effect of air flow.

Critical Components	Input Voltage			
	80 V	400 V	800 V	1000 V
Output Cap (C19)	43.20	45.00	45.60	48.40
Secondary Snubber Resistor	45.50	50.20	58.40	62.00
SR MOSFET (Q1)	46.40	49.20	52.30	54.10
SR MOSFET (Q2)	48.80	51.50	54.10	55.70
Transformer	57.60	62.30	67.60	70.60
InnoSwitch3-AQ	60.80	59.40	70.90	81.40
Primary Snubber Diode	62.10	61.90	57.80	58.70
Primary Snubber (R3)	62.60	66.40	60.50	60.60
Primary Snubber (R15)	60.40	67.00	61.10	60.90
Common Mode Choke	51.20	73.80	62.70	62.40

Table 9 – Thermals Data at 25 °C at Different Input Voltages.

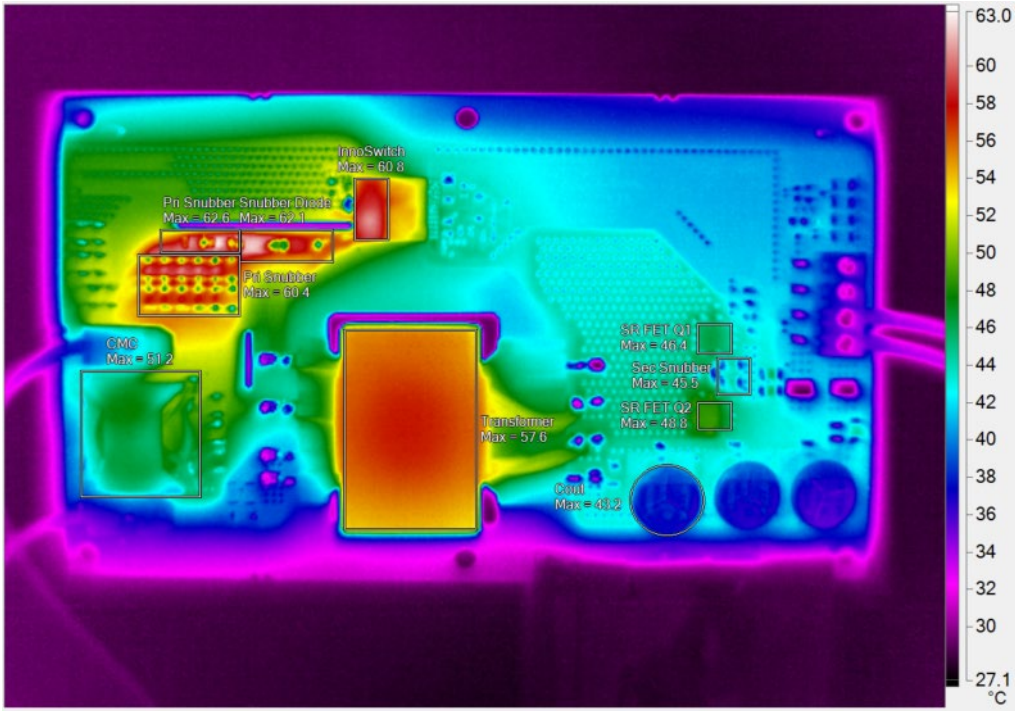


Figure 27 – PCB Top Thermal Scans at 80 V Input.

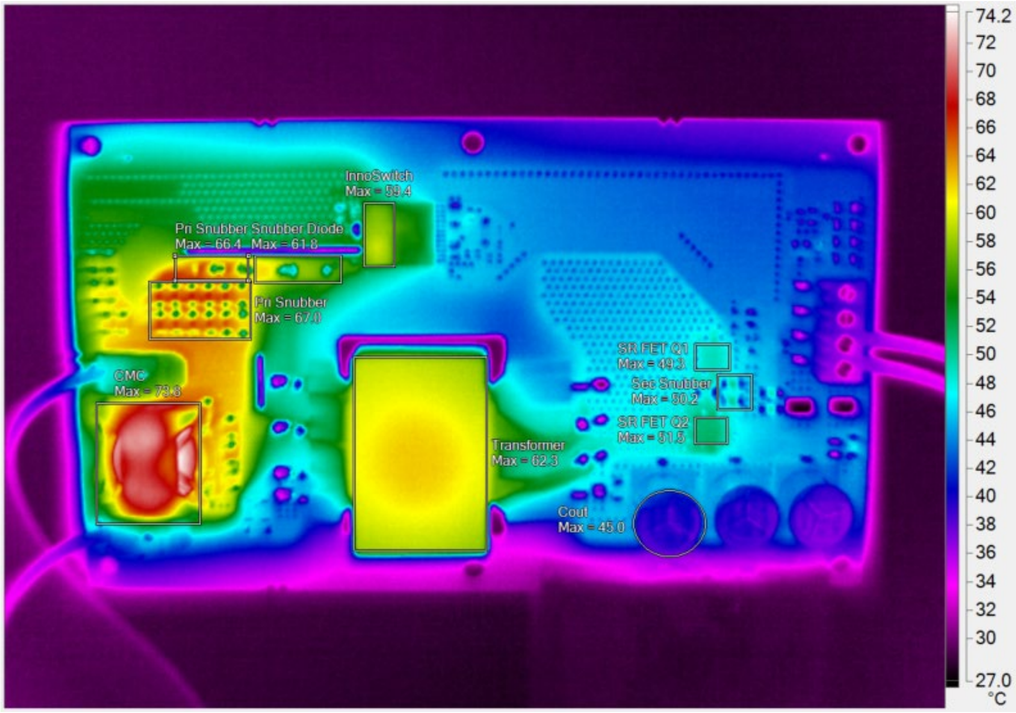


Figure 28 – PCB Top Thermal Scans at 400 V Input.

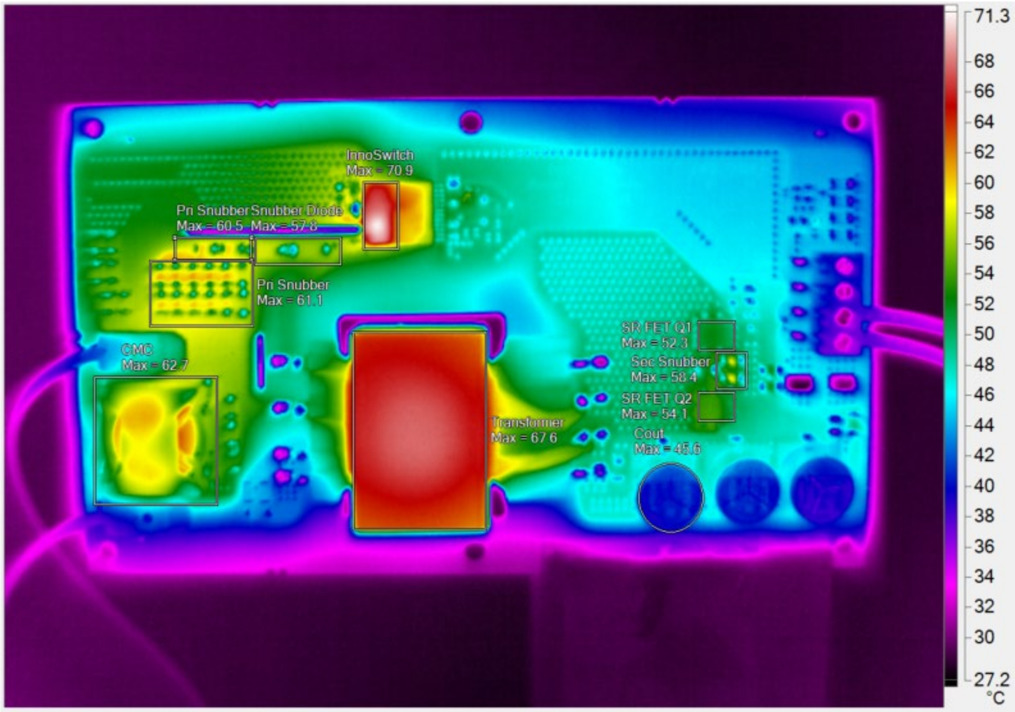


Figure 29 – PCB Top Thermal Scans at 800 V Input.

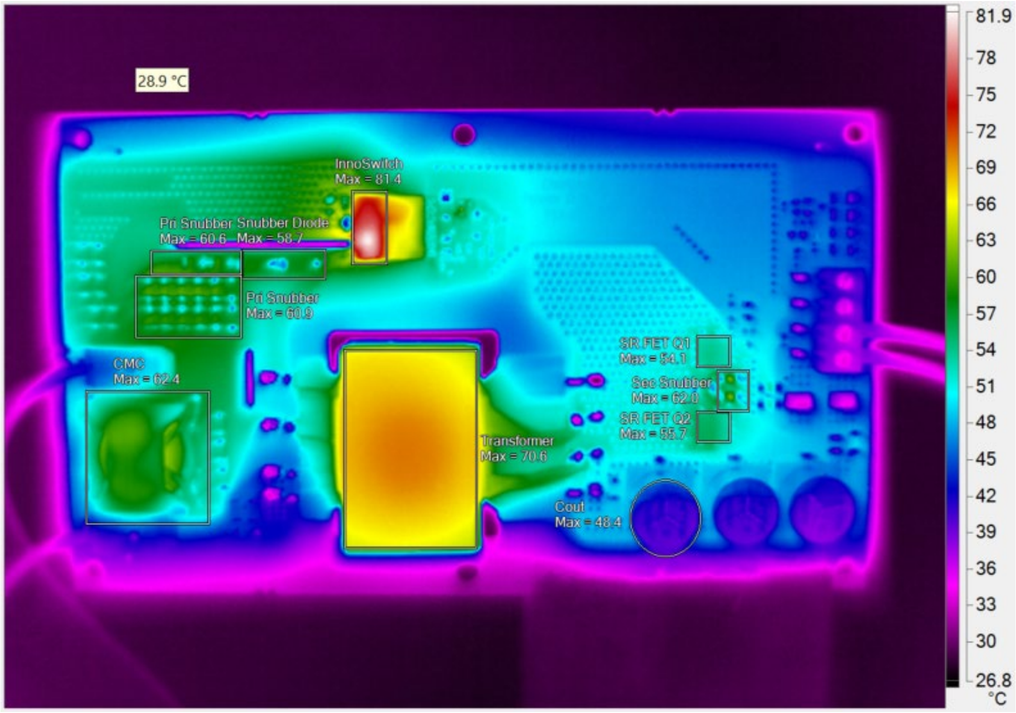


Figure 30 – PCB Top Thermal Scans at 1000 V Input.

11 Waveforms

11.1 *Start-Up Waveforms*

The following measurements were taken by hot plugging-in the unit under test to a DC link capacitor fully charged[21] with different test input voltages. Constant resistance load configuration was used for all start up tests.

11.1.1 Output Voltage and Current at 25 °C Ambient Temperature[22,23]

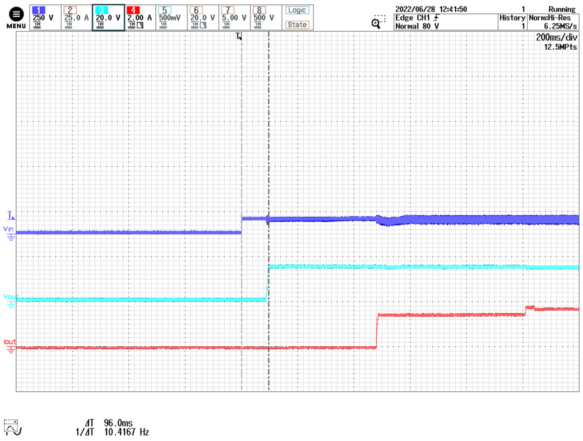


Figure 31 – Output Voltage and Current.
80 V_{DC}, 6.43 ohms Load.
CH1: V_{IN}, 250 V / div.
CH3: V_{OUT}, 20 V / div.
CH4: I_{OUT}, 2 A / div.
Time: 200 ms / div.

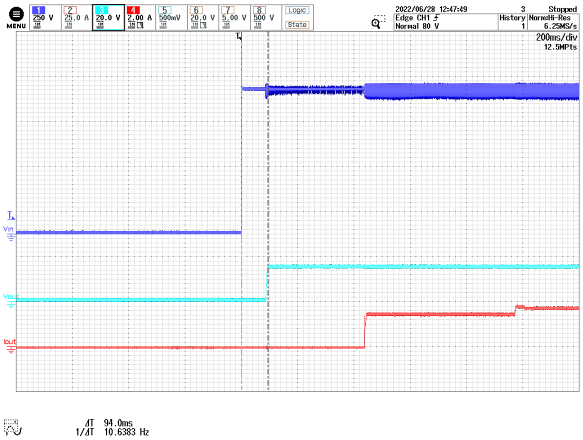


Figure 32 – Output Voltage and Current.
800 V_{DC}, 6.43 ohms Load.
CH1: V_{IN}, 250 V / div.
CH3: V_{OUT}, 20 V / div.
CH4: I_{OUT}, 2 A / div.
Time: 200 ms / div.

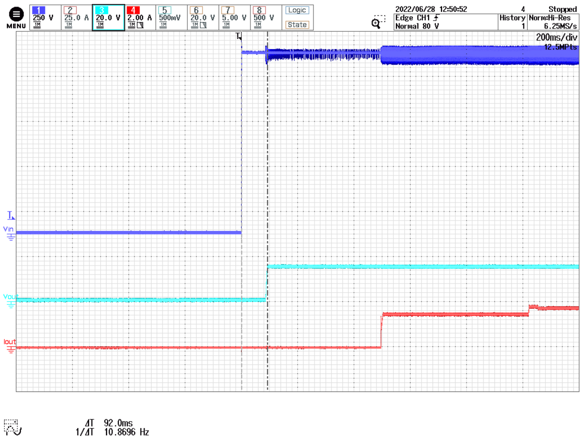


Figure 33 – Output Voltage and Current.
1000 V_{DC}, 6.43 ohms Load.
CH1: V_{IN}, 250 V / div.
CH3: V_{OUT}, 20 V / div.
CH4: I_{OUT}, 2 A / div.
Time: 200 ms / div.

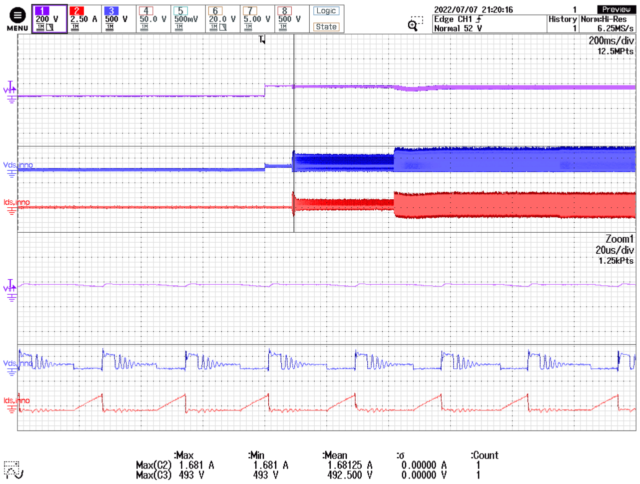
---

[21] Inrush current was limited by adding a 10 Ω series resistor between the DC link capacitor and the unit under test.

[22] Voltage dip on the V_{IN} waveform is due to the effective line impedance from the DC link capacitor to the unit under test.

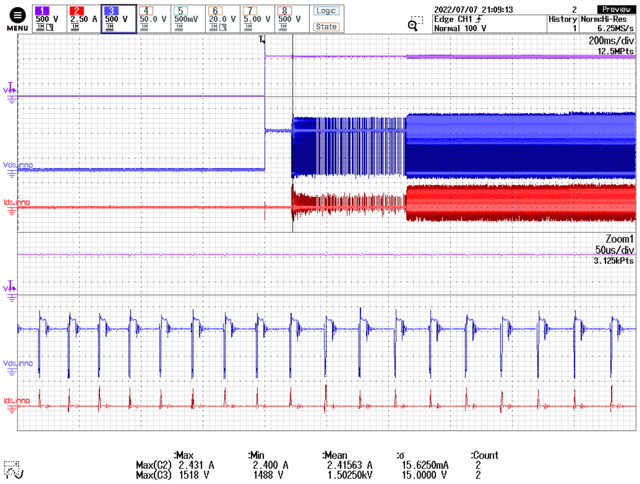
[23] The instance of small step increase seen on the I_{OUT} waveform is due to the CR (Constant Resistance) mode response of the electronic load. The delay between V_{OUT} and I_{OUT} rising edge is also due to the electronic load response.

11.1.2 InnoSwitch3-AQ Drain Voltage and Current at 25 °C Ambient Temperature[24,25]



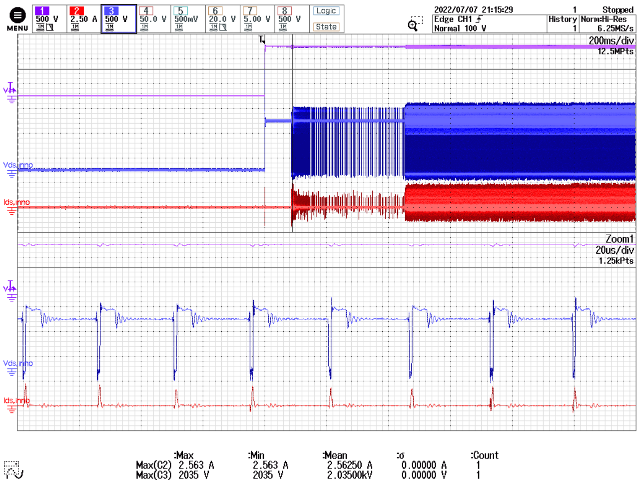
	:Max	:Min	:Mean	:σ	:Count
Max(C2)	1.681 A	1.681 A	1.68125 A	0.00000 A	1
Max(C3)	493 V	493 V	492.500 V	0.00000 V	1

Figure 34 – INN3949CQ Drain Voltage and Current.
80 V_{DC}, 6.43 ohms Load.
CH1: V_{IN}, 200 V / div.
CH2: I_D, 2.5 A / div.
CH3: V_{DS}, 500 V / div.
Time: 200 ms / div.



	:Max	:Min	:Mean	:σ	:Count
Max(C2)	2.431 A	2.400 A	2.41563 A	15.6250mA	2
Max(C3)	1518 V	1488 V	1.50250kV	15.0000 V	2

Figure 35 – INN3949CQ Drain Voltage and Current.
800 V_{DC}, 6.43 ohms Load.
CH1: V_{IN}, 500 V / div.
CH2: I_D, 2.5 A / div.
CH3: V_{DS}, 500 V / div.
Time: 200 ms / div.



	:Max	:Min	:Mean	:σ	:Count
Max(C2)	2.563 A	2.563 A	2.56250 A	0.00000 A	1
Max(C3)	2035 V	2035 V	2.03500kV	0.00000 V	1

Figure 36 – INN3949CQ Drain Voltage and Current.
1000 V_{DC}, 6.43 ohms Load.
CH1: V_{IN}, 500 V / div.
CH2: I_D, 2.5 A / div.
CH3: V_{DS}, 500 V / div.
Time: 200 ms / div.

---

[24] The time between when V_{IN} is turned on and the InnoSwitch starts switching is due to the "Wait and Listen" period of the InnoSwitch.

[25] The change in the switching frequency of the InnoSwitch is due to the CR (Constant Resistance) mode response of the electronic load.

11.1.3 SR FET Drain Voltage and Current at 25 °C Ambient Temperature[26,27]

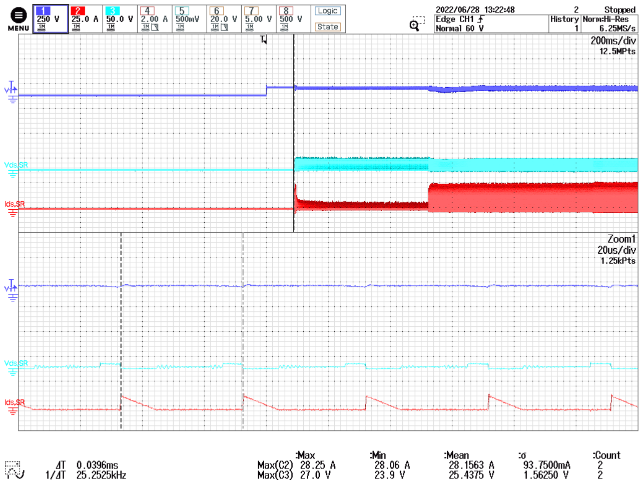
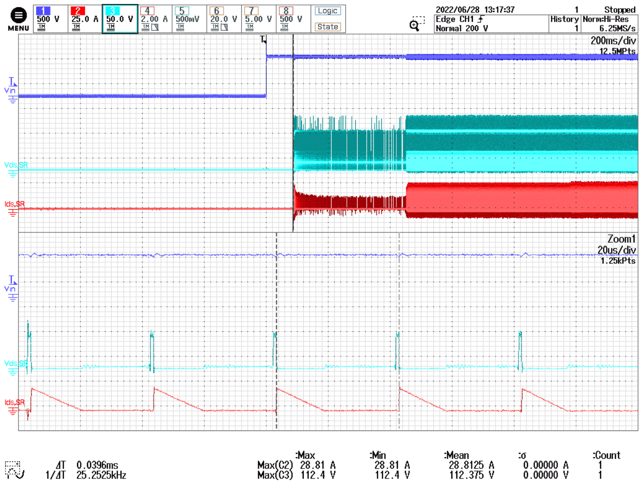


Figure 37 – SR FET Drain Voltage and Current.
80 V_{DC}, 6.43 ohms Load.
CH1: V_{IN}, 250 V / div.
CH3: $V_{DS(SR)}$, 50 V / div.
CH2: $I_{D(SR)}$, 25 A / div.
Time: 200 ms / div.



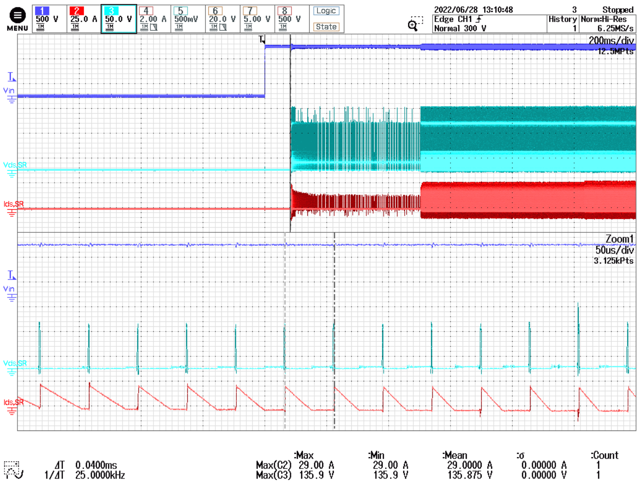


Figure 38 – SR FET Drain Voltage and Current.
800 V_{DC}, 6.43 ohms Load.
CH1: V_{IN}, 500 V / div.
CH3: $V_{DS(SR)}$, 50 V / div.
CH2: $I_{D(SR)}$, 25 A / div.
Time: 200 ms / div.

Figure 39 – SR FET Drain Voltage and Current.
1000 V_{DC}, 6.43 ohms Load.
CH1: V_{IN}, 500 V / div.
CH3: $V_{DS(SR)}$, 50 V / div.
CH2: $I_{D(SR)}$, 25 A / div.
Time: 200 ms / div.

---

[26] The time between when V_{IN} is turned on and the SR FET starts switching is due to the "Wait and Listen" period of the InnoSwitch.
[27] The change in the switching frequency of the SR FET is due to the CR (Constant Resistance) mode response of the electronic load.

11.1.4 Output Voltage and Current at -40 °C Ambient Temperature[28,29]

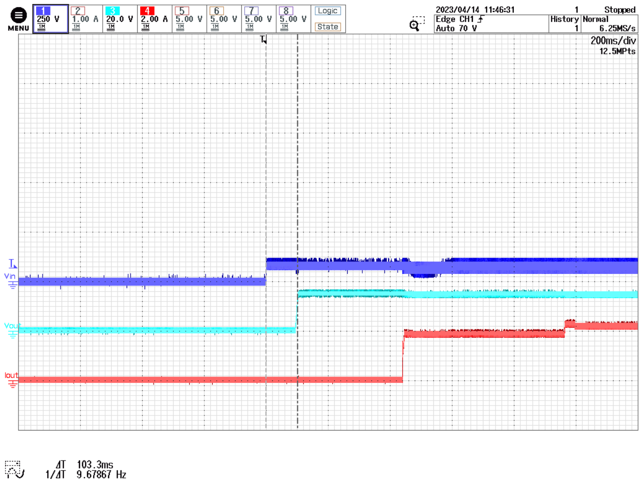
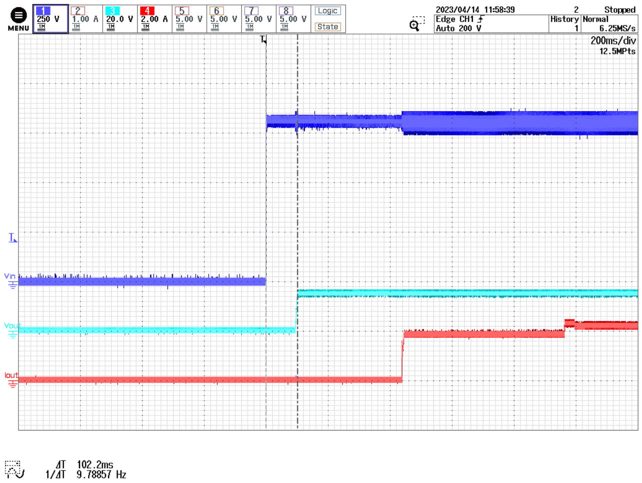


Figure 40 – Output Voltage and Current.
80 V_{DC}, 2.333 A Load
CH1: V_{IN}, 250 V / div.
CH3: V_{OUT}, 20 V / div.
CH4: I_{OUT}, 2 A / div.
Time: 200 ms / div.



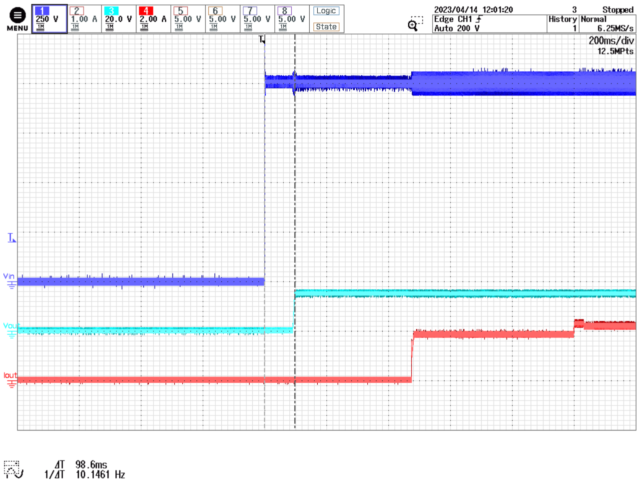


Figure 41 – Output Voltage and Current.
800 V_{DC}, 2.333 A Load.
CH1: V_{IN}, 250 V / div.
CH3: V_{OUT}, 20 V / div.
CH4: I_{OUT}, 2 A / div.
Time: 200 ms / div.

Figure 42 – Output Voltage and Current.
1000 V_{DC}, 2.333 A Load.
CH1: V_{IN}, 250 V / div.
CH3: V_{OUT}, 20 V / div.
CH4: I_{OUT}, 2 A / div.
Time: 200 ms / div.

---

[28] Voltage dip on the V_{IN} waveform is due to the effective line impedance from the DC link capacitor to the unit under test.

[29] The instance of small step increase seen on the I_{OUT} waveform is due to the CR (Constant Resistance) mode response of the electronic load. The delay between V_{OUT} and I_{OUT} rising edge is also due to the electronic load response.

11.1.5 InnoSwitch3-AQ Drain Voltage and Current at -40 °C Ambient Temperature[30,31]

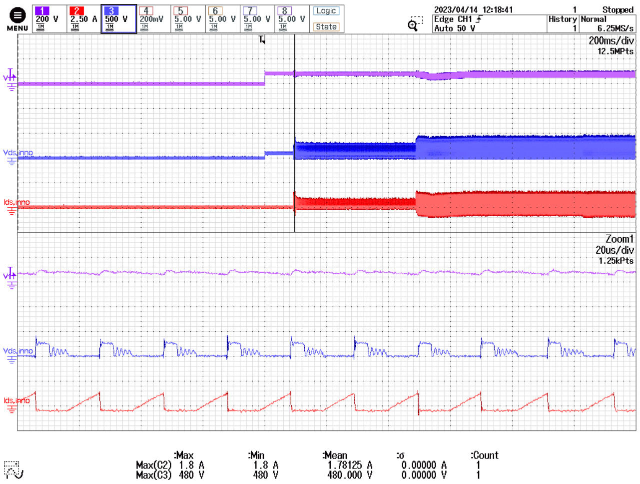


Figure 43 – INN3949CQ Drain Voltage and Current.
80 V_{DC}, 2.333 A Load.
CH1: V_{IN}, 200 V / div.
CH2: I_D, 2.5 A / div.
CH3: V_{DS}, 500 V / div.
Time: 200 ms / div.

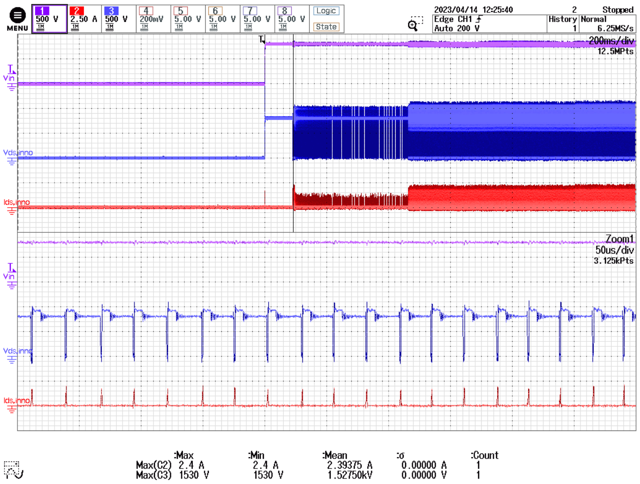


Figure 44 – INN3949CQ Drain Voltage and Current.
800 V_{DC}, 2.333 A Load.
CH1: V_{IN}, 500 V / div.
CH2: I_D, 2.5 A / div.
CH3: V_{DS}, 500 V / div.
Time: 200 ms / div.

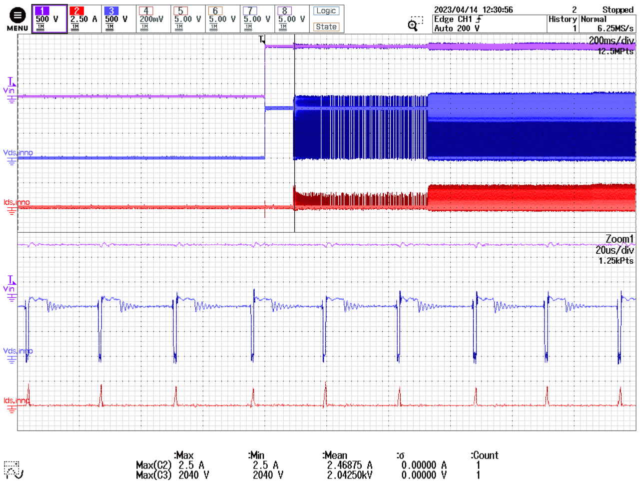


Figure 45 – INN3949CQ Drain Voltage and Current.
1000 V_{DC}, 2.333 A Load.
CH1: V_{IN}, 500 V / div.
CH2: I_D, 2.5 A / div.
CH3: V_{DS}, 500 V / div.
Time: 200 ms / div.

---

[30] The time between when V_{IN} is turned on and the InnoSwitch starts switching is due to the "Wait and Listen" period of the InnoSwitch.

[31] The change in the switching frequency of the InnoSwitch is due to the CR (Constant Resistance) mode response of the electronic load.

11.1.6 SR FET Drain Voltage and Current at -40 °C Ambient Temperature[32,33]

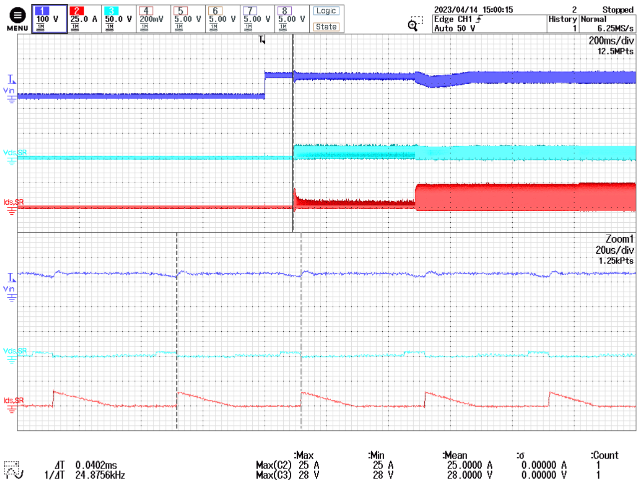


Figure 46 – SR FET Drain Voltage and Current.
80 V_{DC}, 2.333 A Load.
CH1: V_{IN}, 100 V / div.
CH3: $V_{DS(SR)}$, 50 V / div.
CH2: $I_{D(SR)}$, 25 A / div.
Time: 200 ms / div.

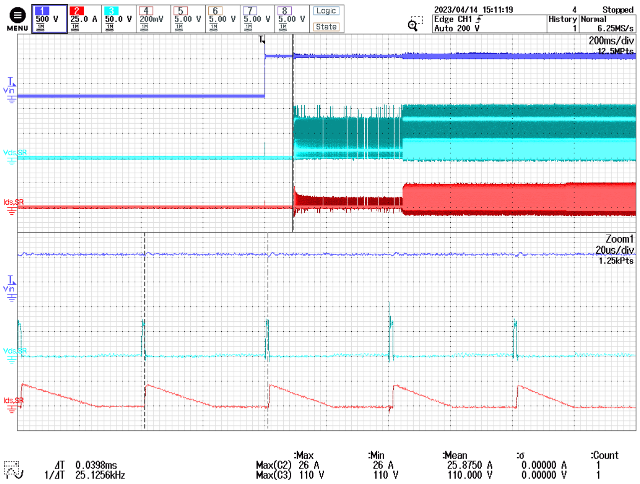


Figure 47 – SR FET Drain Voltage and Current.
800 V_{DC}, 2.333 A ohms Load.
CH1: V_{IN}, 500 V / div.
CH3: $V_{DS(SR)}$, 50 V / div.
CH2: $I_{D(SR)}$, 25 A / div.
Time: 200 ms / div.

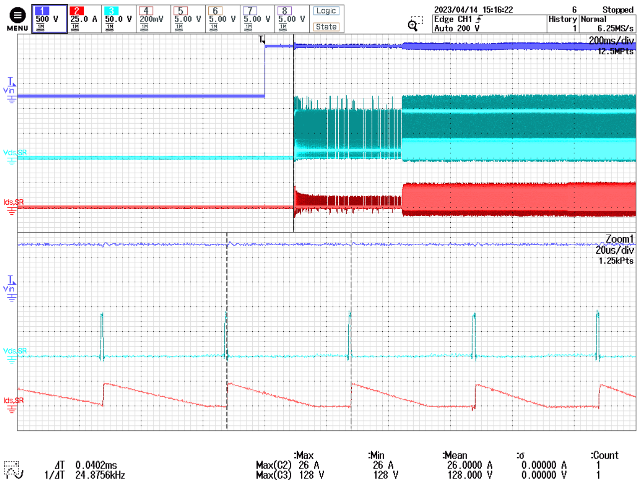


Figure 48 – SR FET Drain Voltage and Current.
1000 V_{DC}, 2.333 A Load.
CH1: V_{IN}, 500 V / div.
CH3: $V_{DS(SR)}$, 50 V / div.
CH2: $I_{D(SR)}$, 25 A / div.
Time: 200 ms / div.

---

[32] The time between when V_{IN} is turned on and the SR FET starts switching is due to the "Wait and Listen" period of the InnoSwitch.

[33] The change in the switching frequency of the SR FET is due to the CR (Constant Resistance) mode response of the electronic load.

11.2 *Steady-State Waveforms*

11.2.1 Switching Waveforms at 85 °C Ambient Temperature

11.2.1.1 Normal Operation Component Stress

	Steady-State Switching Waveforms 85 °C Ambient, Full Load					
Input	**INN3949CQ**			**SR MOSFETs**		
V_{IN}(V)	**I_D(A)**	**V_{DS}(V)**	**V_{STRESS} (%)**	**I_D(A)**[34]	**V_{DS}(V)**[35]	**V_{STRESS} (%)**
80	1.613	511.0	30.06	28.0	27.1	16.27
400	2.088	820.0	48.24	28.19	75.1	48.67
800	2.306	1225.0	72.06	29.0	113	76.00
1000	2.663	1461.0	85.94	30.0	131	88.33

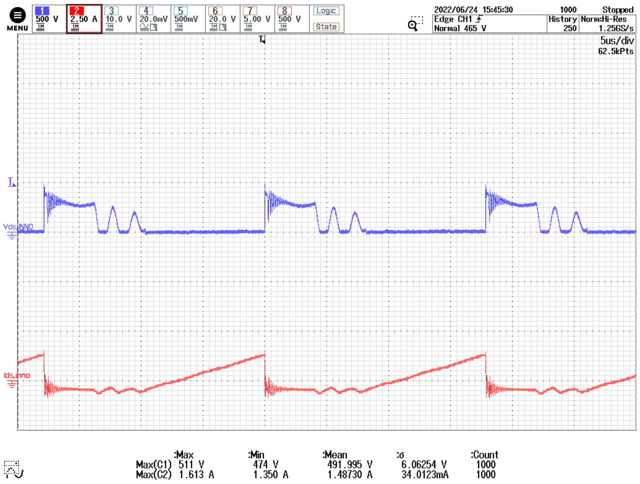
Table 10 – Summary of Critical Component Voltage Stresses at 85 °C Ambient Temperature

---

[34] Synchronous MOSFET current is the sum of Q1 and Q2 currents.

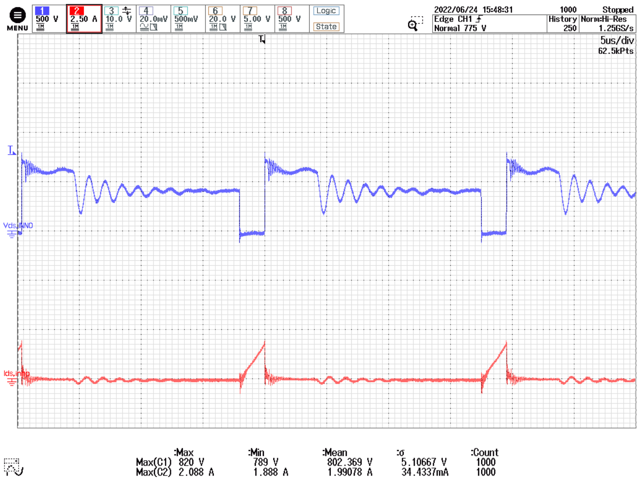
[35] Synchronous MOSFET voltage was taken from Q2.

11.2.1.2 InnoSwitch3-AQ Drain Voltage and Current at 85 °C Ambient Temperature



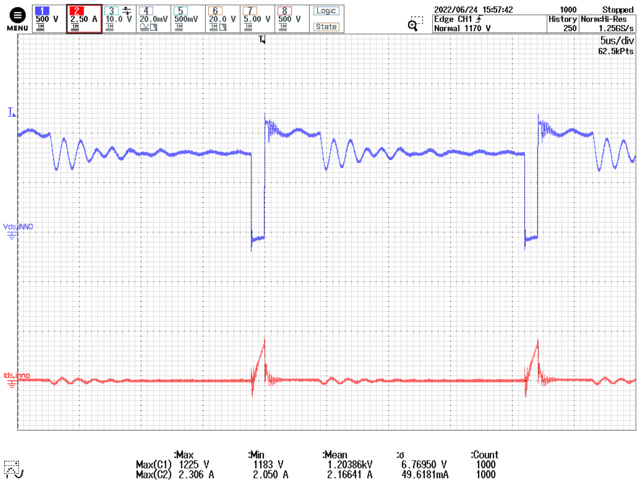
```
          :Max        :Min       :Mean        :σ           :Count
Max(C1)  511 V       474 V      491.995 V    6.06254 V    1000
Max(C2)  1.613 A     1.350 A    1.48730 A    34.0123mA    1000
```

Figure 49 – InnoSwitch3-AQ Drain Voltage and Current.
80 V_{DC}, 2.333 A Load, 85 °C Ambient.
CH1: $V_{DS(IC1)}$, 500 V / div.
CH2: $I_{D(IC1)}$, 2.5 A / div.
Time: 5 µs / div.

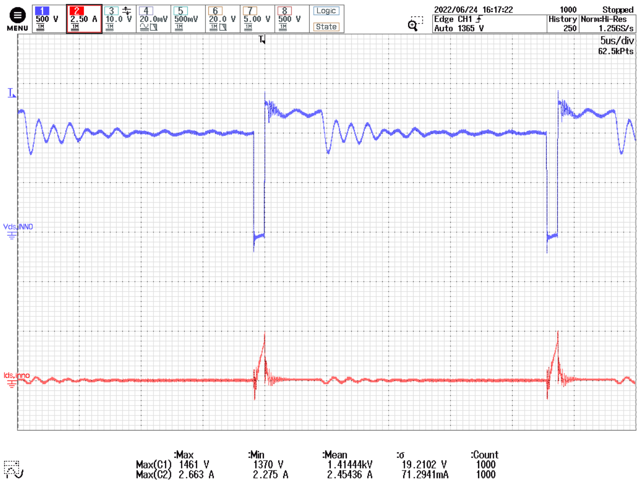


```
          :Max        :Min       :Mean        :σ           :Count
Max(C1)  820 V       789 V      802.369 V    5.10667 V    1000
Max(C2)  2.088 A     1.888 A    1.99078 A    34.4337mA    1000
```

Figure 50 – InnoSwitch3-AQ Drain Voltage and Current.
400 V_{DC}, 2.333 A Load, 85 °C Ambient.
CH1: $V_{DS(IC1)}$, 500 V / div.
CH2: $I_{D(IC1)}$, 2.5 A / div.
Time: 5 µs / div.



```
          :Max        :Min       :Mean        :σ           :Count
Max(C1)  1225 V      1183 V     1.20386kV    6.76950 V    1000
Max(C2)  2.306 A     2.050 A    2.16641 A    49.6181mA    1000
```



```
          :Max        :Min       :Mean        :σ           :Count
Max(C1)  1461 V      1370 V     1.41444kV    19.2102 V    1000
Max(C2)  2.663 A     2.275 A    2.45436 A    71.2941mA    1000
```

Figure 51 – InnoSwitch3-AQ Drain Voltage and Current.
800 V_{DC}, 2.333 A Load, 85 °C Ambient.
CH1: $V_{DS(IC1)}$, 500 V / div.
CH2: $I_{D(IC1)}$, 2.5 A / div.
Time: 5 µs / div.

Figure 52 – InnoSwitch3-AQ Drain Voltage and Current.
1000 V_{DC}, 2.333 A Load, 85 °C Ambient.
CH1: $V_{DS(IC1)}$, 500 V / div.
CH2: $I_{D(IC1)}$, 2.5 A / div.
Time: 5 µs / div.

11.2.1.3 Synchronous Rectifier MOSFETs Drain Voltage and Current at 85 °C Ambient Temperature

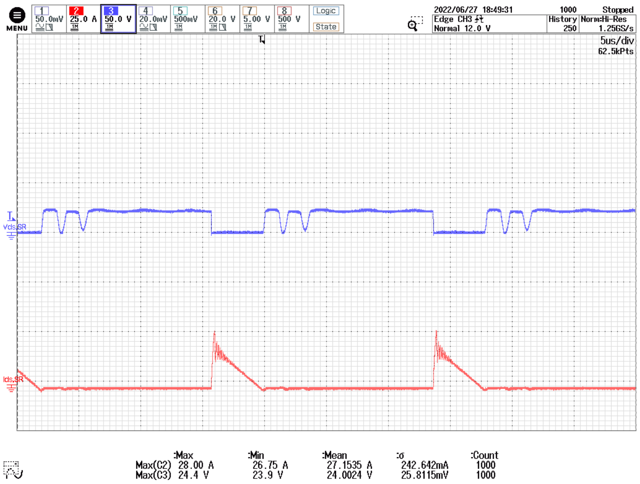


Figure 53 – Synch. Rectifier Drain Voltage and Current.
80 V_{DC}, 2.333 A Load, 85 °C Ambient.
CH3: $V_{DS(SR)}$, 50 V / div.
CH2: $I_{D(SR)}$, 25 A / div.
Time: 5 µs / div.

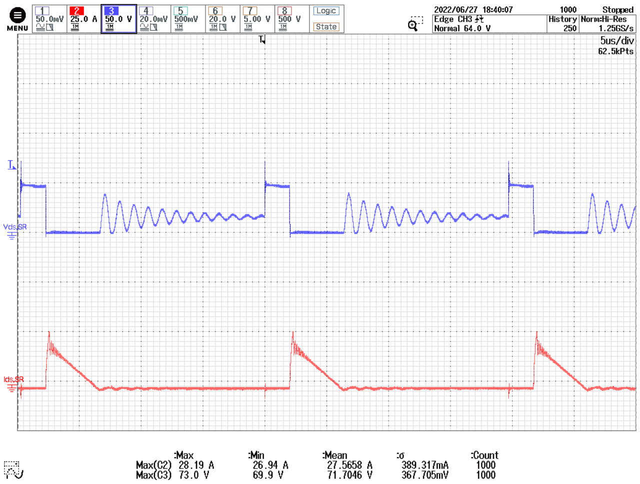


Figure 54 – Synch. Rectifier Drain Voltage and Current.
400 V_{DC}, 2.333 A Load, 85 °C Ambient.
CH3: $V_{DS(SR)}$, 50 V / div.
CH2: $I_{D(SR)}$, 25 A / div.
Time: 5 µs / div.

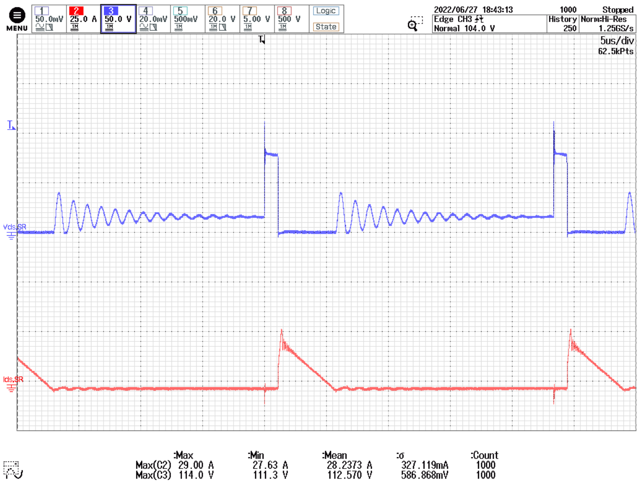


Figure 55 – Synch. Rectifier Drain Voltage and Current.
800 V_{DC}, 2.333 A Load, 85 °C Ambient.
CH1: $V_{DS(SR)}$, 50 V / div.
CH2: $I_{D(SR)}$, 25 A / div.
Time: 5 µs / div.

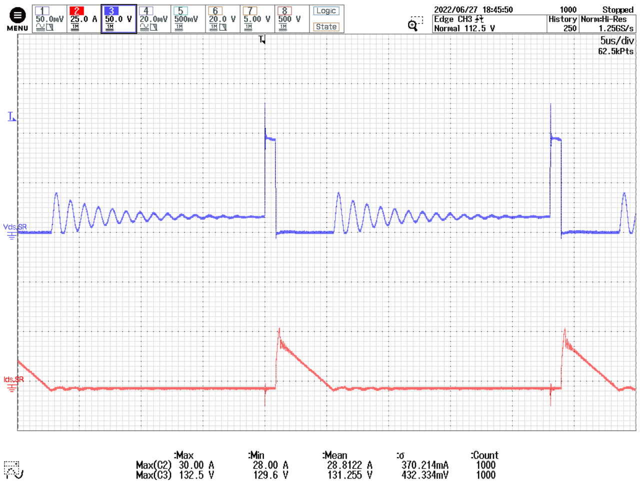


Figure 56 – Synch. Rectifier Drain Voltage and Current.
1000 V_{DC}, 2.333 A Load, 85 °C Ambient.
CH1: $V_{DS(SR)}$, 50 V / div.
CH2: $I_{D(SR)}$, 25 A / div.
Time: 5 µs / div.

11.2.2 Switching Waveforms at 25 °C Ambient Temperature

11.2.2.1 Normal Operation Component Stress

	Steady-State Switching Waveforms 25 °C Ambient, Full Load					
Input	**INN3949CQ**			**SR MOSFETs**		
V_{IN}(V)	**I_D(A)**	**V_{DS}(V)**	**V_{STRESS} (%)**	**I_D(A)[36]**	**V_{DS}(V)[37]**	**V_{STRESS} (%)**
80	1.700	535.0	31.47	28.94	25.0	16.67
400	2.413	848.0	49.88	28.25	71.5	47.67
800	2.775	1188.0	69.88	28.38	112.8	75.20
1000	2.900	1406.0	82.71	28.69	132.0	88.00

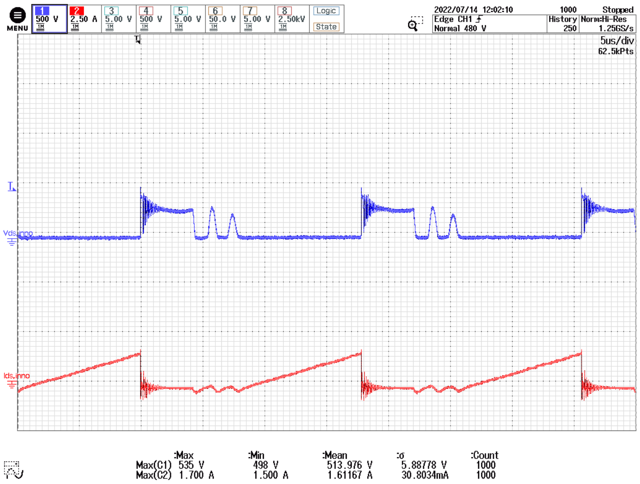
Table 11 – Summary of Critical Component Voltage Stresses at 25 °C Ambient Temperature.

---

[36] Synchronous MOSFET current is the sum of Q1 and Q2 currents.

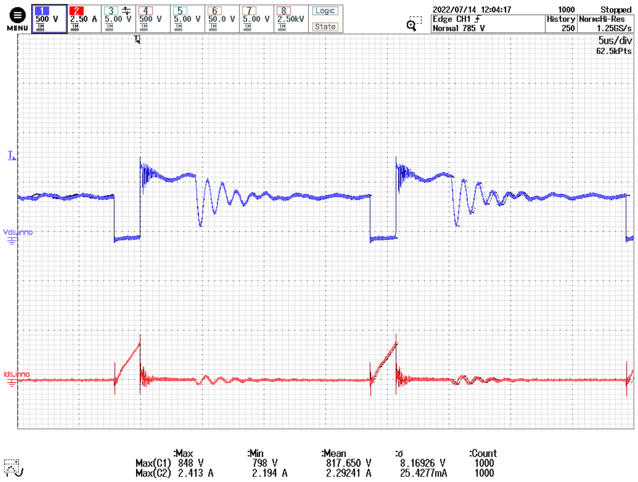
[37] Synchronous MOSFET voltage was taken from Q2.

11.2.2.2 InnoSwitch3-AQ Drain Voltage and Current at 25 °C Ambient Temperature



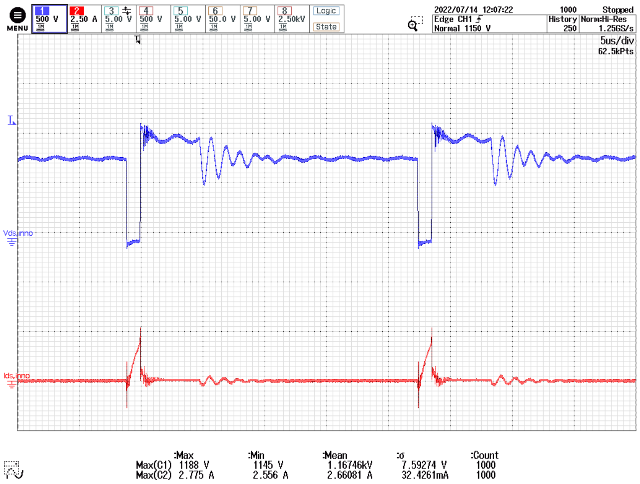
	:Max	:Min	:Mean	:σ	:Count
Max(C1)	535 V	498 V	513.976 V	5.88778 V	1000
Max(C2)	1.700 A	1.500 A	1.61167 A	30.8034mA	1000

Figure 57 – InnoSwitch3-AQ Drain Voltage and Current.
80 V_{DC}, 2.333 A Load, 25 °C Ambient.
CH1: $V_{DS(IC1)}$, 500 V / div.
CH2: $I_{D(IC1)}$, 2.5 A / div.
Time: 5 µs / div.

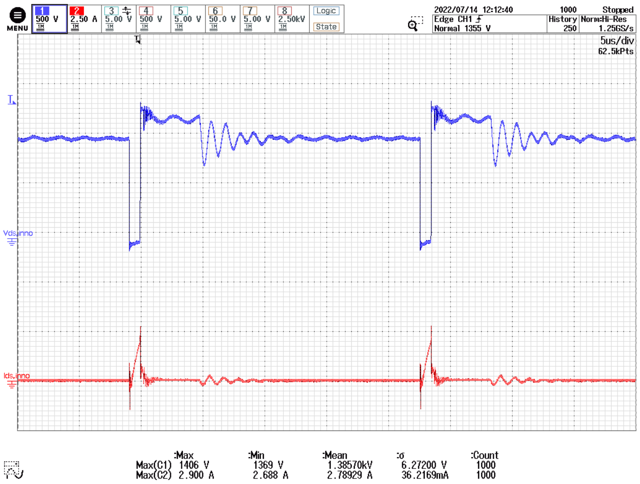


	:Max	:Min	:Mean	:σ	:Count
Max(C1)	848 V	798 V	817.650 V	8.16926 V	1000
Max(C2)	2.413 A	2.194 A	2.29241 A	25.4277mA	1000

Figure 58 – InnoSwitch3-AQ Drain Voltage and Current.
400 V_{DC}, 2.333 A Load, 25 °C Ambient.
CH1: $V_{DS(IC1)}$, 500 V / div.
CH2: $I_{D(IC1)}$, 2.5 A / div.
Time: 5 µs / div.



	:Max	:Min	:Mean	:σ	:Count
Max(C1)	1188 V	1145 V	1.16746kV	7.59274 V	1000
Max(C2)	2.775 A	2.556 A	2.66081 A	32.4261mA	1000

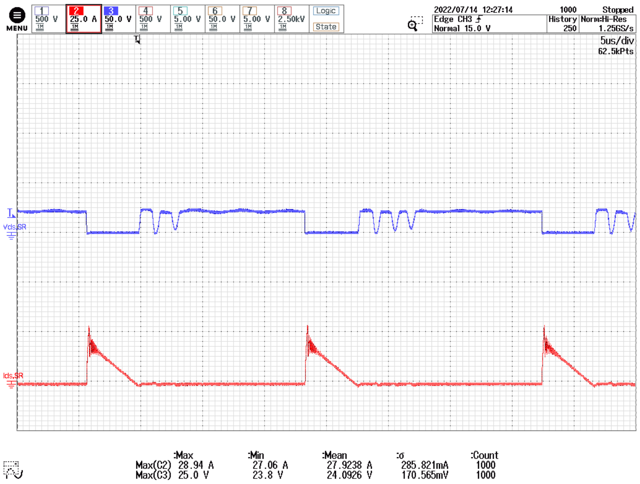


	:Max	:Min	:Mean	:σ	:Count
Max(C1)	1406 V	1369 V	1.38570kV	6.27200 V	1000
Max(C2)	2.900 A	2.688 A	2.78929 A	36.2169mA	1000

Figure 59 – InnoSwitch3-AQ Drain Voltage and Current.
800 V_{DC}, 2.333 A Load, 25 °C Ambient.
CH1: $V_{DS(IC1)}$, 500 V / div.
CH2: $I_{D(IC1)}$, 2.5 A / div.
Time: 5 µs / div.

Figure 60 – InnoSwitch3-AQ Drain Voltage and Current.
1000 V_{DC}, 2.333 A Load, 25 °C Ambient.
CH1: $V_{DS(IC1)}$, 500 V / div.
CH2: $I_{D(IC1)}$, 2.5 A / div.
Time: 5 µs / div.

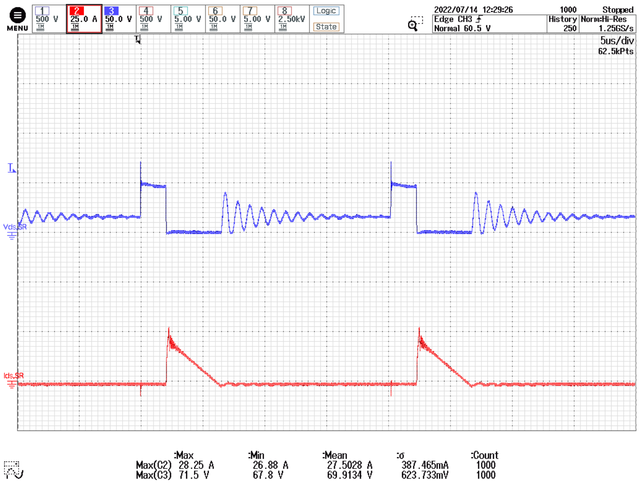
11.2.2.3 Synchronous Rectifier MOSFETs Drain Voltage and Current at 25 °C Ambient Temperature



```
2022/07/14 12:27:14        1000   Stopped
Edge CH3              History Norm:Hi-Res
Normal 15.0 V             250    1.25GS/s

           :Max      :Min     :Mean       :σ          :Count
Max(C2)  28.94 A   27.06 A   27.9238 A   285.821mA   1000
Max(C3)  25.0 V    23.8 V    24.0926 V   170.565mV   1000
```

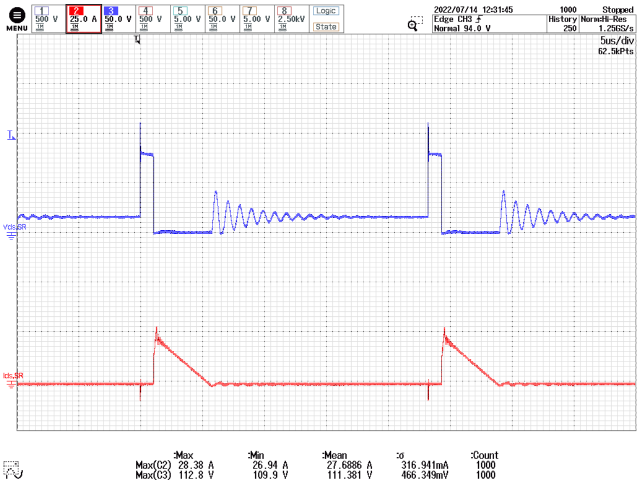
Figure 61 – Synch. Rectifier Drain Voltage and Current.
80 V_{DC}, 2.333 A Load, 25 °C Ambient.
CH3: $V_{DS(SR)}$, 50 V / div.
CH2: $I_{D(SR)}$, 25 A / div.
Time: 5 µs / div.



```
2022/07/14 12:29:26        1000   Stopped
Edge CH3              History Norm:Hi-Res
Normal 60.5 V             250    1.25GS/s

           :Max      :Min     :Mean       :σ          :Count
Max(C2)  28.25 A   26.88 A   27.5028 A   387.465mA   1000
Max(C3)  71.5 V    67.8 V    69.9134 V   623.733mV   1000
```

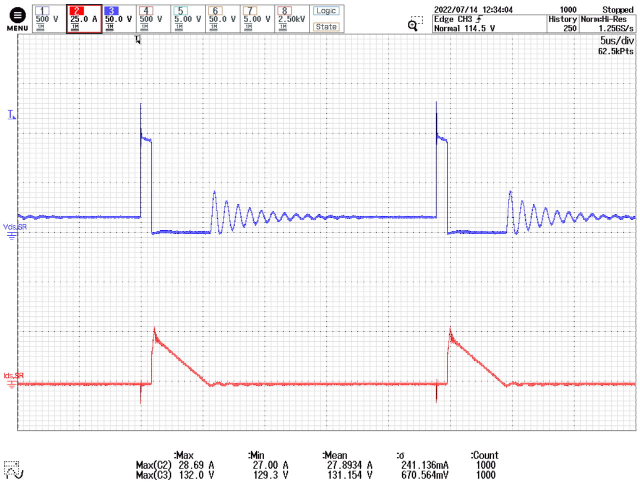
Figure 62 – Synch. Rectifier Drain Voltage and Current.
400 V_{DC}, 2.333 A Load, 25 °C Ambient.
CH3: $V_{DS(SR)}$, 50 V / div.
CH2: $I_{D(SR)}$, 25 A / div.
Time: 5 µs / div.



```
2022/07/14 12:31:45        1000   Stopped
Edge CH3              History Norm:Hi-Res
Normal 94.0 V             250    1.25GS/s

           :Max      :Min     :Mean       :σ          :Count
Max(C2)  28.38 A   26.94 A   27.6886 A   316.941mA   1000
Max(C3)  112.8 V   109.9 V   111.381 V   466.349mV   1000
```

Figure 63 – Synch. Rectifier Drain Voltage and Current.
800 V_{DC}, 2.333 A Load, 25 °C Ambient.
CH1: $V_{DS(SR)}$, 50 V / div.
CH2: $I_{D(SR)}$, 25 A / div.
Time: 5 µs / div.



```
2022/07/14 12:34:04        1000   Stopped
Edge CH3              History Norm:Hi-Res
Normal 114.5 V            250    1.25GS/s

           :Max      :Min     :Mean       :σ          :Count
Max(C2)  28.69 A   27.00 A   27.8934 A   241.136mA   1000
Max(C3)  132.0 V   129.3 V   131.154 V   670.564mV   1000
```

Figure 64 – Synch. Rectifier Drain Voltage and Current.
1000 V_{DC}, 2.333 A Load, 25 °C Ambient.
CH1: $V_{DS(SR)}$, 50 V / div.
CH2: $I_{D(SR)}$, 25 A / div.
Time: 5 µs / div.

11.2.2.4 Short-Circuit Response

The unit is tested by applying output short circuit during normal working conditions and then removing the short circuit to see if the unit will recover and operate normally. The expected response during short-circuit is for the unit to go to AR (auto-restart) mode and attempt recovery every 2.1 seconds. Full load configuration is at 6.43 ohms constant resistance.

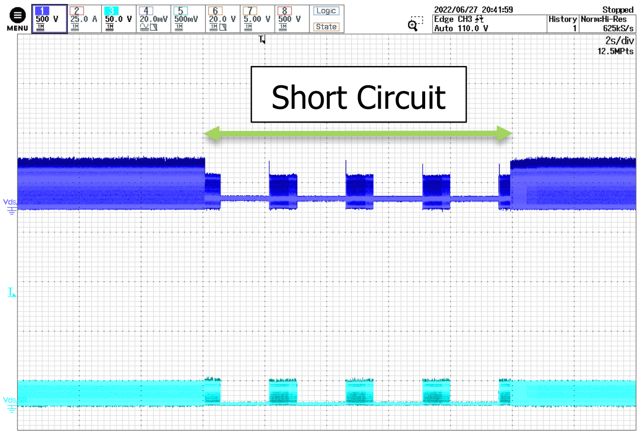


Figure 65 – InnoSwitch3-AQ and SR FET Drain Voltage.
80 V_{DC}, Full Load-Short-Full Load, 85 °C Ambient.
CH1: $V_{DS(IC1)}$, 500 V / div.
CH2: $V_{DS(Q2)}$, 50 V / div.
Time: 2 s / div.

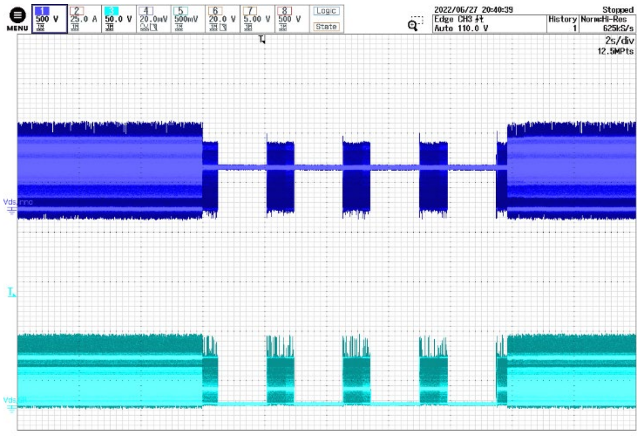


Figure 66 – InnoSwitch3-AQ and SR FET Drain Voltage.
400 V_{DC}, Full Load-Short-Full Load, 85 °C Ambient.
CH1: $V_{DS(IC1)}$, 500 V / div.
CH2: $V_{DS(Q2)}$, 50 V / div.
Time: 2 s / div.

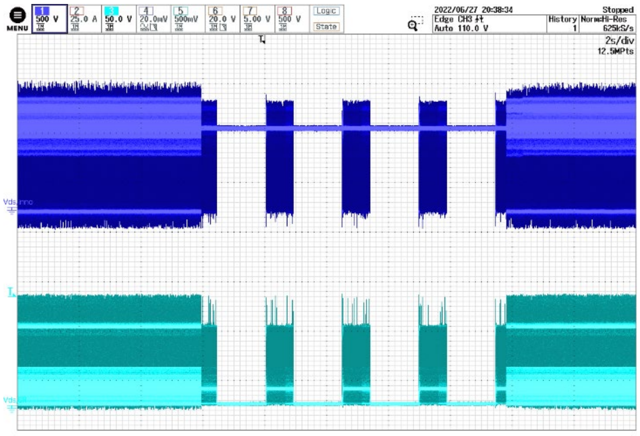


Figure 67 – InnoSwitch3-AQ and SR FET Drain voltage.
800 V_{DC}, Full Load-Short-Full Load, 85 °C Ambient.
CH1: $V_{DS(IC1)}$, 500 V / div.
CH2: $V_{DS(Q2)}$, 50 V / div.
Time: 2 s / div.

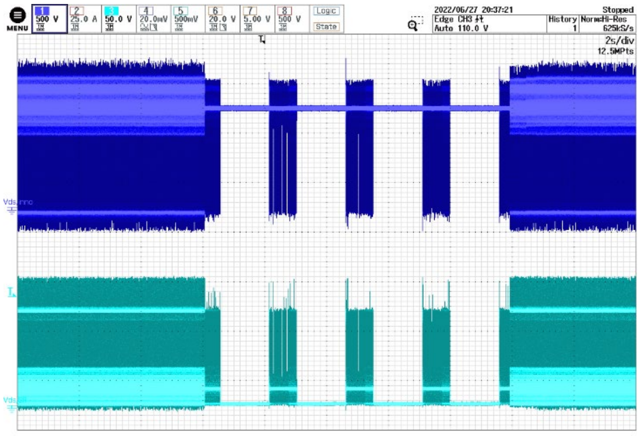


Figure 68 – InnoSwitch3-AQ and SR FET Drain voltage.
1000 V_{DC}, Full Load-Short-Full Load, 85 °C Ambient.
CH1: $V_{DS(IC1)}$, 500 V / div.
CH2: $V_{DS(Q2)}$, 50 V / div.
Time: 2 s / div.

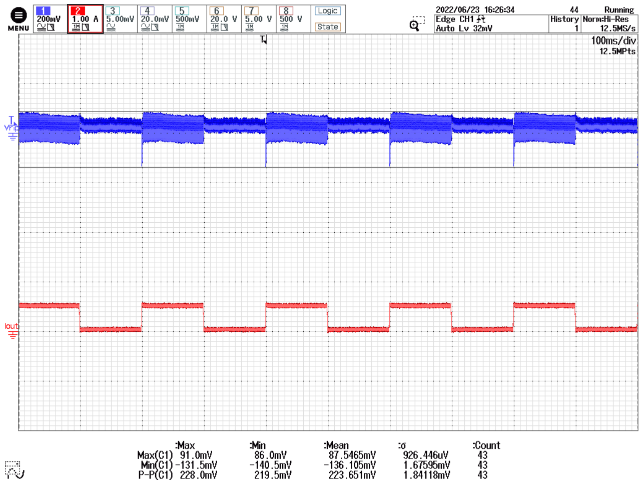
11.3 *Load Transient Response*

Output voltage waveform on the board was captured with dynamic load transient from 0% to 50% and 50% to 100%. The duration for the load states is set to 100 ms and the load slew rate is 100 mA / µs. The test is done at 85 °C ambient temperature.

Dynamic Load Settings	**V_{IN} (V)**	**ΔV_{OUT} (V)**	**$V_{OUT(MAX)}$ (V)**	**$V_{OUT(MIN)}$ (V)**
0% to 50%	60	0.223	15.261	15.0295
	80	0.295	15.2915	14.981
	400	0.284	15.324	15.0215
	800	0.281	15.343	15.0525
	1000	0.308	15.381	15.0635
50% to 100%	60	0.172	15.2705	15.091
	80	0.481	15.295	14.8075
	400	0.231	15.3515	15.114
	800	0.242	15.3775	15.129
	1000	0.254	15.391	15.129

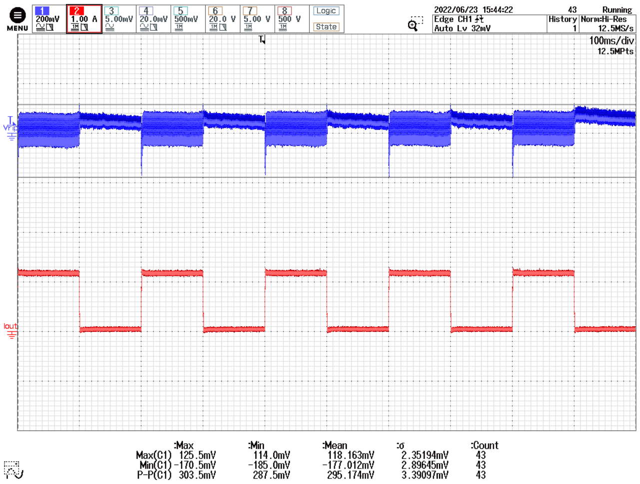
Table 12 – Load Transient Response.

11.3.1 Output Voltage Ripple with 0% to 50% Transient Load at 85 °C Ambient Temperature



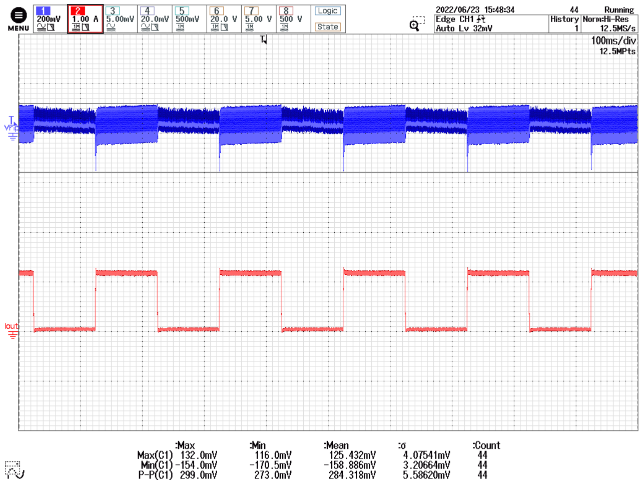
```
          :Max        :Min        :Mean        :σ          :Count
Max(C1)  91.0mV      86.0mV      87.5465mV    926.446uV    43
Min(C1) -131.5mV    -140.5mV    -136.105mV    1.67595mV    43
P-P(C1)  228.0mV     219.5mV     223.651mV    1.84118mV    43
```

Figure 69 – Output Voltage and Current.
60 V_{DC},
0 mA to 500 mA Transient Load,
85 °C Ambient.
CH1: V_{OUT}, 200 mV / div.
CH2: I_{OUT}, 1 A / div.
Time: 100 ms / div.
ΔV = 223.651 mV.



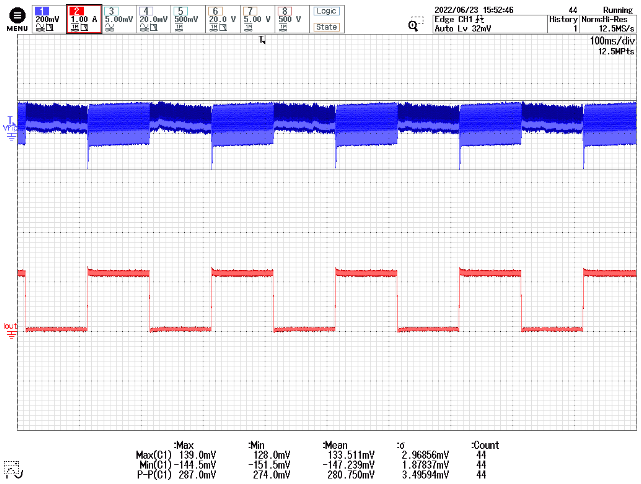
```
          :Max        :Min        :Mean        :σ          :Count
Max(C1)  125.5mV     114.0mV     118.163mV    2.35194mV    43
Min(C1) -170.5mV    -185.0mV    -177.012mV    2.89645mV    43
P-P(C1)  303.5mV     287.5mV     295.174mV    3.39097mV    43
```

Figure 70 – Output Voltage and Current.
80 V_{DC},
0 mA to 1166 mA Transient Load,
85 °C Ambient.
CH1: V_{OUT}, 200 mV / div.
CH2: I_{OUT}, 1 A / div.
Time: 100 ms / div.
ΔV = 295.174 mV.



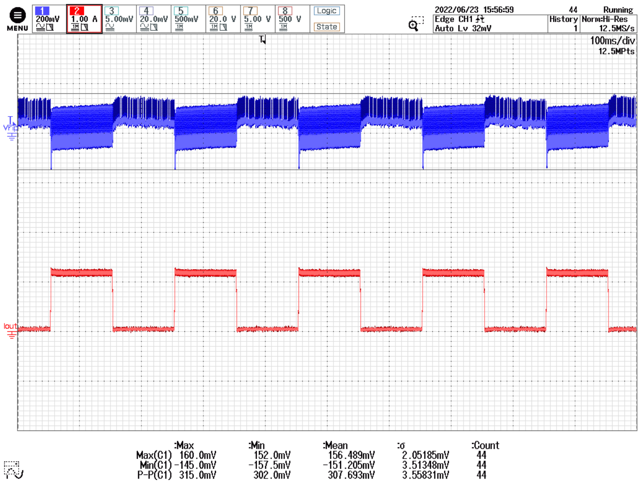
```
          :Max        :Min        :Mean        :σ          :Count
Max(C1)  132.0mV     116.0mV     125.432mV    4.07541mV    44
Min(C1) -154.0mV    -170.5mV    -158.886mV    3.20664mV    44
P-P(C1)  299.0mV     273.0mV     284.318mV    5.58620mV    44
```

Figure 71 – Output Voltage and Current.
400 V_{DC},
0 mA to 1166 mA Transient Load,
85 °C Ambient.
CH1: V_{OUT}, 200 mV / div.
CH2: I_{OUT}, 1 A / div.
Time: 100 ms / div.
ΔV = 284.318 mV.



```
          :Max        :Min        :Mean        :σ          :Count
Max(C1)  139.0mV     128.0mV     133.511mV    2.96856mV    44
Min(C1) -144.5mV    -151.5mV    -147.239mV    1.87837mV    44
P-P(C1)  287.0mV     274.0mV     280.750mV    3.49594mV    44
```

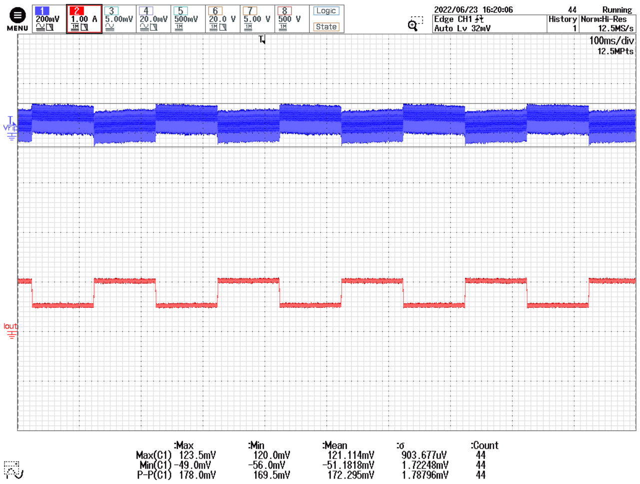
Figure 72 – Output Voltage and Current.
800 V_{DC},
0 mA to 1166 mA Transient Load,
85 °C Ambient.
CH1: V_{OUT}, 200 mV / div.
CH2: I_{OUT}, 1 A / div.
Time: 100 ms / div.
ΔV = 280.750 mV.



```
          :Max        :Min        :Mean         :σ           :Count
Max(C1)  160.0mV     152.0mV     156.489mV     2.05185mV     44
Min(C1) -145.0mV    -157.5mV    -151.205mV     3.51348mV     44
P-P(C1)  315.0mV     302.0mV     307.693mV     3.55831mV     44
```

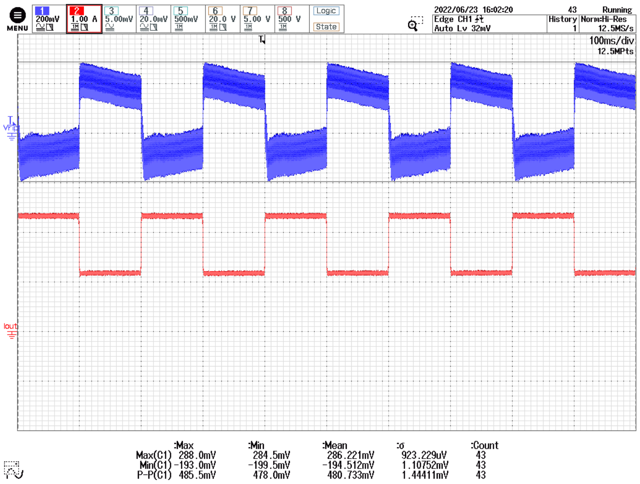
Figure 73 – Output Voltage and Current.
1000 V_{DC},
0 mA to 1166 mA Transient Load,
85 °C Ambient.
CH1: V_{OUT}, 200 mV / div.
CH2: I_{OUT}, 1 A / div.
Time: 100 ms / div.
ΔV = 307.693 mV.

11.3.2 Output Voltage Ripple with 50% to 100% Transient Load at 85 °C Ambient Temperature



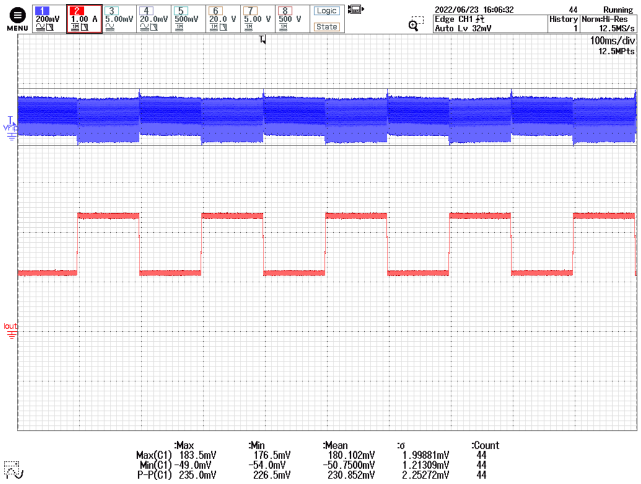
```
          :Max        :Min        :Mean         :σ           :Count
Max(C1)  123.5mV     120.0mV     121.114mV     903.677uV     44
Min(C1) -49.0mV     -56.0mV     -51.1818mV     1.72248mV     44
P-P(C1)  178.0mV     169.5mV     172.295mV     1.78796mV     44
```

Figure 74 – Output Voltage and Current.
60 V_{DC},
500 mA to 1000 mA Transient Load,
85 °C Ambient.
CH1: V_{OUT}, 200 mV / div.
CH2: I_{OUT}, 1 A / div.
Time: 100 ms / div.
ΔV = 172.295 mV.



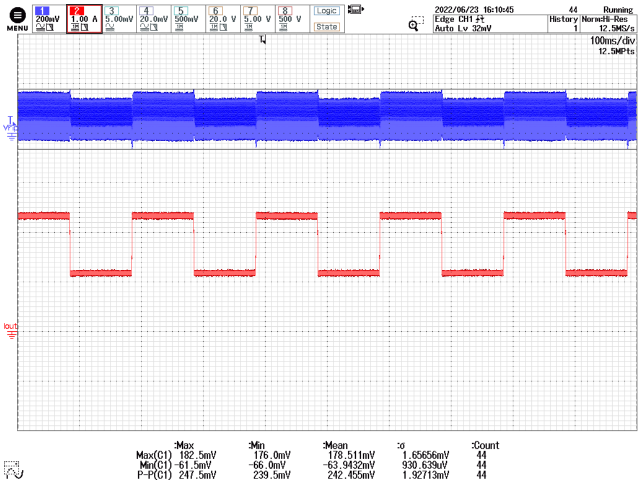
```
          :Max        :Min        :Mean         :σ           :Count
Max(C1)  288.0mV     284.5mV     286.221mV     923.229uV     43
Min(C1) -193.0mV    -199.5mV    -194.512mV     1.10752mV     43
P-P(C1)  485.5mV     478.0mV     480.733mV     1.44411mV     43
```

Figure 75 – Output Voltage and Current.
80 V_{DC},
1166 mA to 2333 mA Transient Load,
85 °C Ambient.
CH1: V_{OUT}, 200 mV / div.
CH2: I_{OUT}, 1 A / div.
Time: 100 ms / div.
ΔV = 480.733 mV.



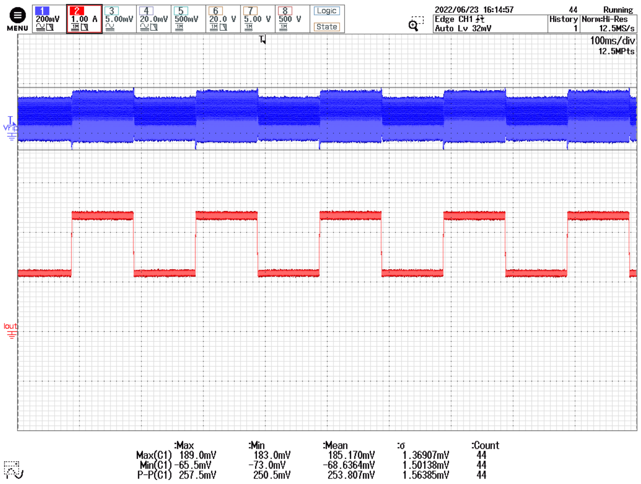
```
          :Max       :Min       :Mean        :σ           :Count
Max(C1)  183.5mV    176.5mV    180.102mV    1.99881mV    44
Min(C1) -49.0mV    -54.0mV    -50.7500mV    1.21309mV    44
P-P(C1)  235.0mV    226.5mV    230.852mV    2.25272mV    44
```

Figure 76 – Output Voltage and Current.
400 V_{DC},
1166 mA to 2333 mA Transient Load,
85 °C Ambient.
CH1: V_{OUT}, 200 mV / div.
CH2: I_{OUT}, 1 A / div.
Time: 100 ms / div.
ΔV = 230.852 mV.



```
          :Max       :Min       :Mean        :σ           :Count
Max(C1)  182.5mV    176.0mV    178.511mV    1.65656mV    44
Min(C1) -61.5mV    -66.0mV    -63.9432mV    930.639uV    44
P-P(C1)  247.5mV    239.5mV    242.455mV    1.92713mV    44
```

Figure 77 – Output Voltage and Current.
800 V_{DC},
1166 mA to 2333 mA Transient Load,
85 °C Ambient.
CH1: V_{OUT}, 200 mV / div.
CH2: I_{OUT}, 1 A / div.
Time: 100 ms / div.
ΔV = 242.455 mV.



```
          :Max       :Min       :Mean        :σ           :Count
Max(C1)  189.0mV    183.0mV    185.170mV    1.36907mV    44
Min(C1) -65.5mV    -73.0mV    -68.6364mV    1.50138mV    44
P-P(C1)  257.5mV    250.5mV    253.807mV    1.56385mV    44
```

Figure 78 – Output Voltage and Current.
1000 V_{DC},
1166 mA to 2333 mA Transient Load,
85 °C Ambient.
CH1: V_{OUT}, 200 mV / div.
CH2: I_{OUT}, 1 A / div.
Time: 100 ms / div.
ΔV = 253.807 mV.

11.4 *Output Ripple Measurements*

11.4.1 Ripple Measurement Technique

For DC output ripple measurements, a modified oscilloscope test probe must be utilized to reduce spurious signals due to pick-up. Details of the probe modification are provided in Figure 79 and Figure 80 below.

A CT2708 probe adapter is affixed with a 1 µF / 50 V ceramic capacitor placed in parallel across the probe tip. A twisted pair of wires kept as short as possible is soldered directly to the probe and the output terminals.

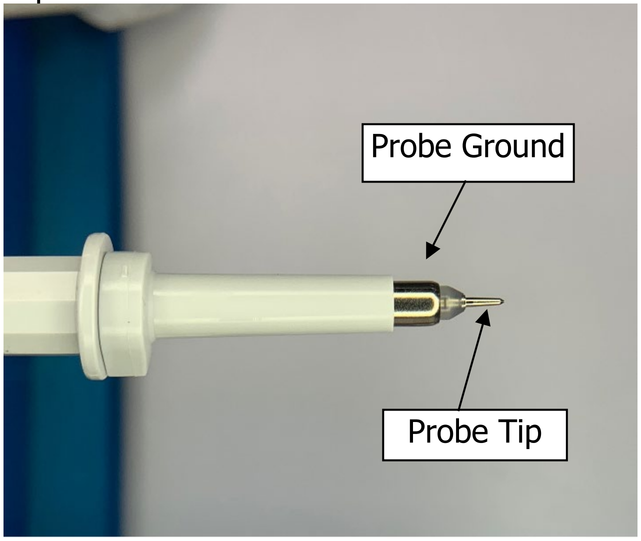


Figure 79 – Oscilloscope Probe Prepared for Ripple Measurement. (End Cap and Ground Lead Removed.)

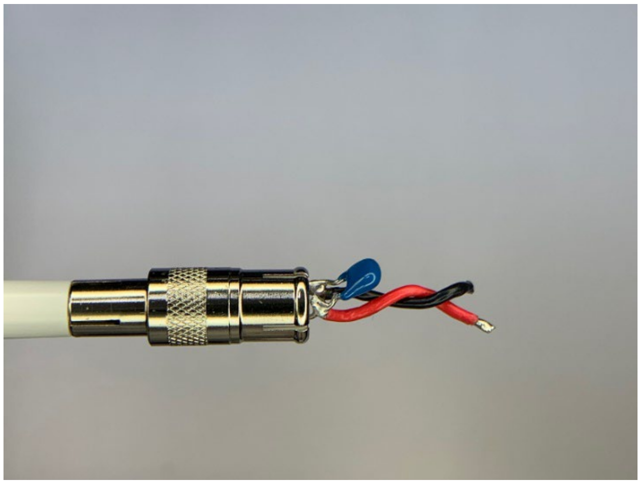


Figure 80 – Oscilloscope Probe with Cal Test CT2708 BNC Adapter. (Modified with Wires for Ripple Measurement, and a Parallel Decoupling Capacitor Added.)

11.4.2 Output Voltage Ripple Waveforms

Output voltage ripple waveform at full load was captured at the output terminals using the ripple measurement probe with decoupling capacitor.

11.4.2.1 Output Voltage Ripple at 85 °C Ambient Constant Full Load[38]

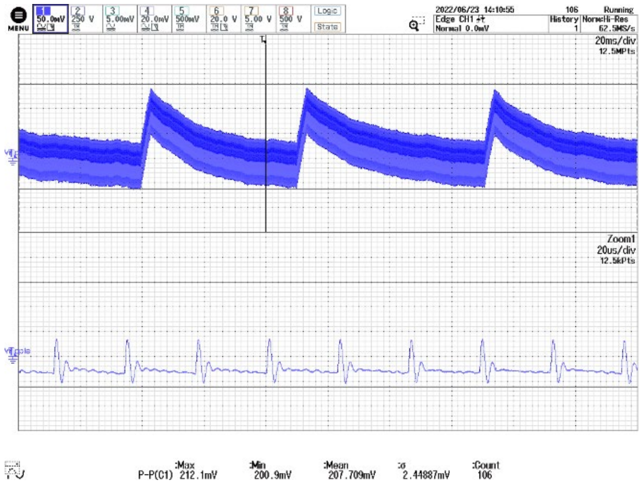


Figure 81 – Output Voltage Ripple.
30 V_{DC}, 500 mA Load, 85 °C Ambient.
CH1: V_{OUT}, 50 mV / div.
Time: 20 ms / div.
V_{RIPPLE} = 207.709 mV.

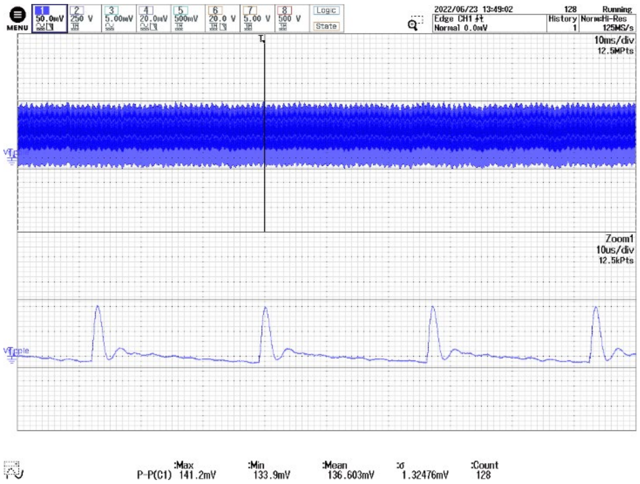


Figure 82 – Output Voltage Ripple.
60 V_{DC}, 1000 mA Load, 85 °C Ambient.
CH1: V_{OUT}, 50 mV / div.
Time: 10 ms / div.
V_{RIPPLE} = 136.603 mV.

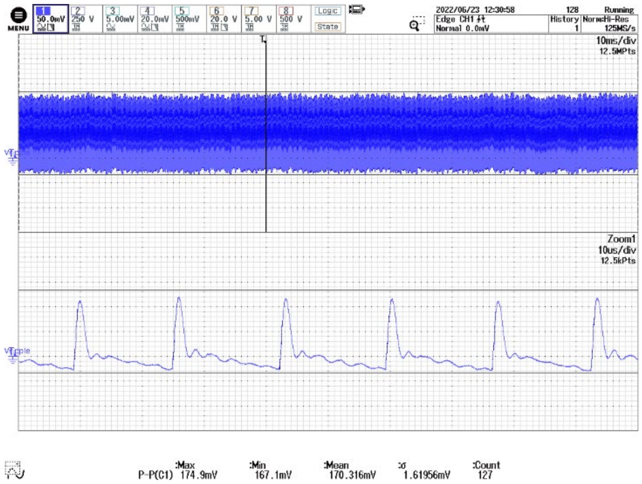


Figure 83 – Output Voltage Ripple.
80 V_{DC}, 2333 mA, 85 °C Ambient.
CH1: V_{OUT}, 50 mV / div.
Time: 10 ms / div.
V_{RIPPLE} = 170.316 mV.

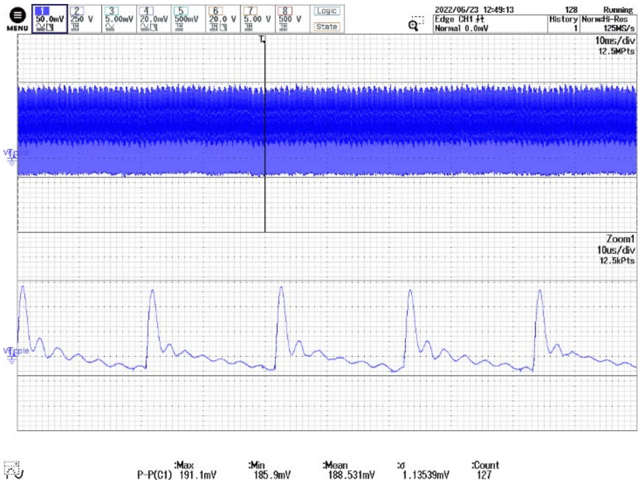
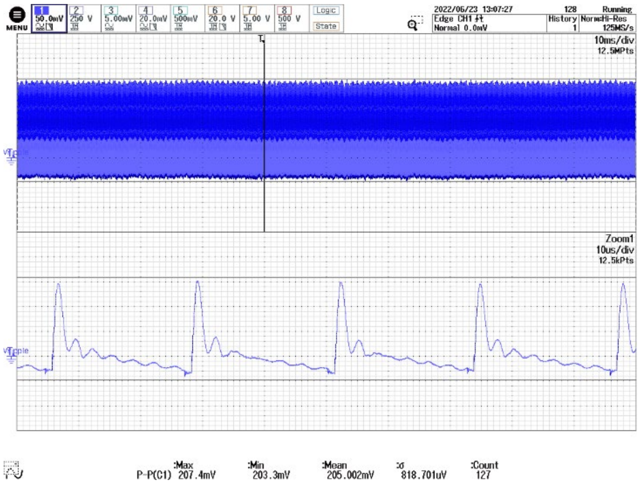


Figure 84 – Output Voltage Ripple.
400 V_{DC}, 2333 mA, 85 °C Ambient.
CH1: V_{OUT}, 50 mV / div.
Time: 10 ms / div.
V_{RIPPLE} = 188.531 mV.

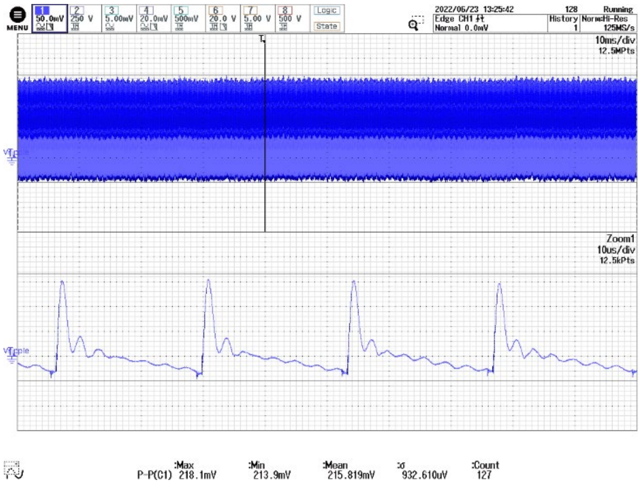
---

[38] Peak-to-peak voltage measurement recorded in each oscilloscope capture is the worst-case ripple which includes both the low frequency and high frequency switching voltage ripple (top portion of each capture).



```
          :Max      :Min      :Mean       :σ          :Count
P-P(C1)  207.4mV   203.3mV   205.002mV   818.701uV   127
```

Figure 85 – Output Voltage Ripple.
800 V_{DC}, 2333 mA, 85 °C Ambient.
CH1: V_{OUT}, 50 mV / div.
Time: 10 ms / div.
V_{RIPPLE} = 205.002 mV.



```
          :Max      :Min      :Mean       :σ          :Count
P-P(C1)  218.1mV   213.9mV   215.819mV   932.610uV   127
```

Figure 86 – Output Voltage Ripple.
1000 V_{DC}, 2333 mA, 85 °C Ambient.
CH1: V_{OUT}, 50 mV / div.
Time: 10 ms / div.
V_{RIPPLE} = 215.819 mV.

11.4.2.2 Output Voltage Ripple at 25 °C Ambient Constant Full Load[39]

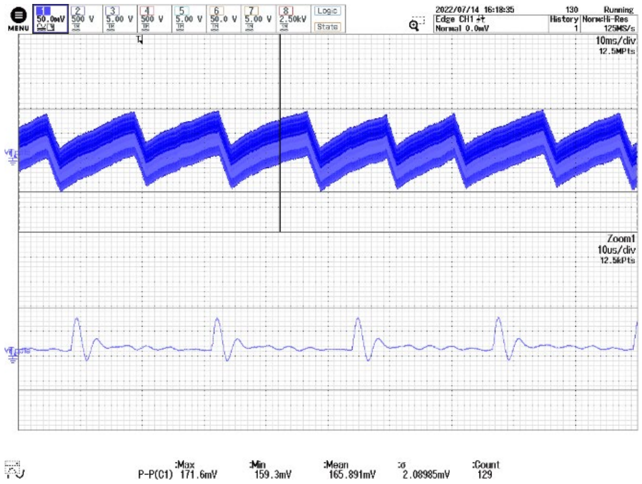


Figure 87 – Output Voltage Ripple.
30 V_{DC}, 500 mA Load, 25 °C Ambient.
CH1: V_{OUT}, 50 mV / div.
Time: 20 ms / div.
V_{RIPPLE} = 165.891 mV.

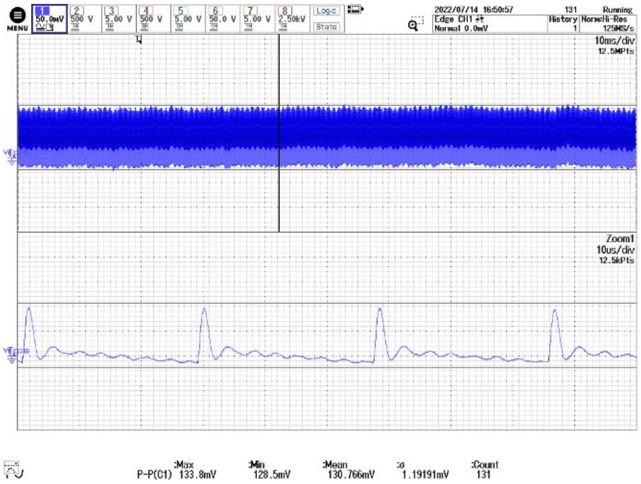


Figure 88 – Output Voltage Ripple.
60 V_{DC}, 1000 mA Load, 25 °C Ambient.
CH1: V_{OUT}, 50 mV / div.
Time: 10 ms / div.
V_{RIPPLE} = 130.766 mV.

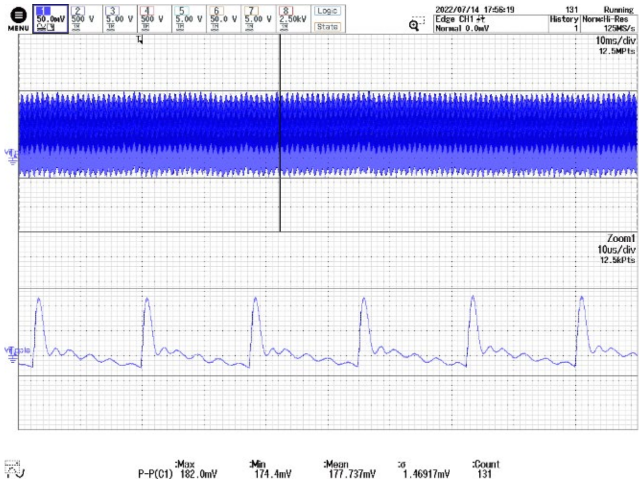


Figure 89 – Output Voltage Ripple.
80 V_{DC}, 2333 mA, 25 °C Ambient.
CH1: V_{OUT}, 50 mV / div.
Time: 10 ms / div.
V_{RIPPLE} = 177.737 mV.

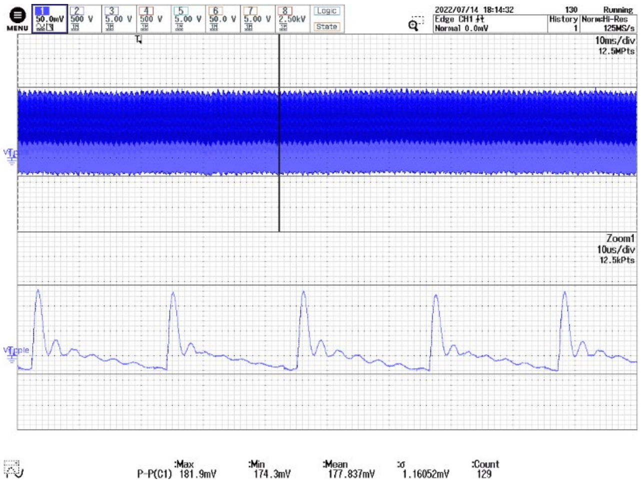


Figure 90 – Output Voltage Ripple.
400 V_{DC}, 2333 mA, 25 °C Ambient.
CH1: V_{OUT}, 50 mV / div.
Time: 10 ms / div.
V_{RIPPLE} = 177.837 mV.

---

[39] Peak-to-peak voltage measurement recorded in each oscilloscope capture is the worst-case ripple which includes both the low frequency and high frequency switching voltage ripple (top portion of each capture).

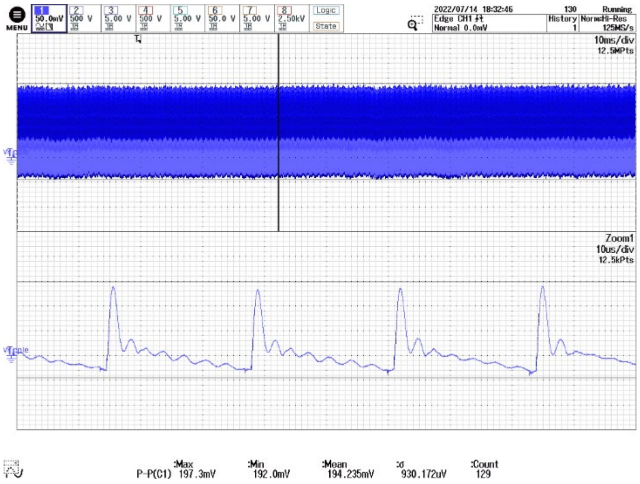


Figure 91 – Output Voltage Ripple.
800 V_{DC}, 2333 mA, 25 °C Ambient.
CH1: V_{OUT}, 50 mV / div.
Time: 10 ms / div.
V_{RIPPLE} = 194.235 mV.

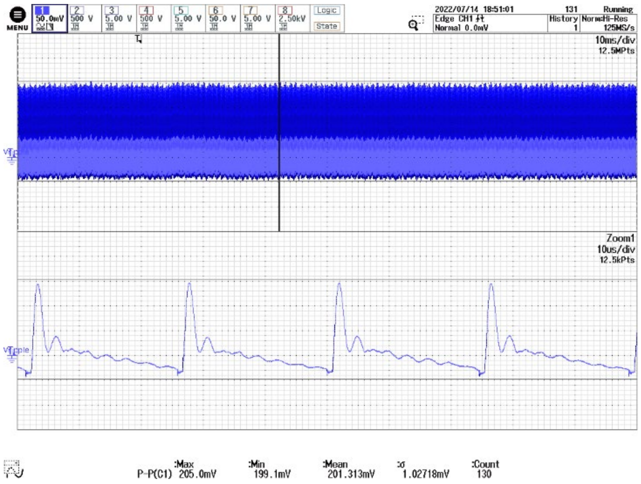


Figure 92 – Output Voltage Ripple.
1000 V_{DC}, 2333 mA, 25 °C Ambient.
CH1: V_{OUT}, 50 mV / div.
Time: 10 ms / div.
V_{RIPPLE} = 201.313 mV.

11.4.2.3 Output Voltage Ripple at -40 °C Ambient Constant Full Load[40]

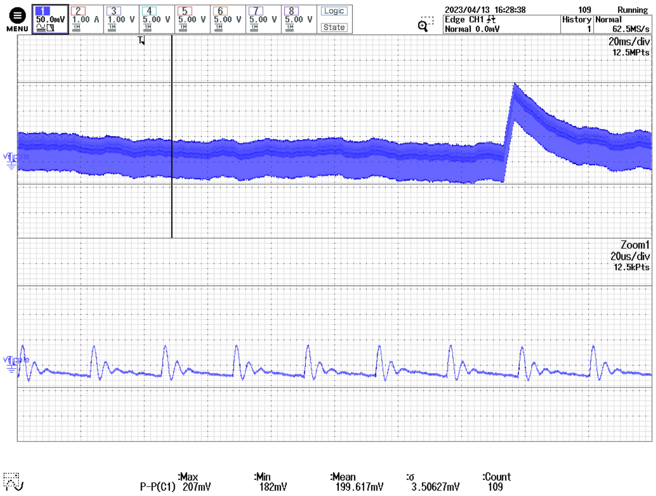


Figure 93 – Output Voltage Ripple.
30 V_{DC}, 500 mA Load, -40 °C Ambient.
CH1: V_{OUT}, 50 mV / div.
Time: 20 ms / div.
V_{RIPPLE} = 199.617 mV.

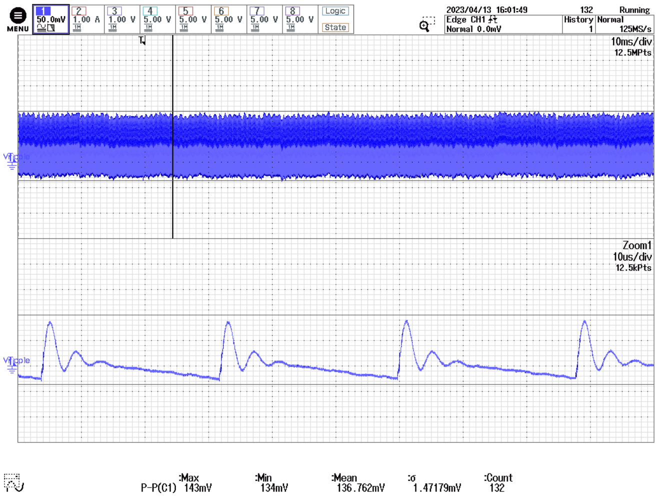


Figure 94 – Output Voltage Ripple.
60 V_{DC}, 1000 mA Load, -40 °C Ambient.
CH1: V_{OUT}, 50 mV / div.
Time: 10 ms / div.
V_{RIPPLE} = 136.762 mV.

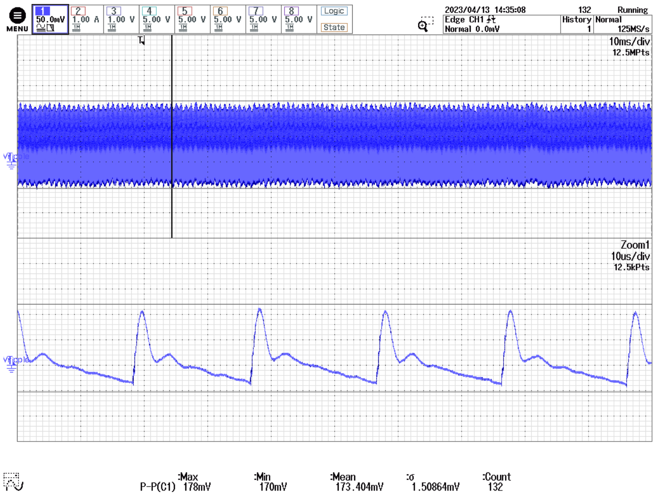


Figure 95 – Output Voltage Ripple.
80 V_{DC}, 2333 mA, -40 °C Ambient.
CH1: V_{OUT}, 50 mV / div.
Time: 10 ms / div.
V_{RIPPLE} = 173.404.737 mV.

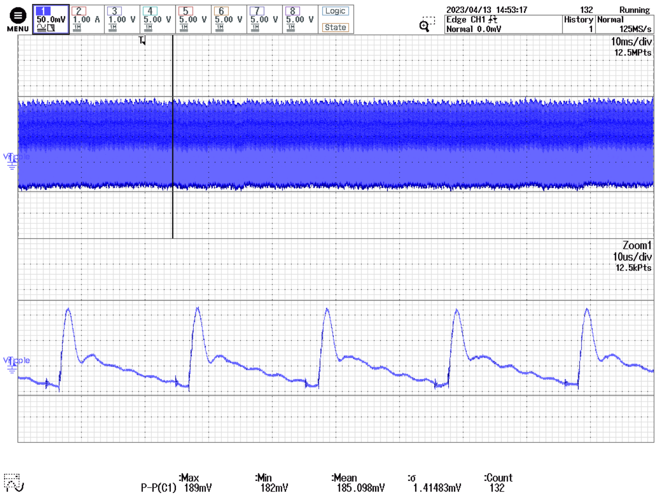
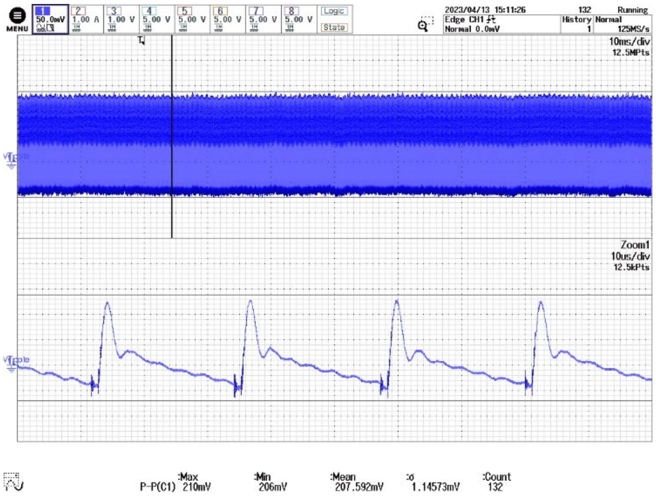


Figure 96 – Output Voltage Ripple.
400 V_{DC}, 2333 mA, -40 °C Ambient.
CH1: V_{OUT}, 50 mV / div.
Time: 10 ms / div.
V_{RIPPLE} = 185.098 mV.

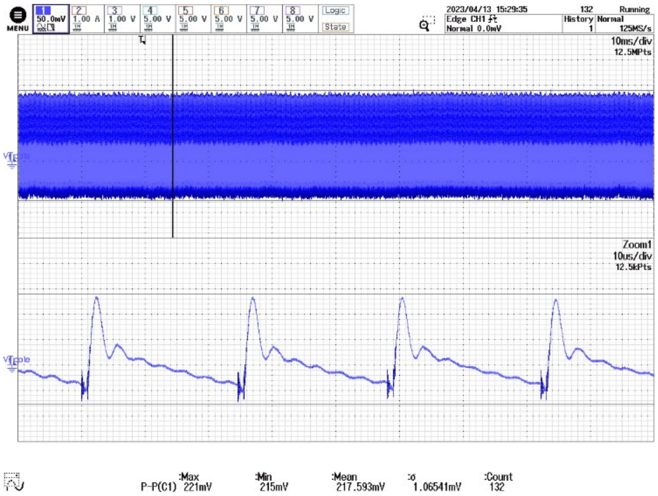
---

[40] Peak-to-peak voltage measurement recorded in each oscilloscope capture is the worst-case ripple which includes both the low frequency and high frequency switching voltage ripple (top portion of each capture).



```
          :Max    :Min    :Mean       :σ          :Count
P-P(C1)   210mV   206mV   207.592mV   1.14573mV   132
```

Figure 97 – Output Voltage Ripple.
800 V_{DC}, 2333 mA, -40 °C Ambient.
CH1: V_{OUT}, 50 mV / div.
Time: 10 ms / div.
V_{RIPPLE} = 207.592 mV.



```
          :Max    :Min    :Mean       :σ          :Count
P-P(C1)   221mV   215mV   217.593mV   1.06541mV   132
```

Figure 98 – Output Voltage Ripple.
1000 V_{DC}, 2333 mA, -40 °C Ambient.
CH1: V_{OUT}, 50 mV / div.
Time: 10 ms / div.
V_{RIPPLE} = 217.593 mV.

11.4.3 Output Ripple vs. Load

11.4.3.1 Output Ripple at 85 °C Ambient

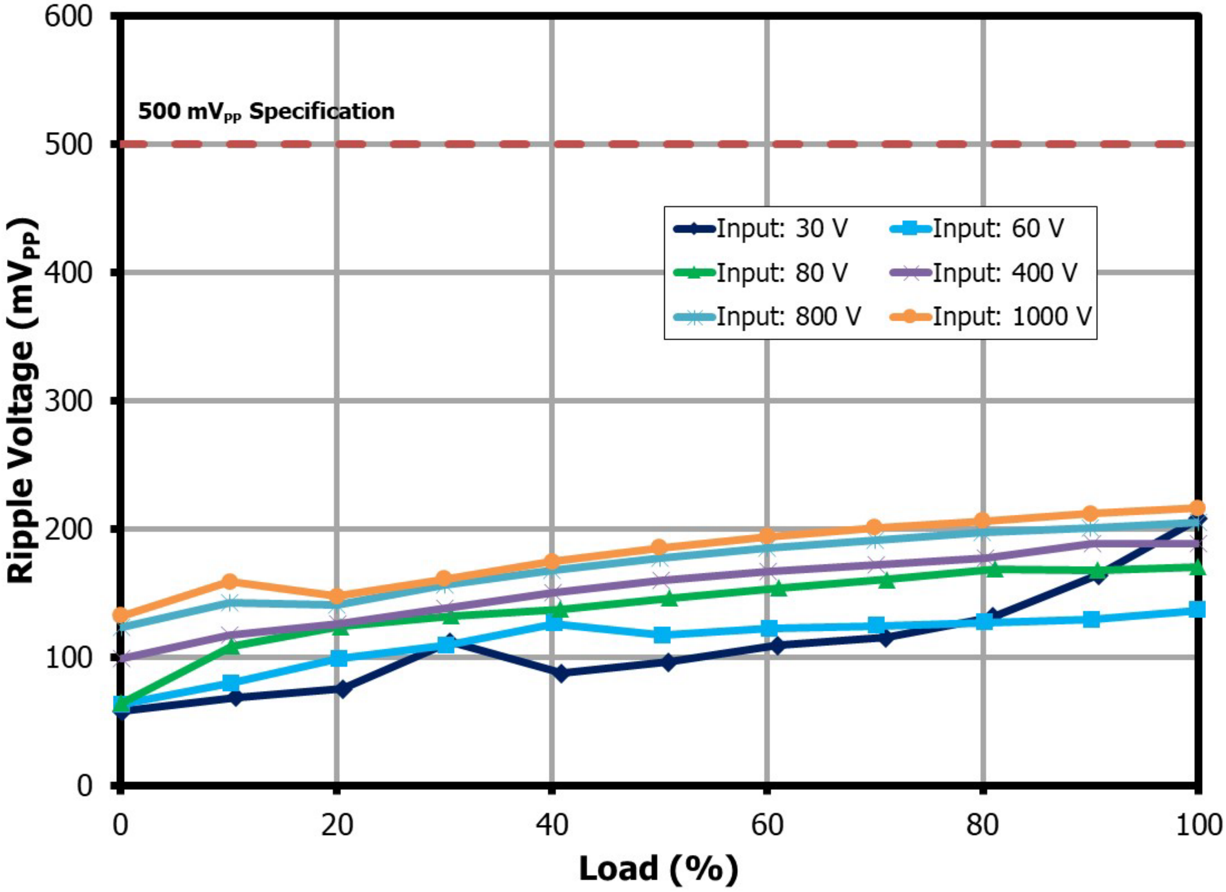


Figure 99 – Output Ripple Voltage Across Full Load Range (85 °C Ambient).[41]

---

[41] 100% load for 60V and 30V input are 1000mA and 500mA, respectively.

11.4.3.2 Output Ripple at 25 °C Ambient

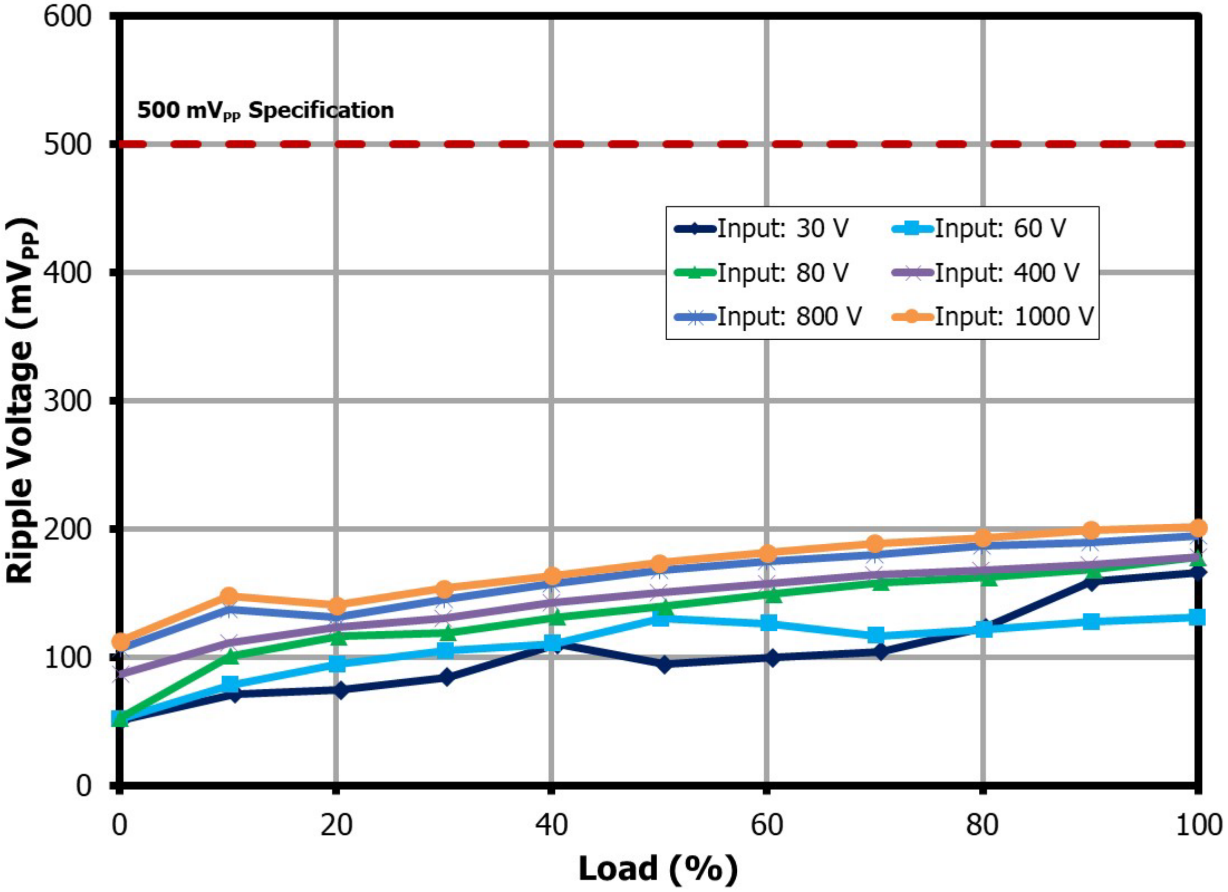


Figure 100 – Output Ripple Voltage Across Full Load Range (25 °C Ambient).[42]

---

[42] 100% load for 60V and 30V input are 1000mA and 500mA, respectively.

11.4.3.3 Output Ripple at -40 °C Ambient

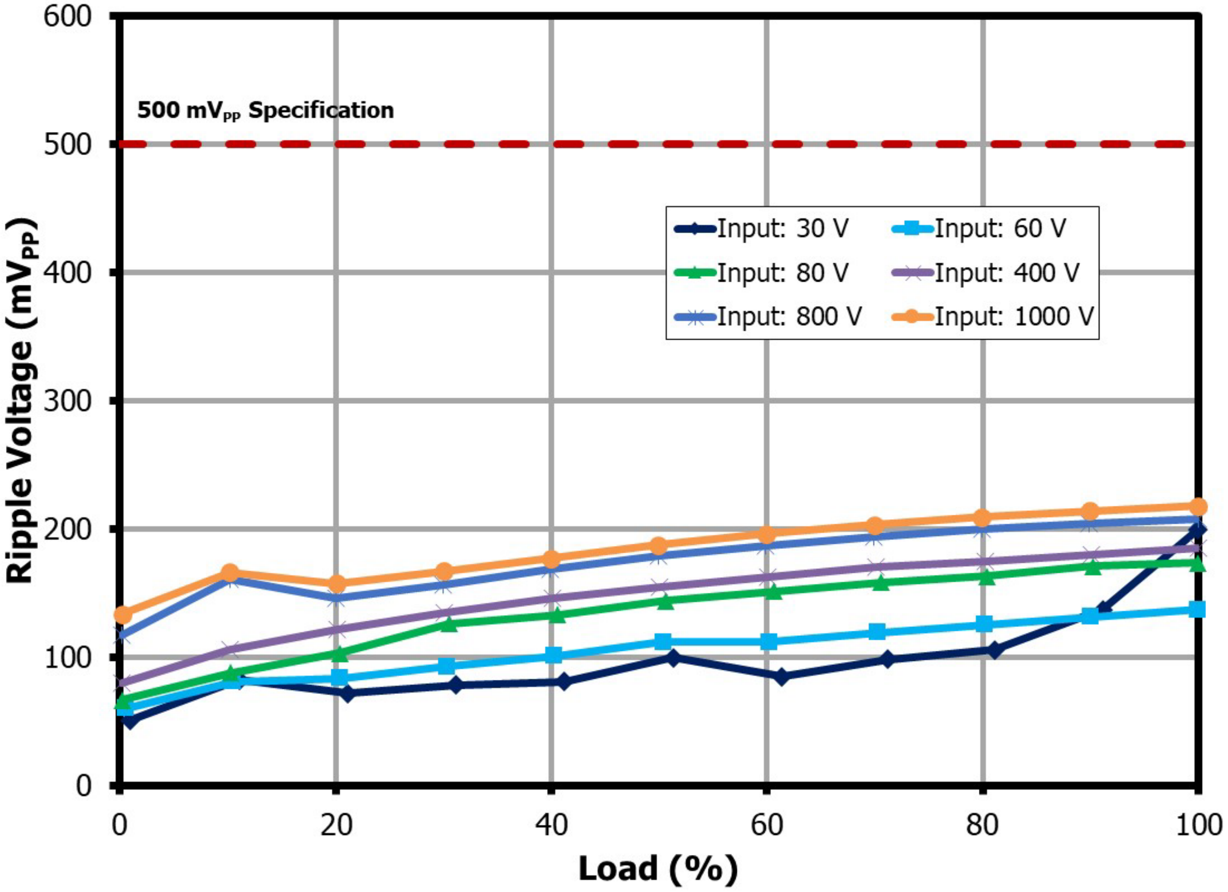


Figure 101 – Output Ripple Voltage Across Full Load Range (-40 °C Ambient).[43]

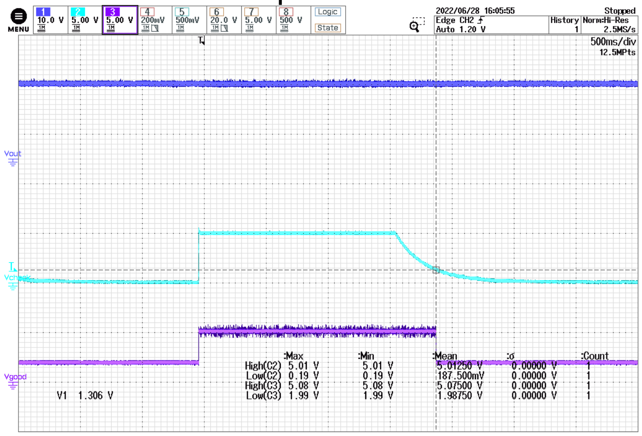
---

[43] 100% load for 60V and 30V input are 1000mA and 500mA, respectively.

12 Diagnostic Circuit

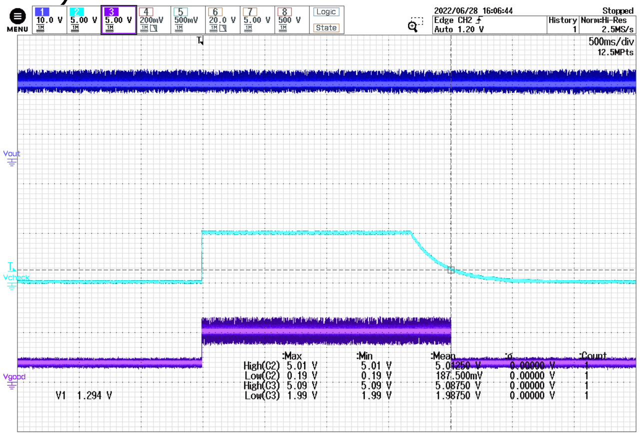
The diagnostic circuit was tested by applying the following signals and settings:

PSU_CHECK: 3.3 V and 5 V
PGOOD_DETECT: 5 V with 300 Ω pull up resistor (10 mA)
15.0 V Output: No-load and Full load (35 W)



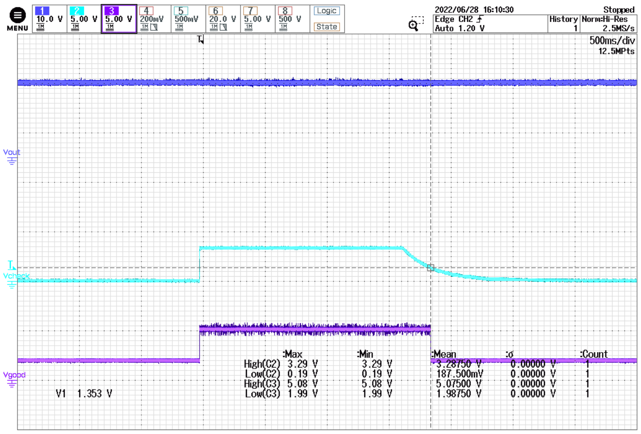
```
          :Max      :Min     :Mean        :σ          :Count
High(C2)  5.01 V    5.01 V   5.01250 V    0.00000 V   1
Low(C2)   0.19 V    0.19 V   187.500mV    0.00000 V   1
High(C3)  5.08 V    5.08 V   5.07500 V    0.00000 V   1
Low(C3)   1.99 V    1.99 V   1.98750 V    0.00000 V   1
```

Figure 102 – Diagnostic Circuit.
PSU_CHECK = 5 V, PGOOD_DETECT = 5 V, No-Load.
CH1: V_{OUT}, 10 V / div.
CH2: V_{PSU_CHECK}, 5 V / div.
CH3: V_{PGOOD_DETECT}, 5 V / div.



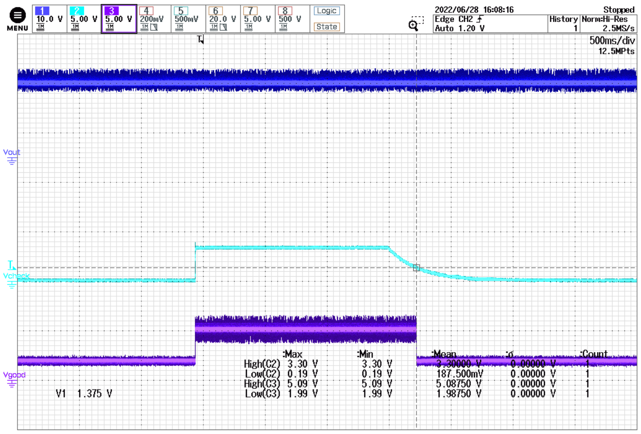
```
          :Max      :Min     :Mean        :σ          :Count
High(C2)  5.01 V    5.01 V   5.01250 V    0.00000 V   1
Low(C2)   0.19 V    0.19 V   187.500mV    0.00000 V   1
High(C3)  5.09 V    5.09 V   5.08750 V    0.00000 V   1
Low(C3)   1.99 V    1.99 V   1.98750 V    0.00000 V   1
```

Figure 103 – Diagnostic Circuit.
PSU_CHECK = 5 V, PGOOD_DETECT = 5 V, Full Load.
CH1: V_{OUT}, 10 V / div.
CH2: V_{PSU_CHECK}, 5 V / div.
CH3: V_{PGOOD_DETECT}, 5 V / div.



```
          :Max      :Min     :Mean        :σ          :Count
High(C2)  3.29 V    3.29 V   3.28750 V    0.00000 V   1
Low(C2)   0.19 V    0.19 V   187.500mV    0.00000 V   1
High(C3)  5.08 V    5.08 V   5.07500 V    0.00000 V   1
Low(C3)   1.99 V    1.99 V   1.98750 V    0.00000 V   1
```

Figure 104 – Diagnostic Circuit.
PSU_CHECK = 3.3 V, PGOOD_DETECT = 5 V, No-Load.
CH1: V_{OUT}, 10 V / div.
CH2: V_{PSU_CHECK}, 5 V / div.
CH3: V_{PGOOD_DETECT}, 5 V / div.



```
          :Max      :Min     :Mean        :σ          :Count
High(C2)  3.30 V    3.30 V   3.30000 V    0.00000 V   1
Low(C2)   0.19 V    0.19 V   187.500mV    0.00000 V   1
High(C3)  5.09 V    5.09 V   5.08750 V    0.00000 V   1
Low(C3)   1.99 V    1.99 V   1.98750 V    0.00000 V   1
```

Figure 105 – Diagnostic Circuit.
PSU_CHECK = 3.3 V, PGOOD_DETECT = 5 V, Full Load.
CH1: V_{OUT}, 10 V / div.
CH2: V_{PSU_CHECK}, 5 V / div.
CH3: V_{PGOOD_DETECT}, 5 V / div.

13 Revision History

Date	Author	Revision	Description & Changes	Reviewed
13-Sep-22	MR	1.0	Initial Release.	Apps & Mktg
09-Jul-23	JS	2.0	Updated and added sections and figures for the data at -40 °C ambient temperature test condition.	

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